12 Power Amplifiers

CHAPTER OBJECTIVES

- The differences between classes A, AB, and C amplifiers
- What causes amplifier distortion
- Efficiency of various classes of amplifiers
- Power calculations for various class amplifiers

12.1 INTRODUCTION–DEFINITIONS AND AMPLIFIER TYPES

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device). In small-signal amplifiers, the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. In Chapter 12, we concentrate on amplifier circuits used to handle large-voltage signals at moderate to high current levels. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal. A brief description of amplifier classes is provided next.

Class A: The output signal varies for a full 360° of the input signal. Figure12.1a shows that this requires the *Q*-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

Class B: A class B circuit provides an output signal varying over one-half the input signal cycle, or for 180° of signal, as shown in Fig. 12.1b. The dc bias point for class B is at 0 V, with the output then varying from this bias point for a half-cycle. Obviously, the

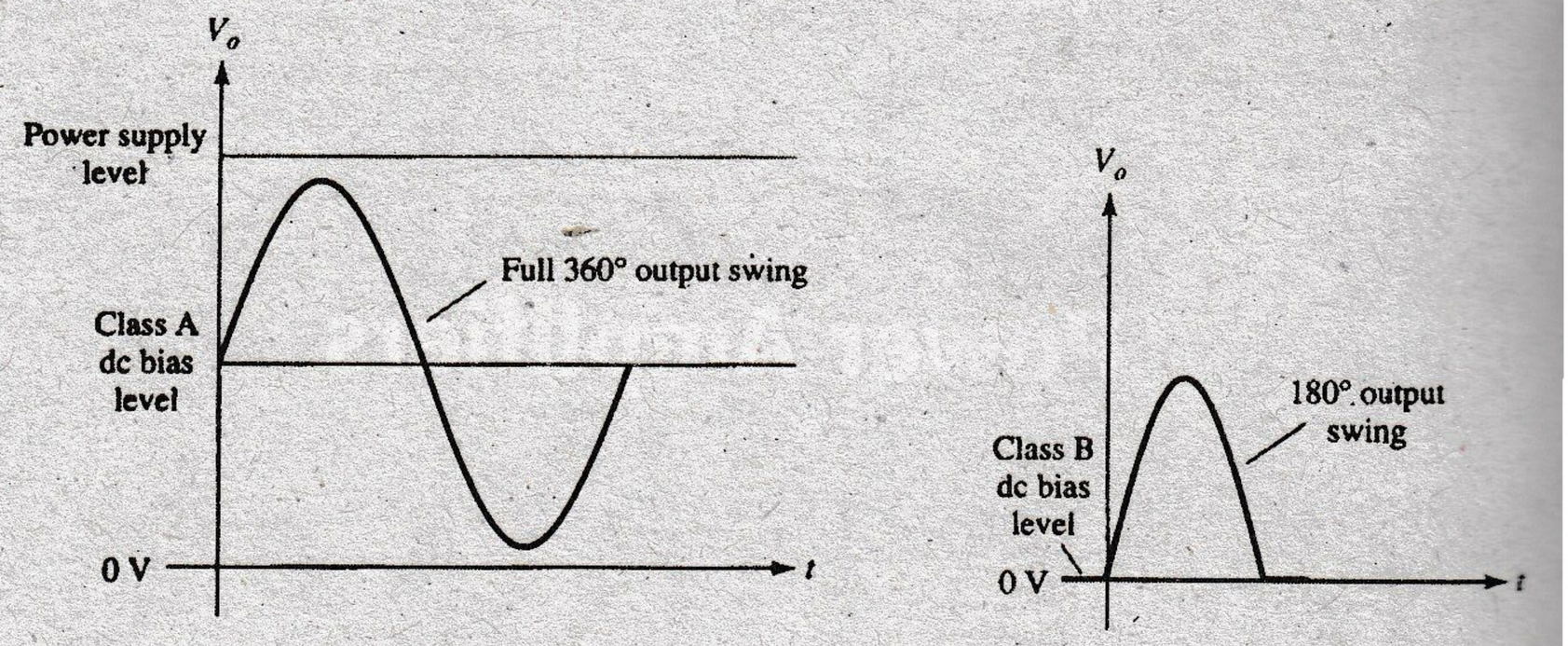


FIG. 12.1
Amplifier operating classes.

output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half-cycle and another to provide operation on the negative-output half-cycle—are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as *push–pull operation*, which is discussed later in this chapter. Note that class B operation by itself creates a very distorted output signal since reproduction of the input takes place for only 180° of the output signal swing.

Class AB: An amplifier may be biased at a dc level above the zero-base-current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push–pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero-base-current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

Class C: The output of a class C amplifier is biased for operation at less than 180° of the cycle and will operate only with a tuned (resonant) circuit, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

Class D: This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample-and-hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is "on" (using power) only for short intervals and the overall efficiency can practically be very high, as described next.

Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%. Table 12.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In class B operation, a push–pull connection is obtained using either a transformer coupling

TABLE 12.1
Comparison of Amplifier Classes

	Class				
	A	AB	B	C[a]	D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

[a]*Class C is usually not used for delivering large amounts of power, and thus the efficiency is not given here.*

or by using complementary (or quasi-complementary) operation with *npn* and *pnp* transistors to provide operation on opposite-polarity cycles. Although transformer operation can provide opposite-cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package. Circuits and examples are provided later in this chapter.

12.2 SERIES-FED CLASS A AMPLIFIER

The simple fixed-bias circuit connection shown in Fig. 12.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

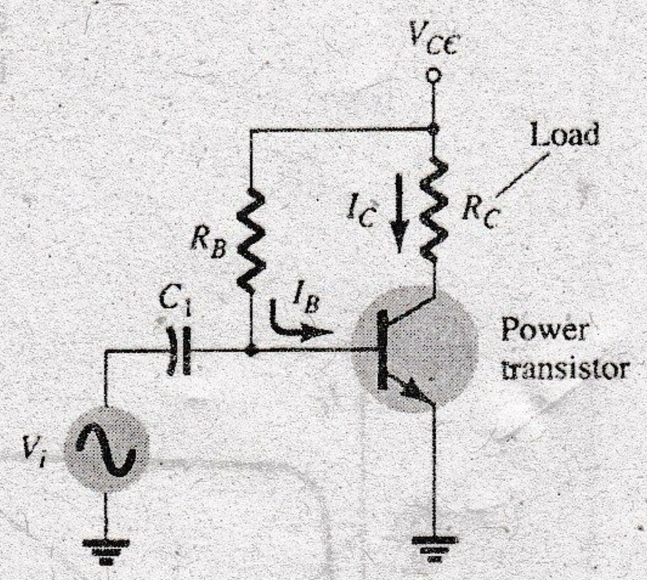


FIG. 12.2
Series-fed class A large-signal amplifier.

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\text{ V}}{R_B} \tag{12.1}$$

with the collector current then being

$$I_C = \beta I_B \tag{12.2}$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C \tag{12.3}$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 12.3. A dc load line is drawn using the

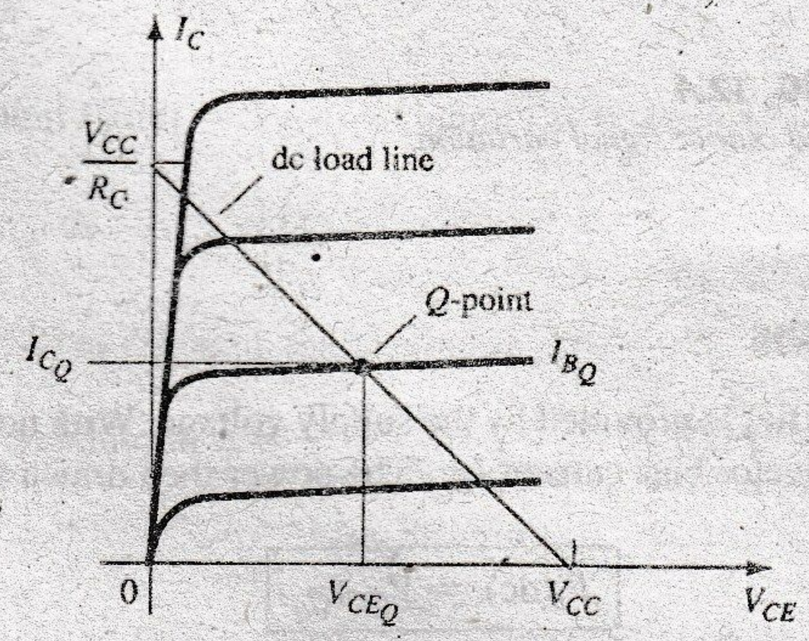


FIG. 12.3
Transistor characteristic showing load line and Q-point.

values of V_{CC} and R_C. The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q-point) for the circuit. The quiescent-point values are those calculated using Eqs. (12.1) through (12.3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and V_{CC}/R_C), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the Q-point set at this optimum bias point, the power considerations for the circuit of Fig. 12.2 are determined as described next.

AC Operation

When an input ac signal is applied to the amplifier of Fig. 12.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 12.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC}/R_C at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC}.

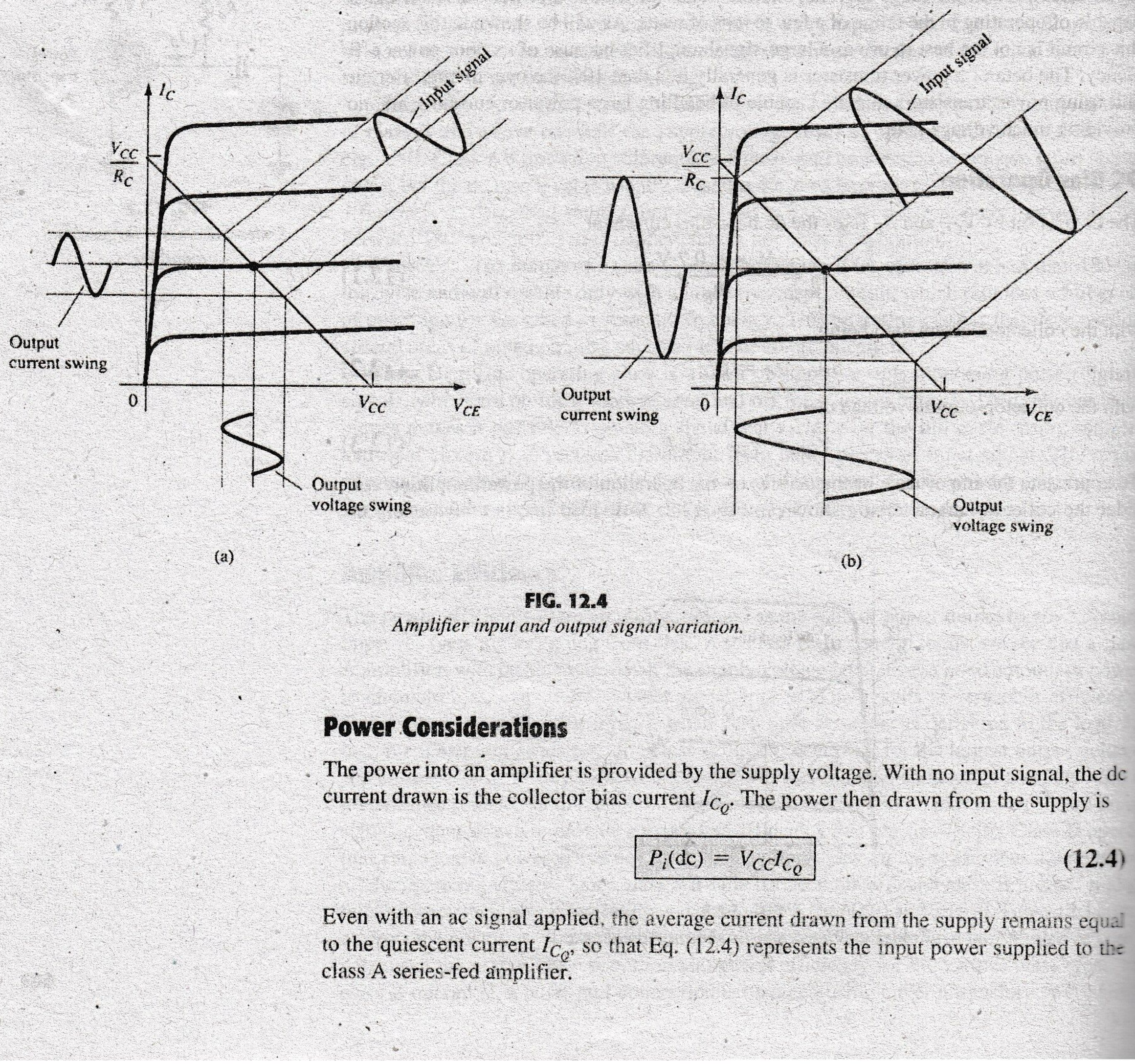


FIG. 12.4
Amplifier input and output signal variation.

Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current I_{C_Q}. The power then drawn from the supply is

$$P_i(\text{dc}) = V_{CC}I_{C_Q} \tag{12.4}$$

Even with an ac signal applied, the average current drawn from the supply remains equal to the quiescent current I_{C_Q}, so that Eq. (12.4) represents the input power supplied to the class A series-fed amplifier.

Output Power The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load R_C in the circuit of Fig. 12.2. The ac signal V_i causes the base current to vary around the dc bias current and the collector current around its quiescent level I_{C_Q}. As shown in Fig. 12.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using RMS signals. The ac power delivered to the load (R_C) may be expressed using

$$\boxed{P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms})} \tag{12.5}$$

$$\boxed{P_o(\text{ac}) = I_C^2(\text{rms})R_C} \tag{12.6}$$

$$\boxed{P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C}} \tag{12.7}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\boxed{\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%} \tag{12.8}$$

Maximum Efficiency For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (12.7) yields

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8} = \frac{V_{CC}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2} = \frac{V_{CC}^2}{2R_C}$$

We can then use Eq. (12.8) to calculate the maximum efficiency:

$$\text{maximum } \%\,\eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\% = 25\%$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

EXAMPLE 12.1 Calculate the input power, output power, and efficiency of the amplifier circuit in Fig. 12.5 for an input voltage that results in a base current of 10 mA peak.

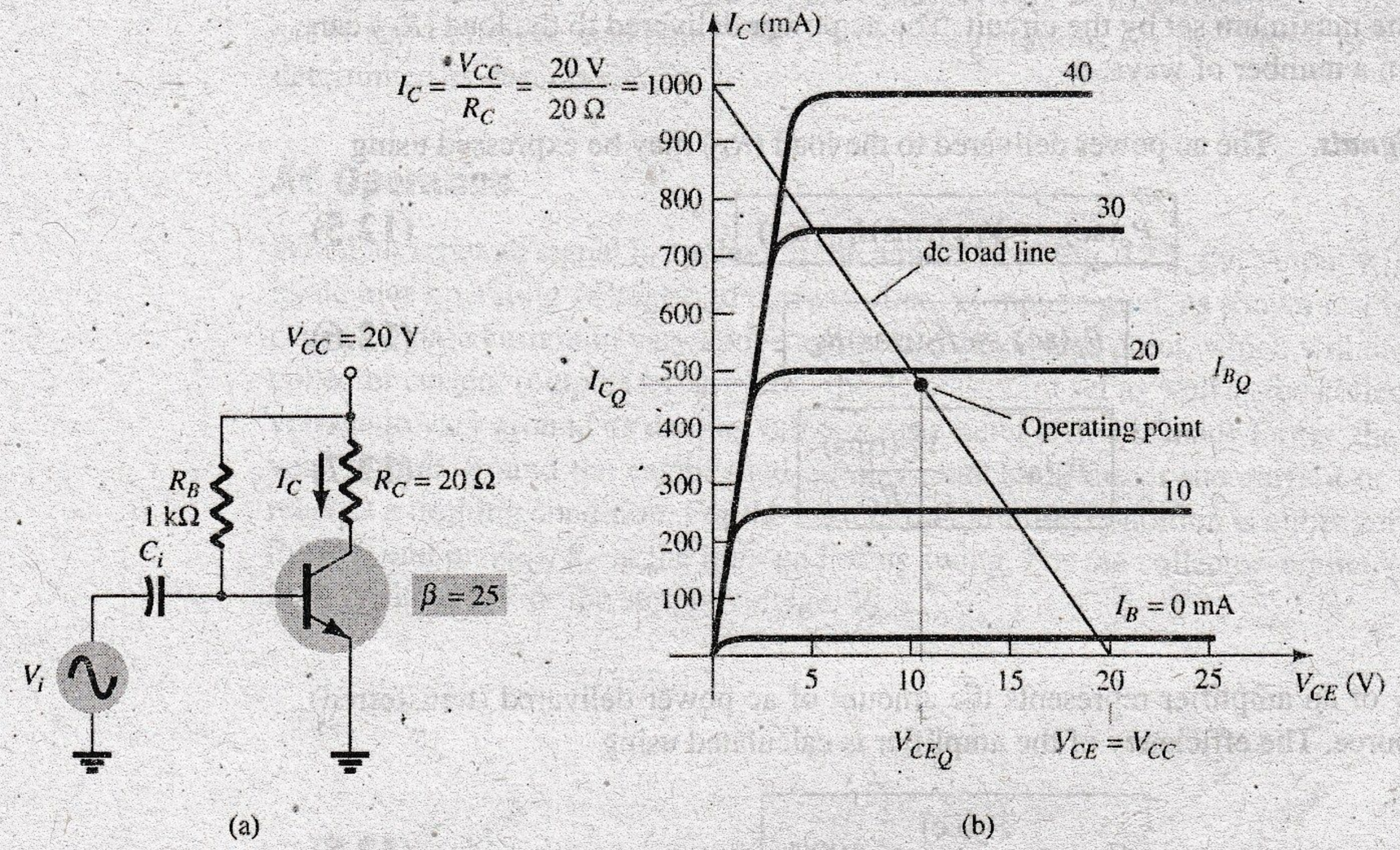


FIG. 12.5
Operation of a series-fed circuit for Example 12.1.

Solution: Using Eqs. (12.1) through (12.3), we can determine the Q-point to be

$$I_{B_Q} = \frac{V_{CC} - 0.7\text{ V}}{R_B} = \frac{20\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 19.3\text{ mA}$$

$$I_{C_Q} = \beta I_B = 25(19.3\text{ mA}) = 482.5\text{ mA} \cong 0.48\text{ A}$$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20\text{ V} - (0.48\ \Omega)(20\ \Omega) = 10.4\text{ V}$$

This bias point is marked on the transistor collector characteristic of Fig. 12.5b. The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 12.5b by connecting $V_{CE} = V_{CC} = 20$ V with $I_C = V_{CC}/R_C = 1000\text{ mA} = 1$ A, as shown. When the input ac base current increases from its dc bias level, the collector current rises by

$$I_C(\text{p}) = \beta I_B(\text{p}) = 25(10\text{ mA peak}) = 250\text{ mA peak}$$

Using Eq. (12.6) yields

$$P_o(\text{ac}) = I_C^2(rms)R_C = \frac{I_C^2(\text{p})}{2}R_C = \frac{(250 \times 10^{-3}\text{ A})^2}{2}(20\ \Omega) = \mathbf{0.625\text{ W}}$$

Using Eq. (12.4) results in

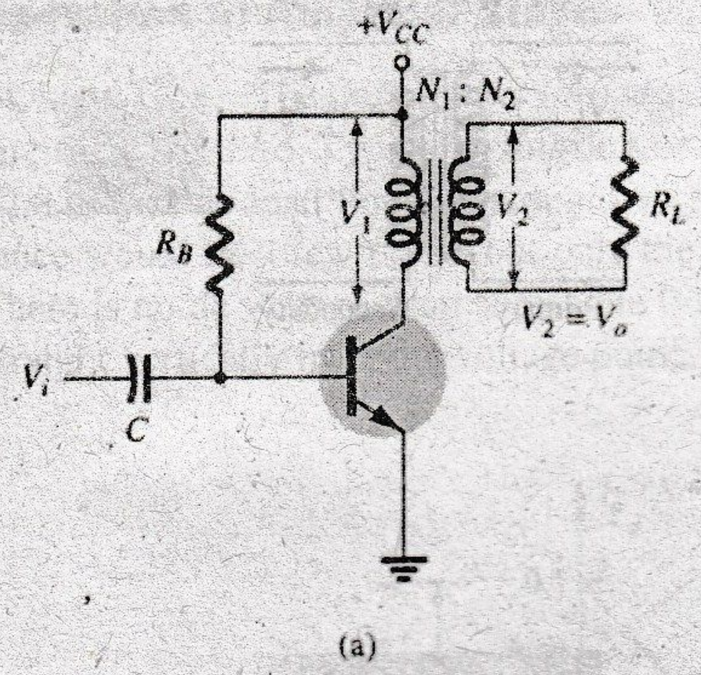
$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (20\text{ V})(0.48\text{ A}) = \mathbf{9.6\text{ W}}$$

The amplifier's power efficiency can then be calculated using Eq. (12.8):

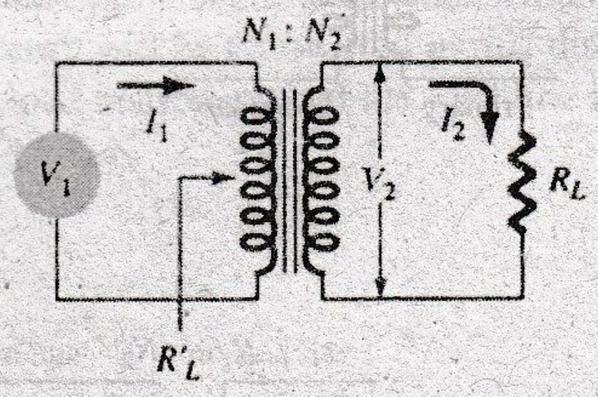
$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.625\text{ W}}{9.6\text{ W}} \times 100\% = \mathbf{6.5\%}$$

12.3 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 12.6. This is a simple circuit form to use in presenting a few basic concepts. More practical circuit versions are covered later.



(a)



(b)

FIG. 12.6
Transformer-coupled audio power amplifier.

Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented next.

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

Voltage Transformation As shown in Fig. 12.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by

$$\boxed{\frac{V_2}{V_1} = \frac{N_2}{N_1}} \qquad \textbf{(12.9)}$$

Equation (12.9) shows that if the number of turns of wire on the secondary side is larger than the number on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

Current Transformation The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by

$$\boxed{\frac{I_2}{I_1} = \frac{N_1}{N_2}} \qquad \textbf{(12.10)}$$

This relationship is shown in Fig. 12.7b. If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

Impedance Transformation Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed. As shown in Fig. 12.7c, an impedance R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R'_L). This can be shown as follows:

$$\frac{R_L}{R'_L} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2 I_1}{I_2 V_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{N_2 N_2}{N_1 N_1} = \left(\frac{N_2}{N_1}\right)^2$$

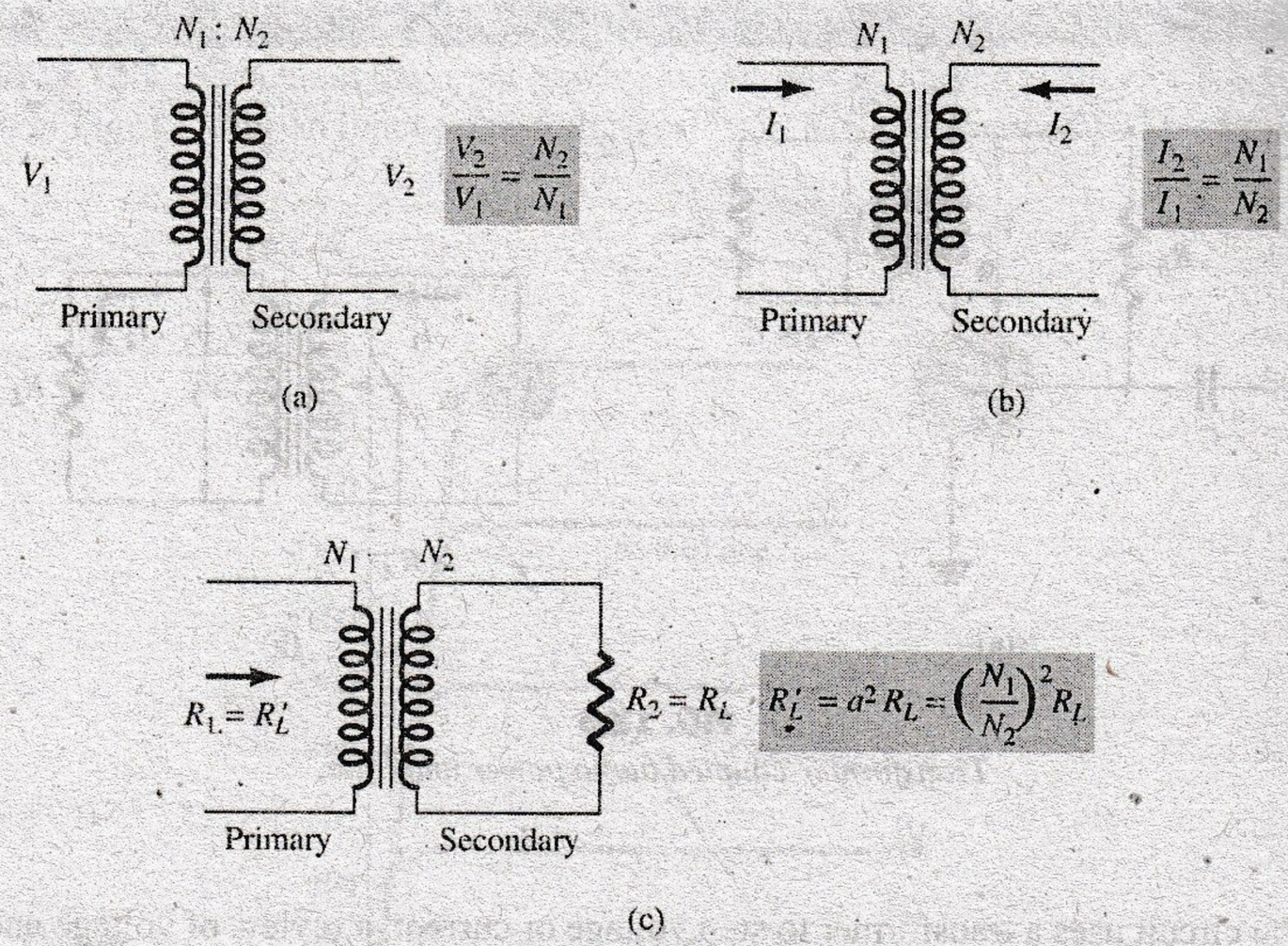


FIG. 12.7
Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

If we define $a = N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes

$$\boxed{\frac{R_L'}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2} \tag{12.11}$$

We can express the load resistance reflected to the primary side as

$$\boxed{R_1 = a^2 R_2} \quad \text{or} \quad \boxed{R_L' = a^2 R_L} \tag{12.12}$$

where R_L' is the reflected impedance. As shown in Eq. (12.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

EXAMPLE 12.2 Calculate the effective resistance seen looking into the primary of a 15:1 transformer connected to an 8-Ω load.

Solution: Eq. (12.22):

$$R_L' = a^2 R_L = (15)^2(8\ \Omega) = 1800\ \Omega = \mathbf{1.8\ k\Omega}$$

EXAMPLE 12.3 What transformer turns ratio is required to match a 16-Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ?

Solution: Eq. (12.11):

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{R_L'}{R_L} = \frac{10\ \text{k}\Omega}{16\ \Omega} = 625$$

$$\frac{N_1}{N_2} = \sqrt{625} = \mathbf{25{:}1}$$

Operation of Amplifier Stage

DC Load Line The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 12.6. Typically, this dc resistance is small (ideally 0 Ω) and, as shown in Fig. 12.8, a 0-Ω dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the 0-Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CE_Q} = V_{CC}$.

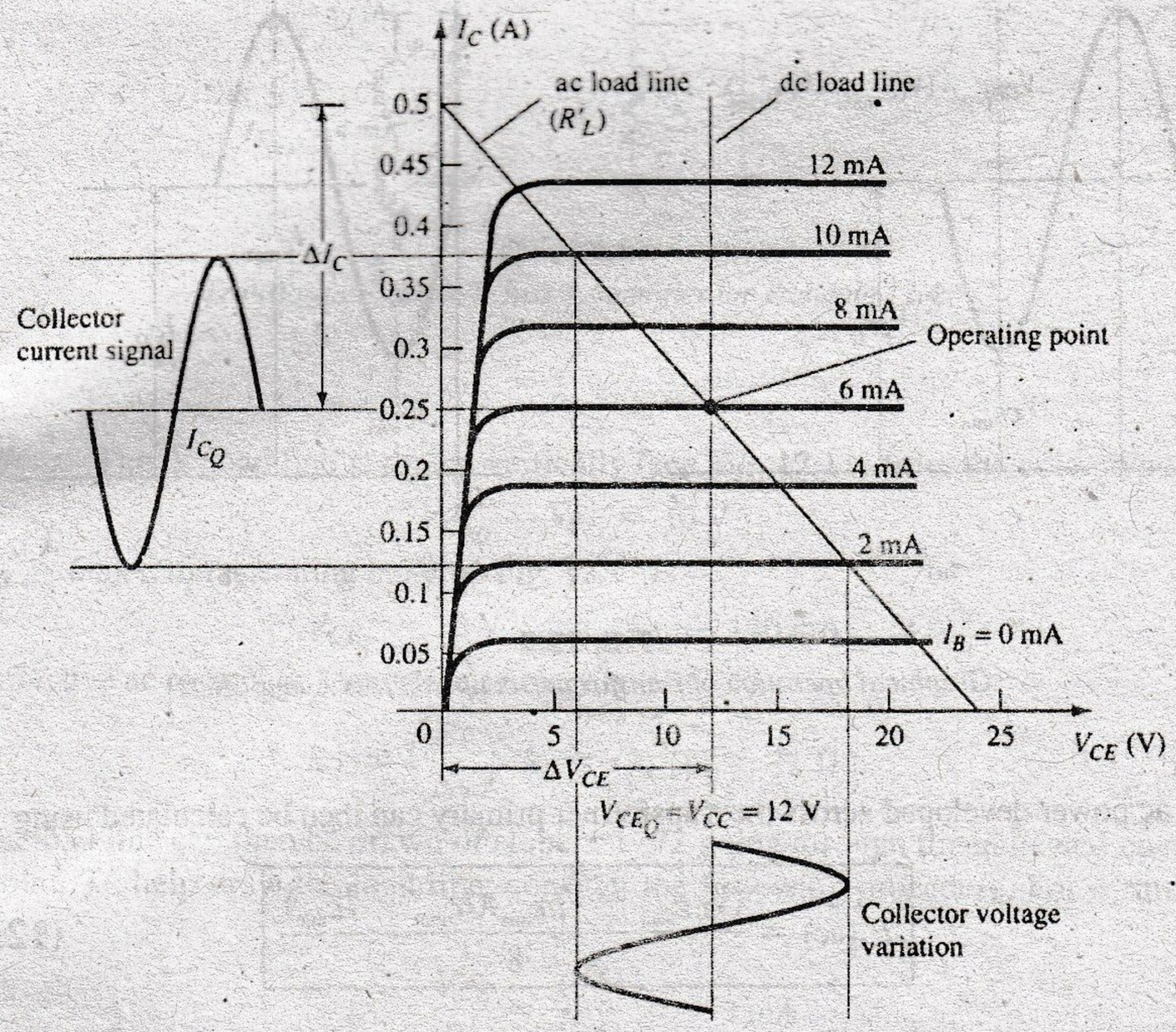


FIG. 12.8
Load lines for class A transformer-coupled amplifier.

Quiescent Operating Point The operating point in the characteristic curve of Fig. 12.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than the maximum of 50%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

AC Load Line To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance (R'_L) is calculated using Eq. (12.12) using the value of the load connected across the secondary (R_L) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to $-1/R'_L$ (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of V_{CC}. In fact, the voltage developed across the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

Signal Swing and Output AC Power Figure 12.9 shows the voltage and current signal swings from the circuit of Fig. 12.6. From the signal variations shown in Fig. 12.9, the values of the peak-to-peak signal swings are

$$V_{CE}(\text{p-p}) = V_{CE_{max}} - V_{CE_{min}}$$
$$I_C(\text{p-p}) = I_{C_{max}} - I_{C_{min}}$$

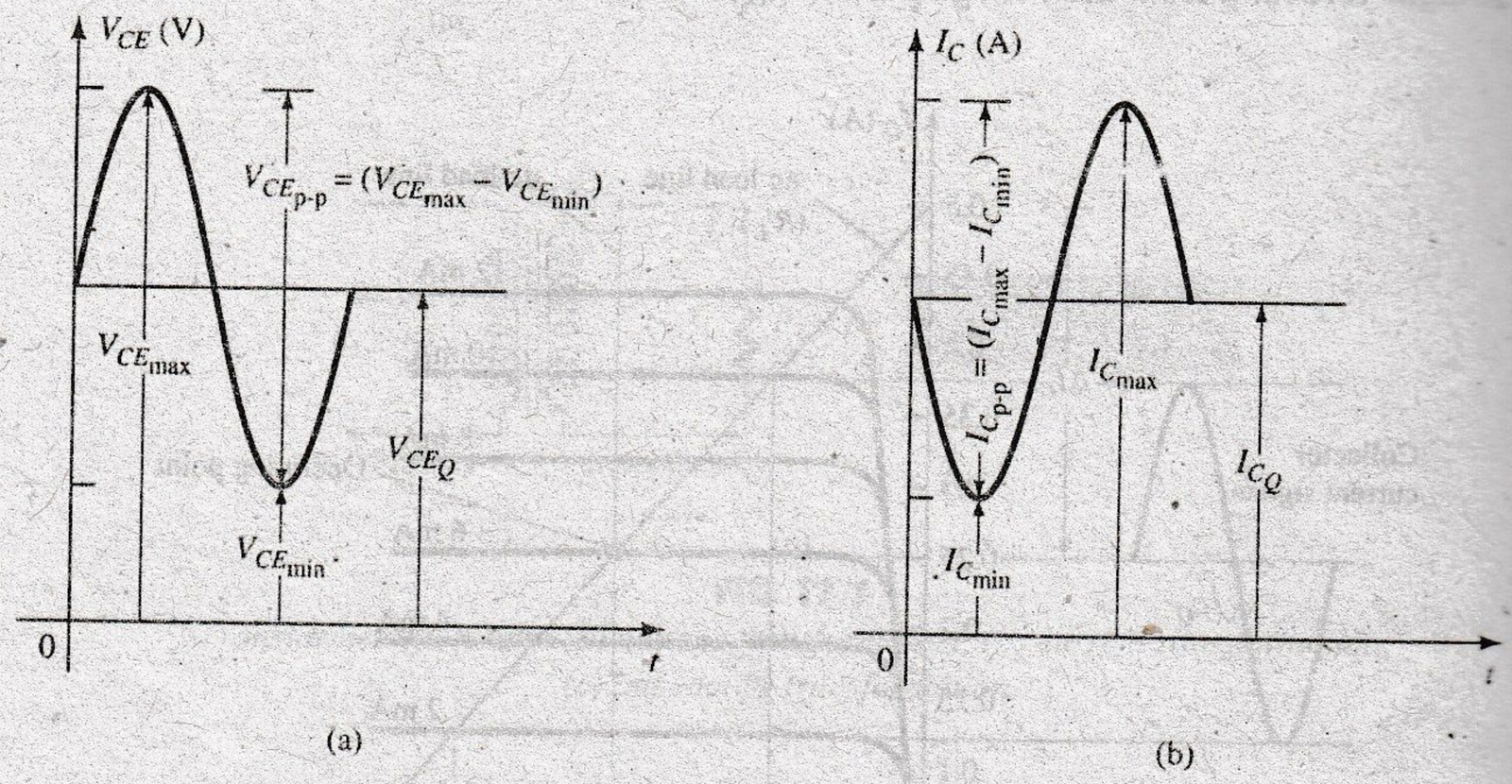


FIG. 12.9
Graphical operation of transformer-coupled class A amplifier.

The ac power developed across the transformer primary can then be calculated using

$$P_o(\text{ac}) = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8} \tag{12.13}$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), we find that the power delivered by the secondary to the load is approximately that calculated using Eq. (12.13). The output ac power can also be determined using the voltage delivered to the load.

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (12.9):

$$V_L = V_2 = \frac{N_2}{N_1}V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

and equals the power calculated using Eq. (12.5c).

Using Eq. (12.10) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2}I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms})R_L$$

EXAMPLE 12.4 Calculate the ac power delivered to the 8-Ω speaker for the circuit of Fig. 12.10. The circuit component values result in a dc base current of 6 mA, and the input signal (V_i) results in a peak base current swing of 4 mA.

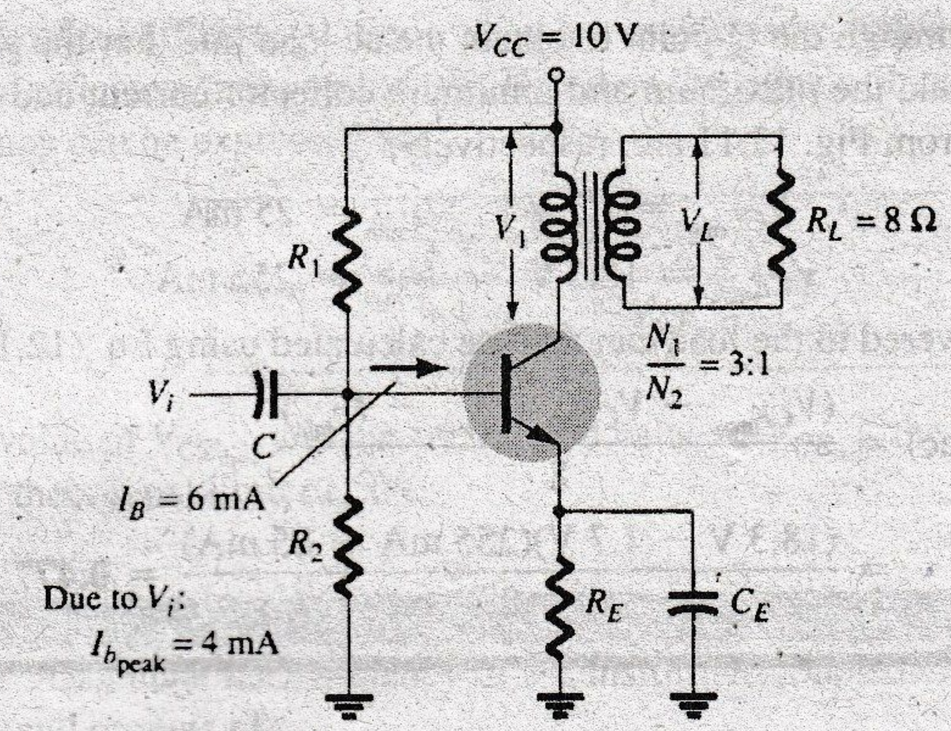


FIG. 12.10
Transformer-coupled class A amplifier for Example 12.4.

Solution: The dc load line is drawn vertically (see Fig. 12.11) from the voltage point:

$$V_{CE_Q} = V_{CC} = 10\text{ V}$$

For $I_B = 6$ mA, the operating point on Fig. 12.11 is

$$V_{CE_Q} = 10\text{ V} \quad \text{and} \quad I_{C_Q} = 140\text{ mA}$$

The effective ac resistance seen at the primary is

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = (3)^2(8) = 72\ \Omega$$

The ac load line can then be drawn of slope $-1/72$ going through the indicated operating point. To help draw the load line, consider the following procedure. For a current swing of

$$I_C = \frac{V_{CE}}{R'_L} = \frac{10\text{ V}}{72\ \Omega} = 139\text{ mA}$$

mark a point A:

$$I_{CE_Q} + I_C = 140\text{ mA} + 139\text{ mA} = 279\text{ mA along the } y\text{-axis}$$

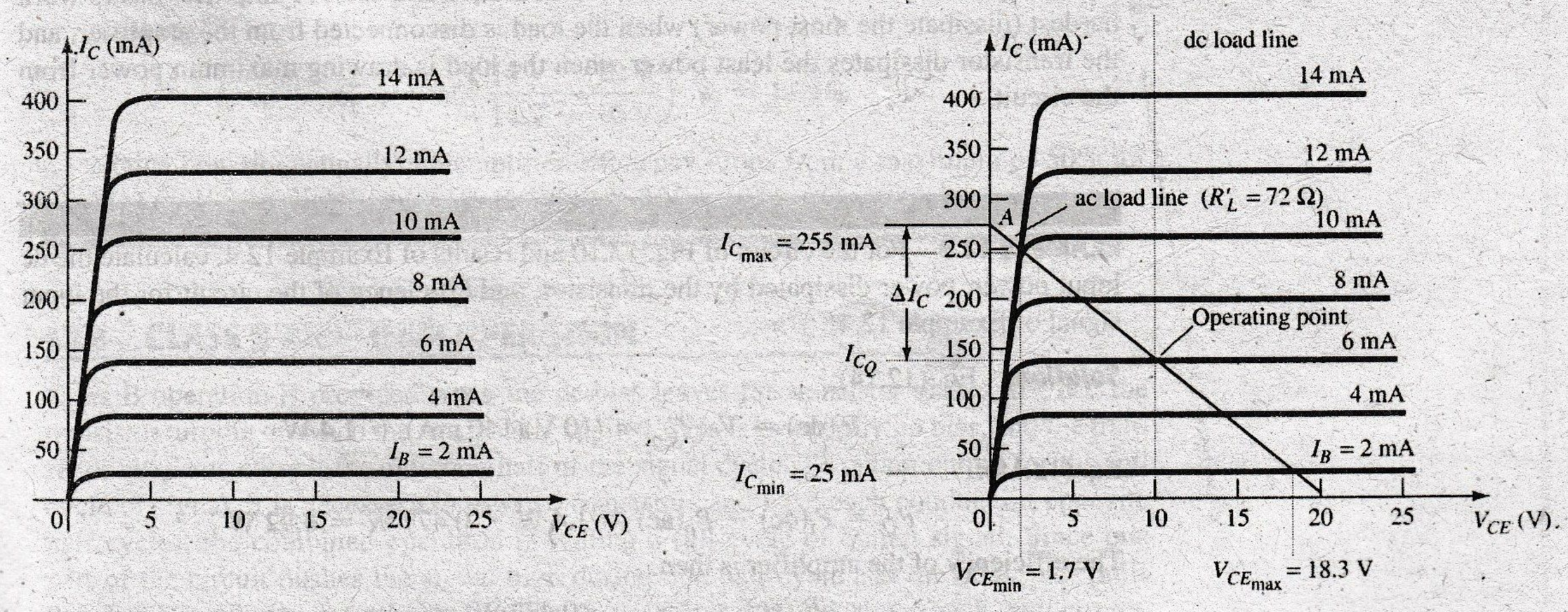


FIG. 12.11
Transformer-coupled class A transistor characteristic for Examples 12.4 and 12.5: (a) device characteristic; (b) dc and ac load lines.

Connect point A through the Q-point to obtain the ac load line. For the given base current swing of 4 mA peak, the maximum and minimum collector current and collector–emitter voltage obtained from Fig. 12.11 are, respectively,

$$V_{CE_{min}} = 1.7\text{ V} \qquad I_{C_{min}} = 25\text{ mA}$$
$$V_{CE_{max}} = 18.3\text{ V} \qquad I_{C_{max}} = 255\text{ mA}$$

The ac power delivered to the load can then be calculated using Eq. (12.13):

$$P_o(\text{ac}) = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8}$$
$$= \frac{(18.3\text{ V} - 1.7\text{ V})(255\text{ mA} - 25\text{ mA})}{8} = \mathbf{0.477\text{ W}}$$

Efficiency

So far we have considered calculating the ac power delivered to the load. We next consider the input power from the battery, power losses in the amplifier, and the overall power efficiency of the transformer-coupled class A amplifier.

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$\boxed{P_i(\text{dc}) = V_{CC}I_{C_Q}} \qquad \textbf{(12.14)}$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$\boxed{P_Q = P_i(\text{dc}) - P_o(\text{ac})} \qquad \textbf{(12.15)}$$

where P_Q is the power dissipated as heat. Although the equation is simple, it is nevertheless significant when operating a class A amplifier. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates the least power when the load is drawing maximum power from the circuit.

EXAMPLE 12.5 For the circuit of Fig. 12.10 and results of Example 12.4, calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 12.4.

Solution: Eq. (12.14):

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (10\text{ V})(140\text{ mA}) = \mathbf{1.4\text{ W}}$$

Eq. (12.15):

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4\text{ W} - 0.477\text{ W} = \mathbf{0.92\text{ W}}$$

The efficiency of the amplifier is then

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477\text{ W}}{1.4\text{ W}} \times 100\% = \mathbf{34.1\%}$$

Maximum Theoretical Efficiency For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\%\,\eta = 50\left(\frac{V_{CE_{max}} - V_{CE_{min}}}{V_{CE_{max}} + V_{CE_{min}}}\right)^2 \% \qquad \textbf{(12.16)}$$

The larger the value of $V_{CE_{max}}$ and the smaller the value of $V_{CE_{min}}$, the closer the efficiency approaches the theoretical limit of 50%.

EXAMPLE 12.6 Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

a. $V(\text{p}) = 12\text{ V}$.
b. $V(\text{p}) = 6\text{ V}$.
c. $V(\text{p}) = 2\text{ V}$.

Solution:

a. Since $V_{CE_Q} = V_{CC} = 12\text{ V}$, the maximum and minimum of the voltage swing are, respectively,

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 12\text{ V} = 24\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 12\text{ V} = 0\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{24\text{ V} - 0\text{ V}}{24\text{ V} + 0\text{ V}}\right)^2 \% = \mathbf{50\%}$$

b.

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 6\text{ V} = 18\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 6\text{ V} = 6\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{18\text{ V} - 6\text{ V}}{18\text{ V} + 6\text{ V}}\right)^2 \% = \mathbf{12.5\%}$$

c.

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 2\text{ V} = 14\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 2\text{ V} = 10\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{14\text{ V} - 10\text{ V}}{14\text{ V} + 10\text{ V}}\right)^2 \% = \mathbf{1.39\%}$$

Notice how dramatically the amplifier efficiency drops from a maximum of 50% for $V(\text{p}) = V_{CC}$ to slightly over 1% for $V(\text{p}) = 2\text{ V}$.

12.4 CLASS B AMPLIFIER OPERATION

Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. This is essentially no bias, and the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push–pull circuit*. Figure 12.12 shows a diagram for push–pull operation. An ac input signal is applied to the push–pull circuit, with each half operating on alternate half-cycles, the load then

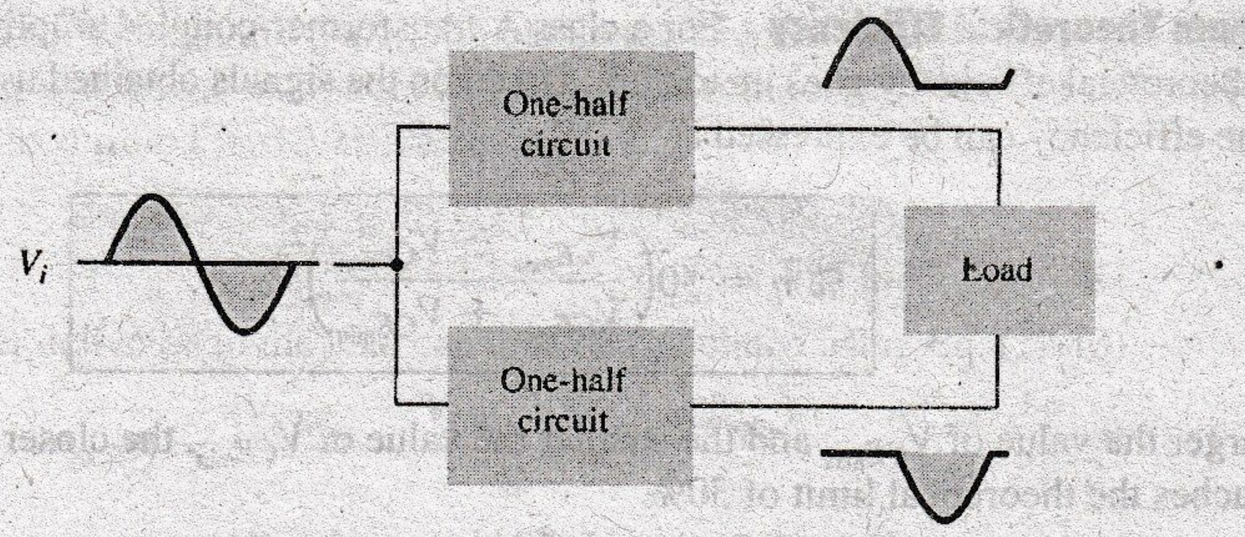


FIG. 12.12
Block representation of push–pull operation.

receiving a signal for the full ac cycle. The power transistors used in the push–pull circuit are capable of delivering the desired power to the load, and the class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; see Fig. 12.13) that provides the input or dc power. The amount of this input power can be calculated using

$$\boxed{P_i(\text{dc}) = V_{CC}I_{\text{dc}}} \tag{12.17}$$

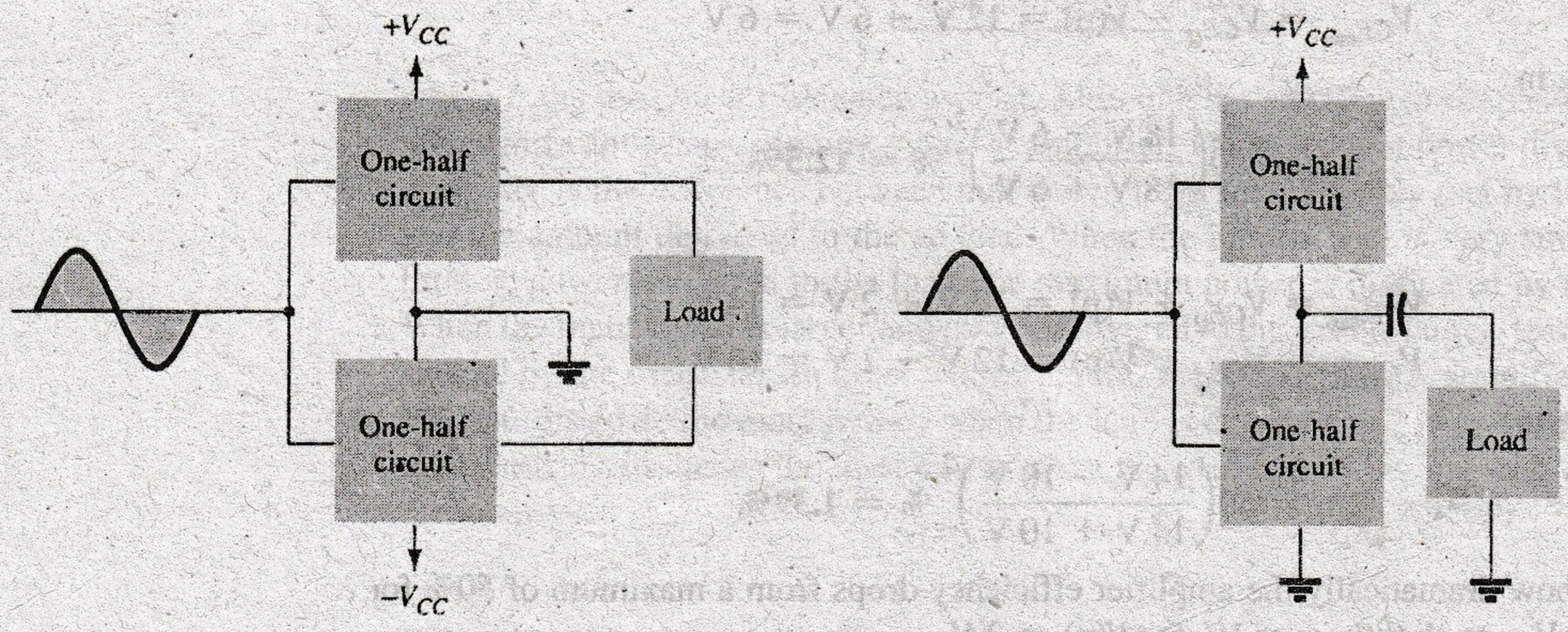


FIG. 12.13
Connection of push–pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.

where I_{dc} is the average or dc current drawn from the power supplies. In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, whereas that drawn from two power supplies has the form of a half-wave rectified signal from each supply. In either case, the value of the average current drawn can be expressed as

$$\boxed{I_{\text{dc}} = \frac{2}{\pi}I(\text{p})} \tag{12.18}$$

where $I(\text{p})$ is the peak value of the output current waveform. Using Eq. (12.18) in the power input equation (12.17) results in

$$\boxed{P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi}I(\text{p})\right)} \qquad \textbf{(12.19)}$$

Output (AC) Power

The power delivered to the load (usually referred to as a resistance R_L) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$\boxed{P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L}} \qquad \textbf{(12.20)}$$

If one is using an oscilloscope, the measured peak or peak-to-peak output voltage can be used:

$$\boxed{P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L}} \qquad \textbf{(12.21)}$$

The larger the rms or peak output voltage, the larger is the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Using Eqs. (12.19) and (12.21) in the efficiency equation above results in

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4}\frac{V_L(\text{p})}{V_{CC}} \times 100\% \qquad \textbf{(12.22)}$$

[using $I(\text{p}) = V_L(\text{p})/R_L$]. Equation (12.22) shows that the larger the peak voltage, the higher is the circuit efficiency, up to a maximum value when $V_L(\text{p}) = V_{CC}$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power Dissipated by Output Transistors The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

$$P_{2Q} = P_i(\text{dc}) - P_o(\text{ac}) \qquad \textbf{(12.23)}$$

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \qquad \textbf{(12.24)}$$

EXAMPLE 12.7 For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of $V_{CC} = 30$ V, determine the input power, output power, and circuit efficiency.

Solution: A 20-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{20\text{ V}}{16\ \Omega} = 1.25\text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2}{\pi}(1.25\text{ A}) = 0.796\text{ A}$$

and the input power delivered by the supply voltage is

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = (30\text{ V})(0.796\text{ A}) = \mathbf{23.9\text{ W}}$$

The output power delivered to the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(20\text{ V})^2}{2(16\ \Omega)} = \mathbf{12.5\text{ W}}$$

for a resulting efficiency of

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{12.5\text{ W}}{23.9\text{ W}} \times 100\% = \mathbf{52.3\%}$$

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when $V_L(\text{p}) = V_{CC}$:

$$\boxed{\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}} \qquad \textbf{(12.25)}$$

The corresponding peak ac current $I(\text{p})$ is then

$$I(\text{p}) = \frac{V_{CC}}{R_L}$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{\text{dc}} = \frac{2}{\pi} I(\text{p}) = \frac{2V_{CC}}{\pi R_L}$$

Using this current to calculate the maximum value of input power results in

$$\boxed{\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{\text{dc}}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}} \qquad \textbf{(12.26)}$$

The maximum circuit efficiency for class B operation is then

$$\text{maximum } \%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\%$$

$$= \frac{\pi}{4} \times 100\% = \mathbf{78.54\%} \qquad \textbf{(12.27)}$$

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(\text{p}) = 0.636V_{CC} \qquad \left(= \frac{2}{\pi} V_{CC}\right)$$

for a maximum transistor power dissipation of

$$\boxed{\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}} \qquad \textbf{(12.28)}$$

EXAMPLE 12.8 For a class B amplifier using a supply of $V_{CC} = 30$ V and driving a load of 16 Ω, determine the maximum input power, output power, and transistor dissipation.

Solution: The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{2(16\ \Omega)} = \mathbf{28.125\ W}$$

The maximum input power drawn from the voltage supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30\text{ V})^2}{\pi(16\ \Omega)} = \mathbf{35.81\ W}$$

The circuit efficiency is then

$$\text{maximum } \%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125\text{ W}}{35.81\text{ W}} \times 100\% = 78.54\%$$

as expected. The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30\text{ V})^2}{\pi^2 16\ \Omega}\right] = \mathbf{5.7\ W}$$

Under maximum conditions a pair of transistors each handling 5.7 W at most can deliver 28.125 W to a 16-Ω load while drawing 35.81 W from the supply.

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L}$$

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = V_{CC}\left[\frac{2V_L(\text{p})}{\pi R_L}\right]$$

so that

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)(V_L(\text{p})/R_L)]} \times 100\%$$

$$\%\,\eta = 78.54\frac{V_L(\text{p})}{V_{CC}}\% \qquad \textbf{(12.29)}$$

EXAMPLE 12.9 Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 24$ V with peak output voltages of:

a. $V_L(\text{p}) = 22$ V.
b. $V_L(\text{p}) = 6$ V.

Solution: Using Eq. (12.29) gives

a. $\%\,\eta = 78.54\dfrac{V_L(\text{p})}{V_{CC}}\% = 78.54\left(\dfrac{22\text{ V}}{24\text{ V}}\right) = \mathbf{72\%}$

b. $\%\,\eta = 78.54\left(\dfrac{6\text{ V}}{24\text{ V}}\right)\% = \mathbf{19.6\%}$

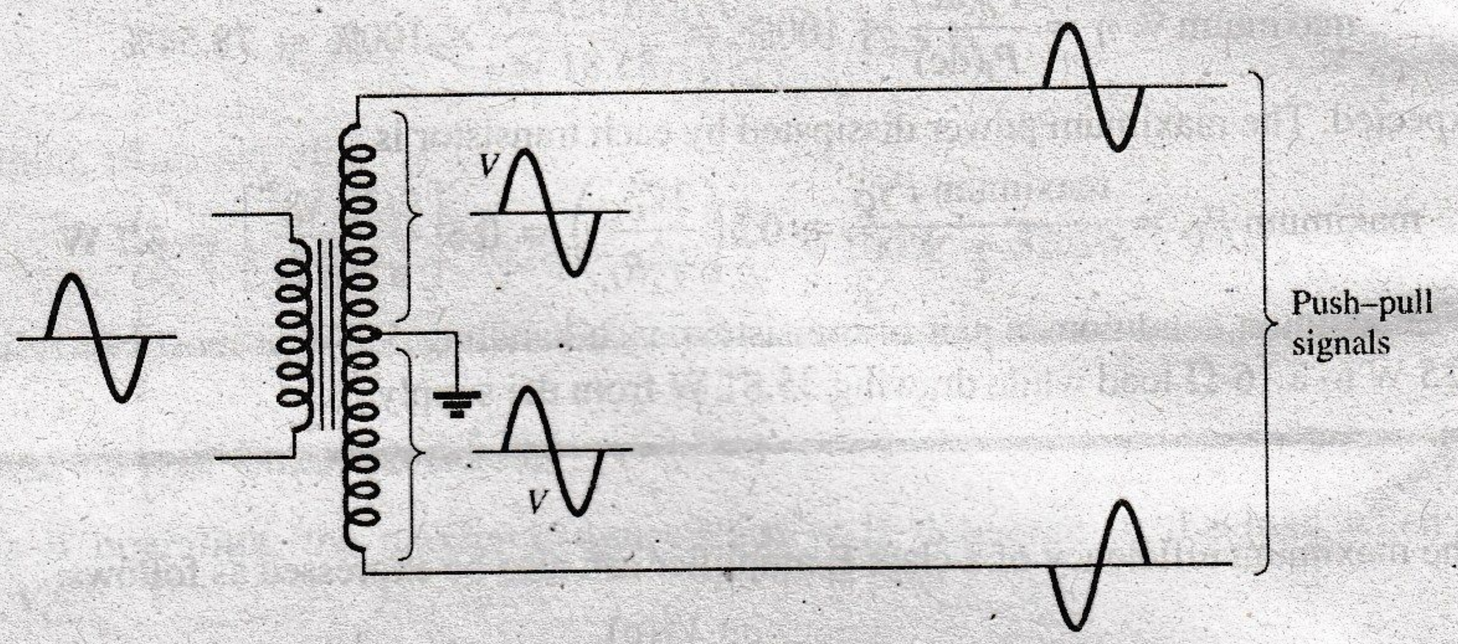
Notice that a voltage near the maximum [22 V in part (a)] results in an efficiency near the maximum, whereas a small voltage swing [6 V in part (b)] still provides an efficiency near 20%. Similar power supply and signal swings would have resulted in much poorer efficiency in a class A amplifier.

12.5 CLASS B AMPLIFIER CIRCUITS

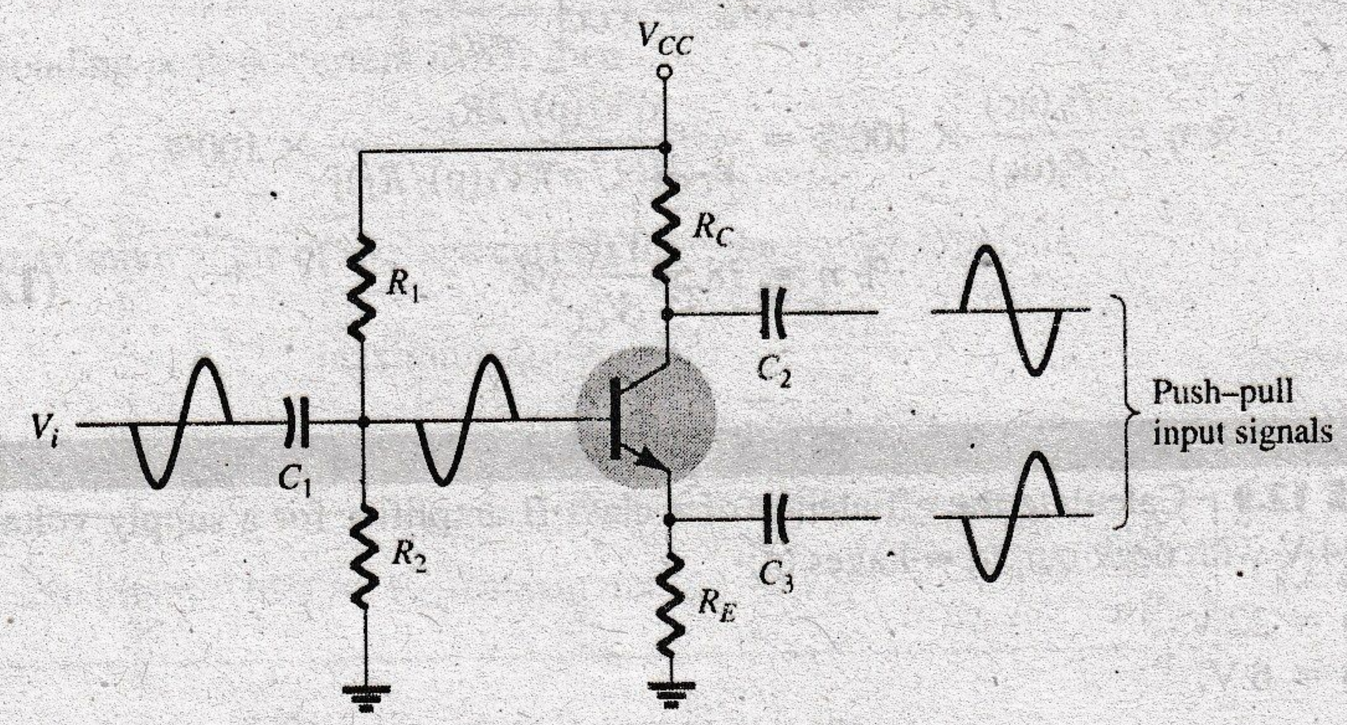
A number of circuit arrangements for obtaining class B operation are possible. We will consider the advantages and disadvantages of a number of the more popular circuits in this section. The input signals to the amplifier could be a single signal, the circuit then

providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite-polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, and the transformer-coupled amplifier has been very popular for a long time. Opposite-polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite-polarity signals. An opposite-polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *n*MOS and *p*MOS).

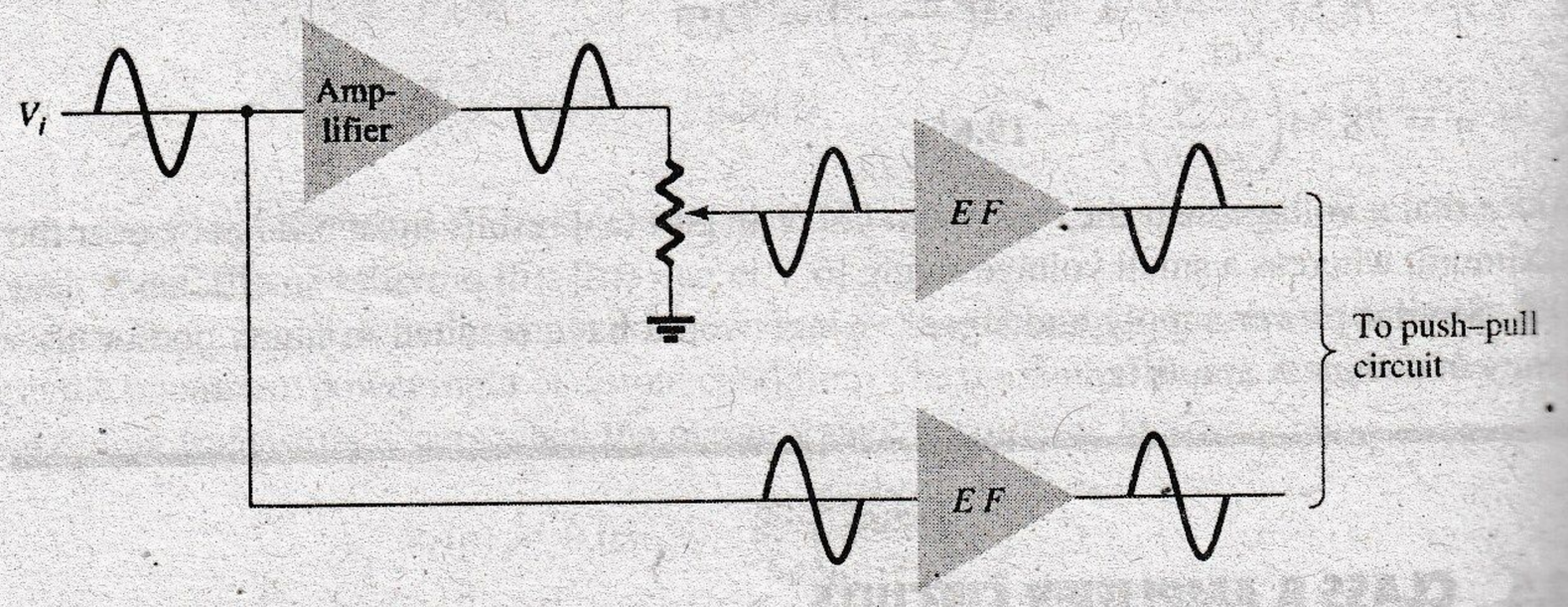
Figure 12.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 12.14a shows a center-tapped transformer to provide opposite-phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite



(a)



(b)



(c)

FIG. 12.14
Phase-splitter circuits.

in phase and of the same magnitude. The circuit of Fig. 12.14b uses a BJT stage with in-phase output from the emitter and opposite-phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a noninverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

Transformer-Coupled Push–Pull Circuits

The circuit of Fig. 12.15 uses a center-tapped input transformer to produce opposite-polarity signals to the two transistor inputs and an output transformer to drive the load in a push–pull mode of operation described next.

During the first half-cycle of operation, transistor Q_1 is driven into conduction, whereas transistor Q_2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q_2 conducts, whereas Q_1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.

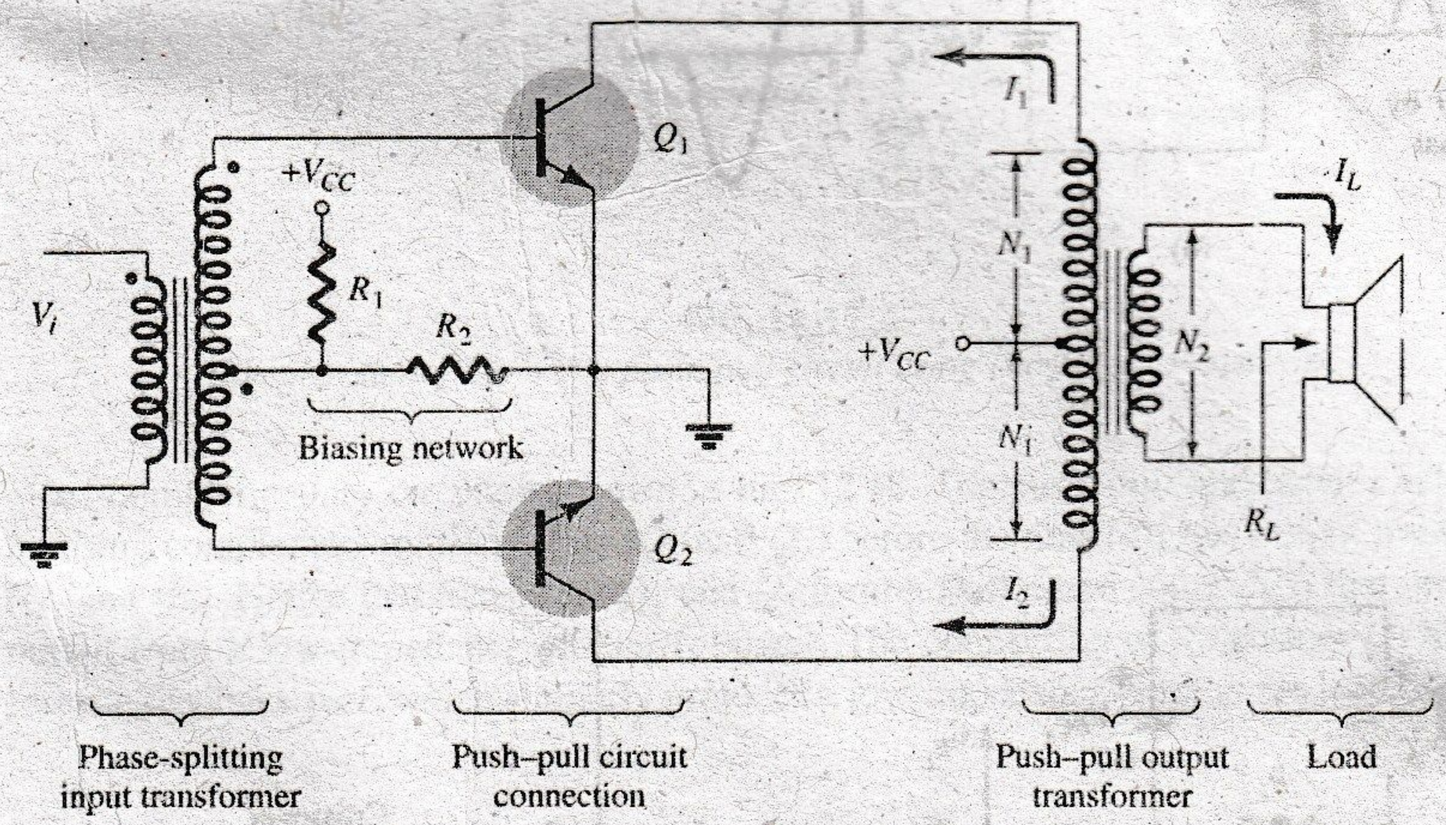
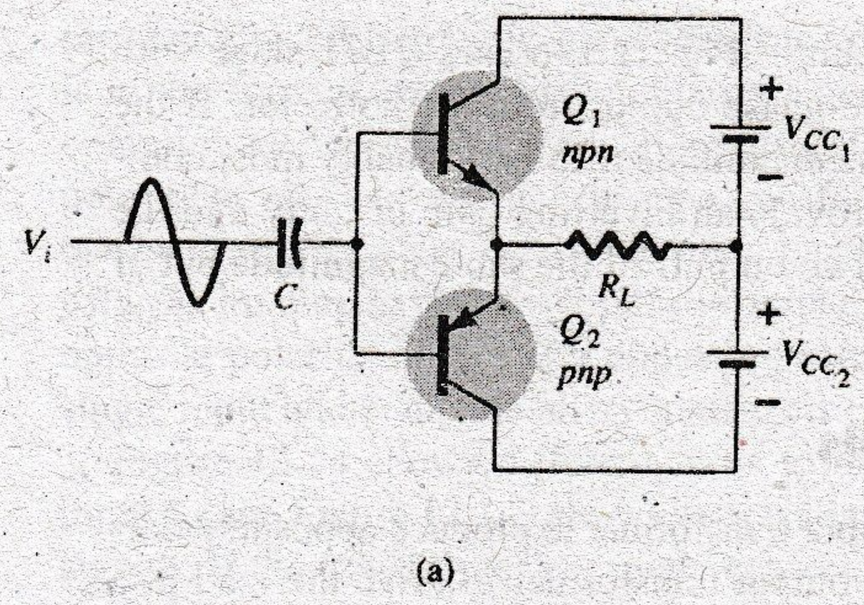


FIG. 12.15
Push–pull circuit.

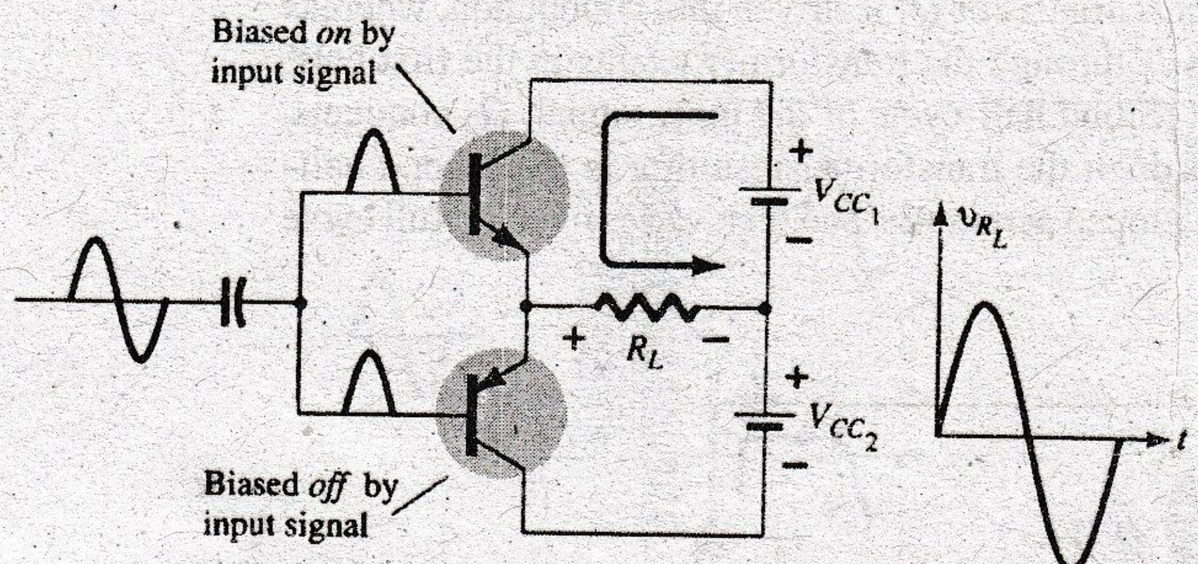
Complementary-Symmetry Circuits

Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 12.16a. Whereas a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 12.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 12.16c.

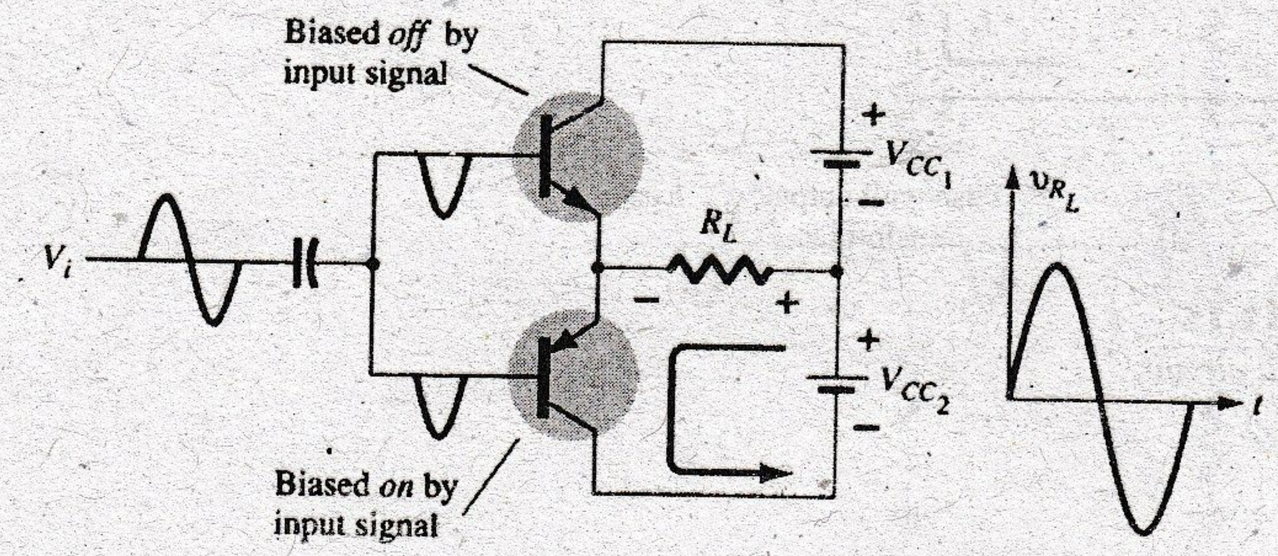
During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 12.16d). *Crossover distortion* refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off so that the output voltage does not follow the input around the zero-voltage condition. Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.



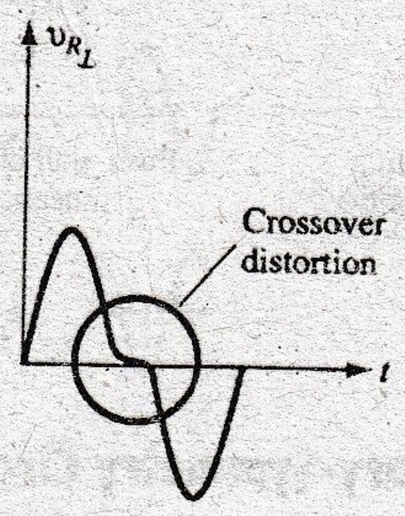
(a)



(b)



(c)



(d)

FIG. 12.16
Complementary-symmetry push–pull circuit.

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 12.17. Note that the load is driven as the output of an emitter-follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-connected transistors to provide higher output current and lower output resistance.

Quasi-Complementary Push-Pull Amplifier

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push–pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same matched *npn* transistors for the output is provided by a

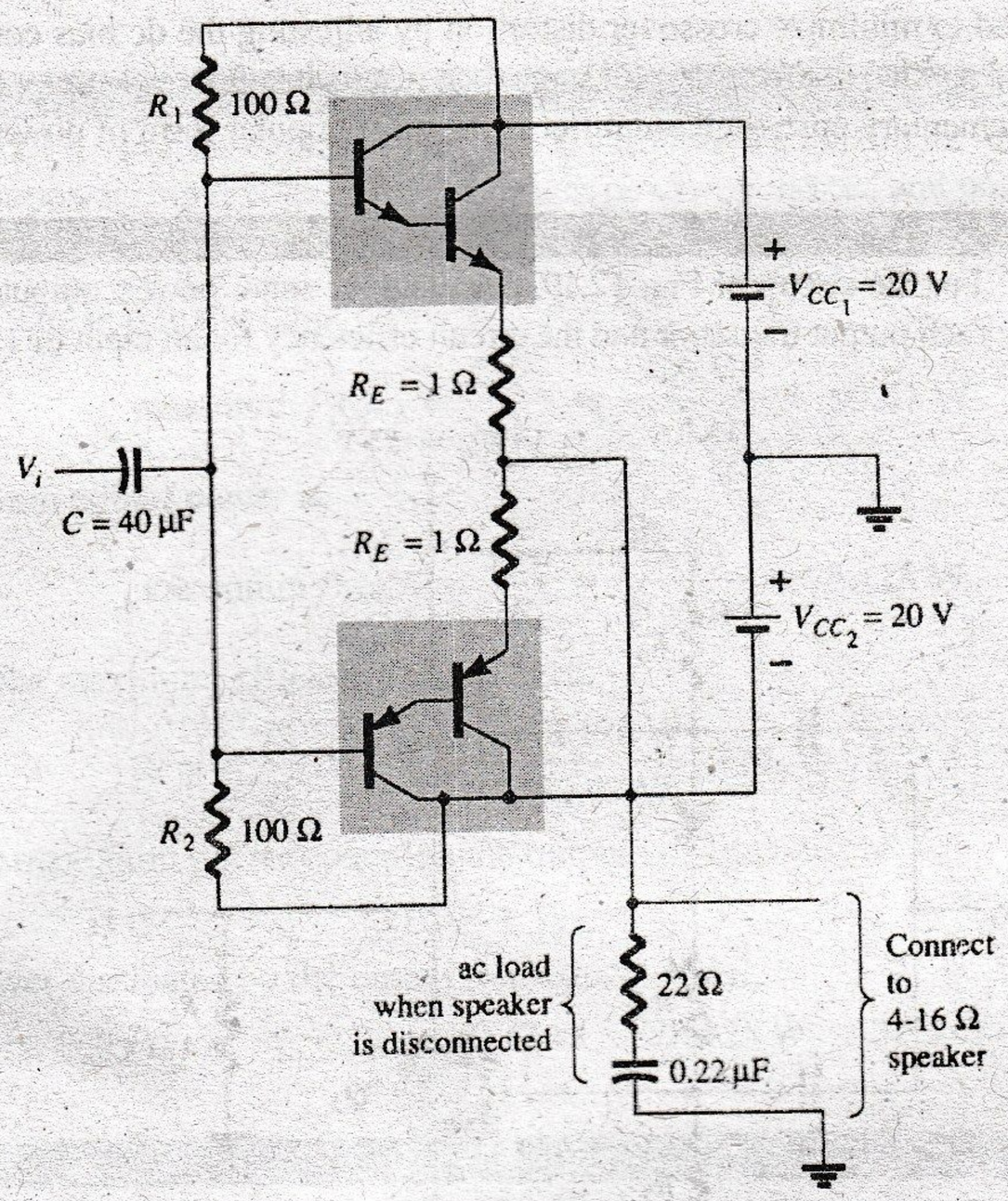


FIG. 12.17
Complementary-symmetry push–pull circuit using Darlington transistors.

quasi-complementary circuit, as shown in Fig. 12.18. The push–pull operation is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor

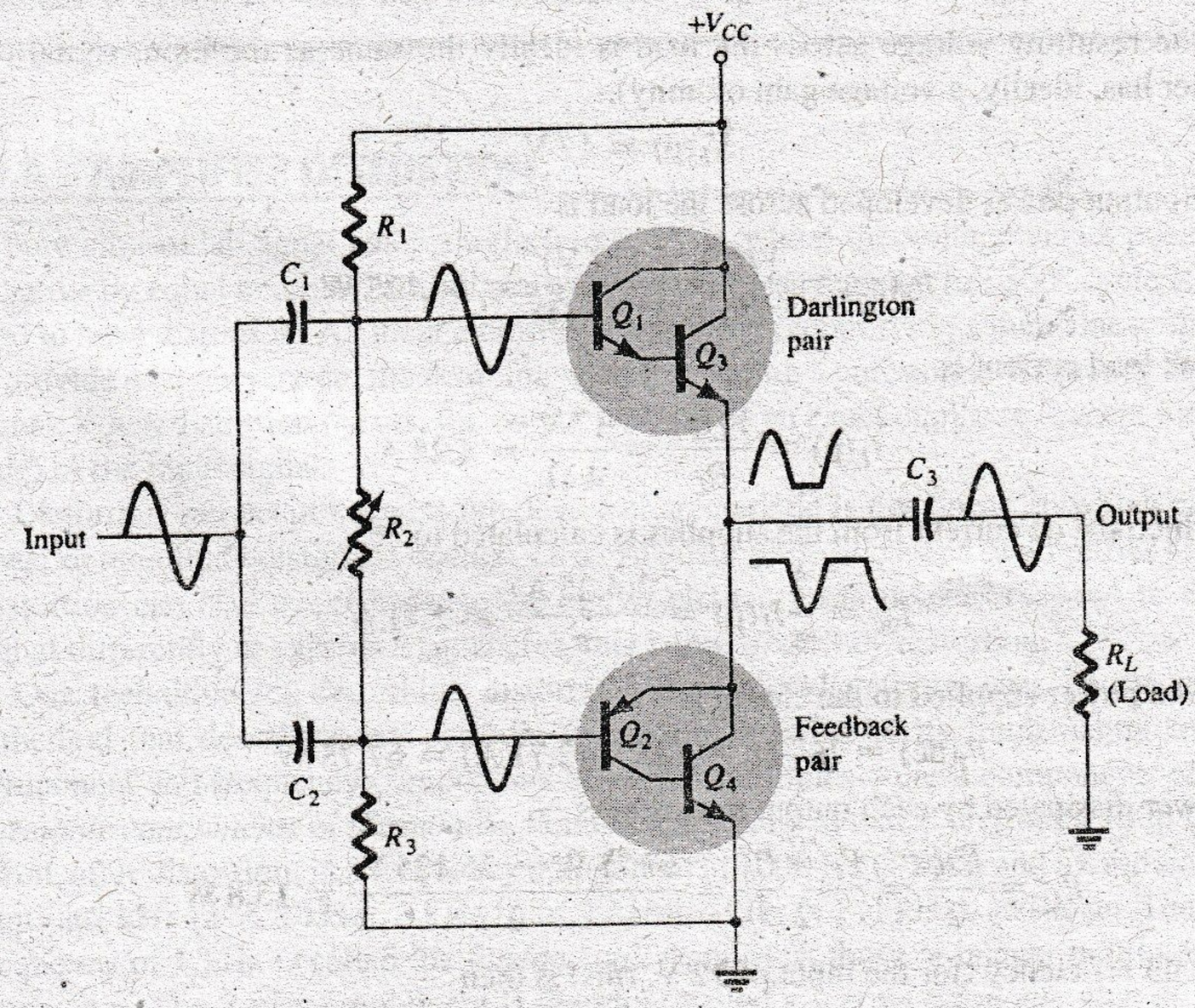


FIG. 12.18
Quasi-complementary push–pull transformerless power amplifier.

R_2 can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push–pull stage then results in a full cycle output to the load. The quasi-complementary push–pull amplifier is the most popular form of power amplifier.

EXAMPLE 12.10 For the circuit of Fig. 12.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.

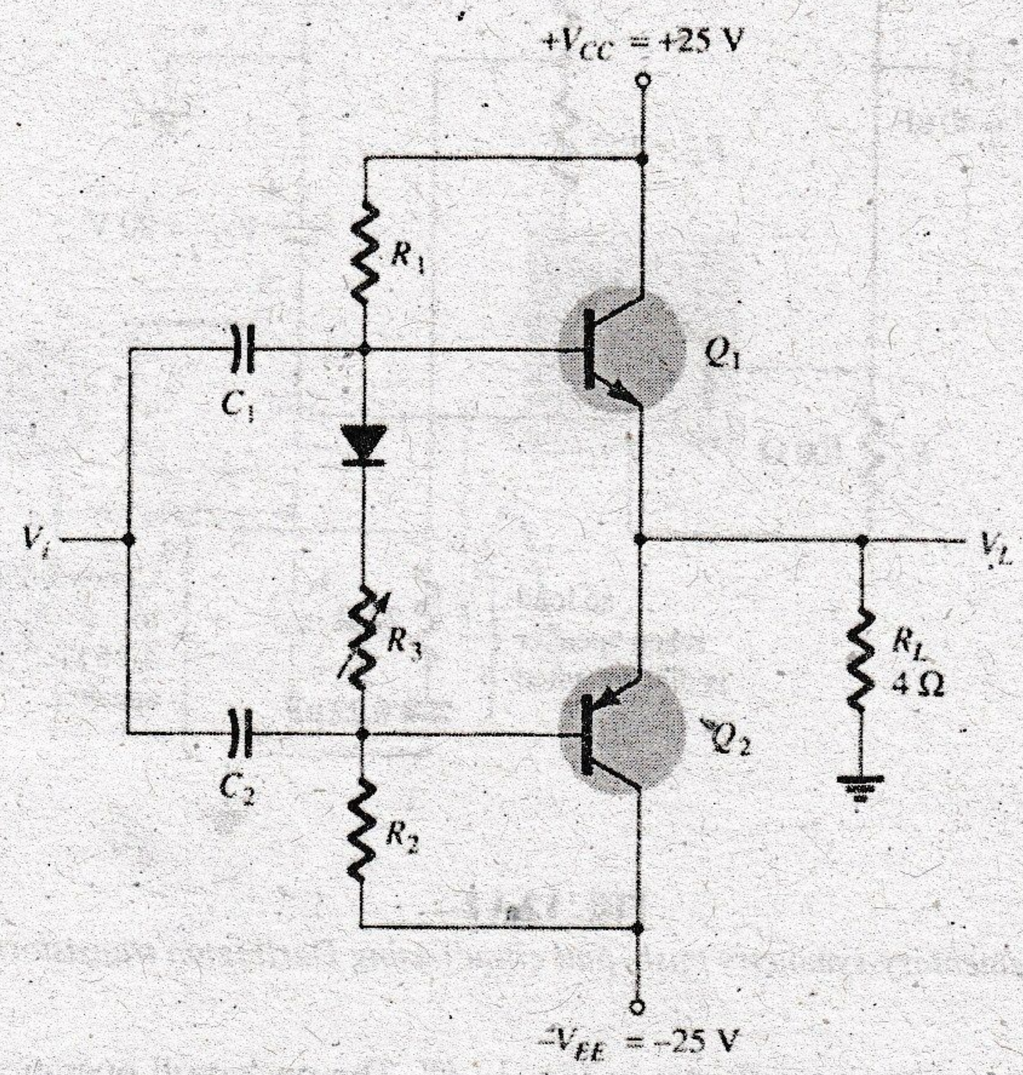


FIG. 12.19
Class B power amplifier for Examples 12.10 to 12.12.

Solution: The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\,V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(\text{p}) = 17\text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = \mathbf{36.125\text{ W}}$$

The peak load current is

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\ \Omega} = 4.25\text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = (25\text{ V})(2.71\text{ A}) = \mathbf{67.75\text{ W}}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\text{ W} - 36.125\text{ W}}{2} = \mathbf{15.8\text{ W}}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125\text{ W}}{67.75\text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 12.11 For the circuit of Fig. 12.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and power dissipated by the output transistors at this voltage.

Solution: The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25\text{ V})^2}{\pi 4\ \Omega} = \mathbf{99.47\ W}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25\text{ V})^2}{2(4\ \Omega)} = \mathbf{78.125\ W}$$

[Note that the maximum efficiency is achieved:

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125\text{ W}}{99.47\text{ W}}100\% = 78.54\%]$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25\text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47\text{ W} - 78.125\text{ W} = \mathbf{21.3\ W}$$

EXAMPLE 12.12 For the circuit of Fig. 12.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution: The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25\text{ V})^2}{\pi^2 4\ \Omega} = \mathbf{31.66\ W}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(\text{p}) = 0.636(25\text{ V}) = \mathbf{15.9\ V}$$

(Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, whereas at $V_L = 25$ V they only had to dissipate 21.3 W.)

12.6 AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs, the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics*. For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz (2 × 1 kHz), 3 kHz (3 × 1 kHz), 4 kHz (4 × 1 kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency*; those at integer multiples are the *harmonics*. The 2-kHz component is therefore called a *second harmonic*, that at 3 kHz is the *third harmonic*, and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude A_1 and the nth frequency component has an amplitude A_n, a harmonic distortion can be defined as

$$\% \, n\text{th harmonic distortion} = \% \, D_n = \frac{|A_n|}{|A_1|} \times 100\% \tag{12.30}$$

The fundamental component is typically larger than any harmonic component.

EXAMPLE 12.13 Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution: Using Eq. (12.30) yields

$$\% \, D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{10\%}$$

$$\% \, D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{4\%}$$

$$\% \, D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{2\%}$$

Total Harmonic Distortion When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\% \text{ THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\% \tag{12.31}$$

where THD is total harmonic distortion.

EXAMPLE 12.14 Calculate the total harmonic distortion for the amplitude components given in Example 12.13.

Solution: Using the computed values of $D_2 = 0.10$, $D_3 = 0.04$, and $D_4 = 0.02$ in Eq. (12.31), we obtain

$$\begin{aligned} \% \text{ THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= \mathbf{10.95\%} \end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

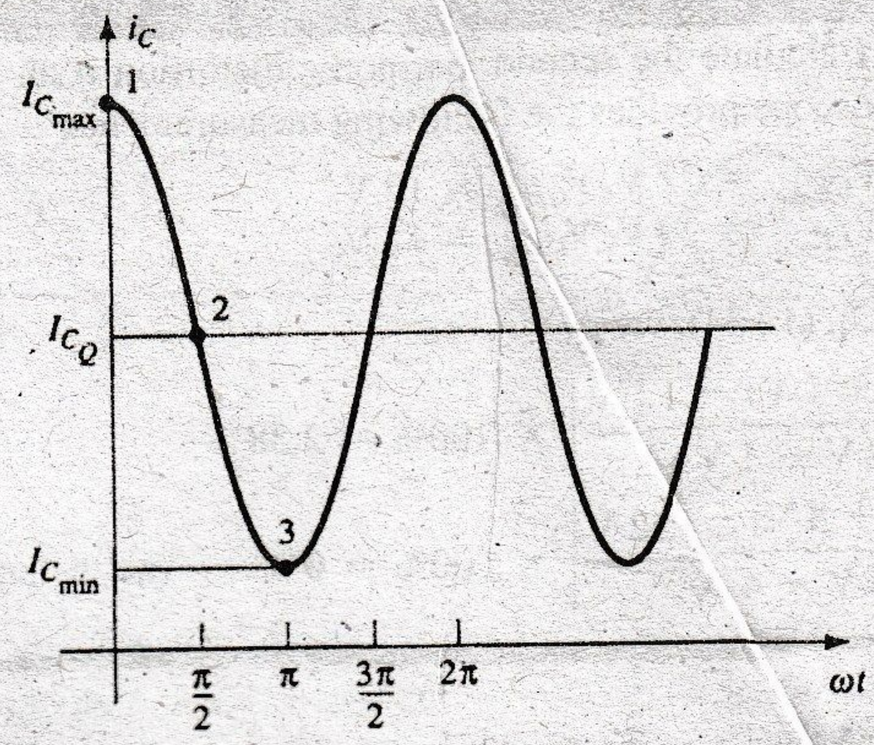


FIG. 12.20
Waveform for obtaining second harmonic distortion.

Second Harmonic Distortion Figure 12.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The signal shown indicates that some distortion is present. An equation that approximately describes the distorted signal waveform is

$$i_C \approx I_{C_Q} + I_0 + I_1 \cos \omega t + I_2 \cos \omega t \tag{12.32}$$

The current waveform contains the original quiescent current I_{C_Q}, which occurs with zero input signal; an additional dc current I_0, due to the nonzero average of the distorted signal; the fundamental component of the distorted ac signal I_1; and a second harmonic component I_2, at twice the fundamental frequency. Although other harmonics are also present, only the second is considered here. Equating the resulting current from Eq. (12.32) at a few points in the cycle to that shown on the current waveform provides the following three relations:

At point 1 ($\omega t = 0$),

$$i_C = I_{C_{max}} = I_{C_Q} + I_0 + I_1 \cos 0 + I_2 \cos 0$$
$$I_{C_{max}} = I_{C_Q} + I_0 + I_1 + I_2$$

At point 2 ($\omega t = \pi/2$),

$$i_C = I_{C_Q} = I_{C_Q} + I_0 + I_1 \cos \frac{\pi}{2} + I_2 \cos \frac{2\pi}{2}$$
$$I_{C_Q} = I_{C_Q} + I_0 - I_2$$

At point 3 ($\omega t = \pi$),

$$i_C = I_{C_{min}} = I_{C_Q} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$
$$I_{C_{min}} = I_{C_Q} + I_0 - I_1 + I_2$$

Solving the preceding three equations simultaneously gives the following results:

$$I_0 = I_2 = \frac{I_{C_{max}} + I_{C_{min}} - 2I_{C_Q}}{4}, \qquad I_1 = \frac{I_{C_{max}} - I_{C_{min}}}{2}$$

Referring to Eq. (12.30), we can express the definition of second harmonic distortion as

$$D_2 = \left|\frac{I_2}{I_1}\right| \times 100\%$$

Inserting the values of I_1 and I_2 determined above gives

$$D_2 = \left|\frac{\frac{1}{2}(I_{C_{max}} + I_{C_{min}}) - I_{C_Q}}{I_{C_{max}} - I_{C_{min}}}\right| \times 100\% \tag{12.33}$$

In a similar manner, the second harmonic distortion can be expressed in terms of measured collector–emitter voltages:

$$D_2 = \left|\frac{\frac{1}{2}(V_{CE_{max}} + V_{CE_{min}}) - V_{CE_Q}}{V_{CE_{max}} - V_{CE_{min}}}\right| \times 100\% \tag{12.34}$$

EXAMPLE 12.15 Calculate the second harmonic distortion if an output waveform displayed on an oscilloscope provides the following measurements:

a. $V_{CE_{min}} = 1\text{ V}$, $V_{CE_{max}} = 22\text{ V}$, $V_{CE_Q} = 12\text{ V}$.
b. $V_{CE_{min}} = 4\text{ V}$, $V_{CE_{max}} = 20\text{ V}$, $V_{CE_Q} = 12\text{ V}$.

Solution: Using Eq. (12.34), we get

a. $$D_2 = \left|\frac{\frac{1}{2}(22\text{ V} + 1\text{ V}) - 12\text{ V}}{22\text{ V} - 1\text{ V}}\right| \times 100\% = \mathbf{2.38\%}$$

b. $$D_2 = \left|\frac{\frac{1}{2}(20\text{ V} + 4\text{ V}) - 12\text{ V}}{20\text{ V} - 4\text{ V}}\right| \times 100\% = \mathbf{0\%} \qquad \text{(no distortion)}$$

Power of a Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor R_C due to the fundamental component of the distorted signal is

$$P_1 = \frac{I_1^2 R_C}{2} \tag{12.35}$$

The total power due to all the harmonic components of the distorted signal can then be calculated using

$$P = (I_1^2 + I_2^2 + I_3^2 + \cdots)\frac{R_C}{2} \tag{12.36}$$

The total power can also be expressed in terms of the total harmonic distortion,

$$P = (1 + D_2^2 + D_3^2 + \cdots)I_1^2\frac{R_C}{2} = (1 + \text{THD}^2)P_1 \tag{12.37}$$

EXAMPLE 12.16 For a harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$, and $D_4 = 0.01$, with $I_1 = 4\text{ A}$ and $R_C = 8\ \Omega$, calculate the total harmonic distortion, fundamental power component, and total power.

Solution: The total harmonic distortion is

$$\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.1)^2 + (0.02)^2 + (0.01)^2} \approx \mathbf{0.1}$$

The fundamental power, using Eq. (12.35), is

$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(4\text{ A})^2(8\ \Omega)}{2} = \mathbf{64\text{ W}}$$

The total power calculated using Eq. (12.37) is then

$$P = (1 + \text{THD}^2)P_1 = [1 + (0.1)^2]64 = (1.01)64 = \mathbf{64.64\text{ W}}$$

(Note that the total power is due mainly to the fundamental component even with 10% second harmonic distortion.)

Graphical Description of Harmonic Components of a Distorted Signal

A distorted waveform such as that which occurs in class B operation can be represented using Fourier analysis as a fundamental with harmonic components. Figure 12.21a shows a positive half-cycle such as the type that would result in one side of a class B amplifier. Using Fourier analysis techniques, we can obtain the fundamental component of the distorted signal as shown in Fig. 12.21b. Similarly, the second and third harmonic components can be obtained and are shown in Fig. 12.21c and d, respectively. Using the Fourier technique, we can construct the distorted waveform by adding the fundamental and harmonic components, as shown in Fig. 12.21e. In general, any periodic distorted waveform can be represented by adding a fundamental component and all harmonic components, each of varying amplitude and at various phase angles.

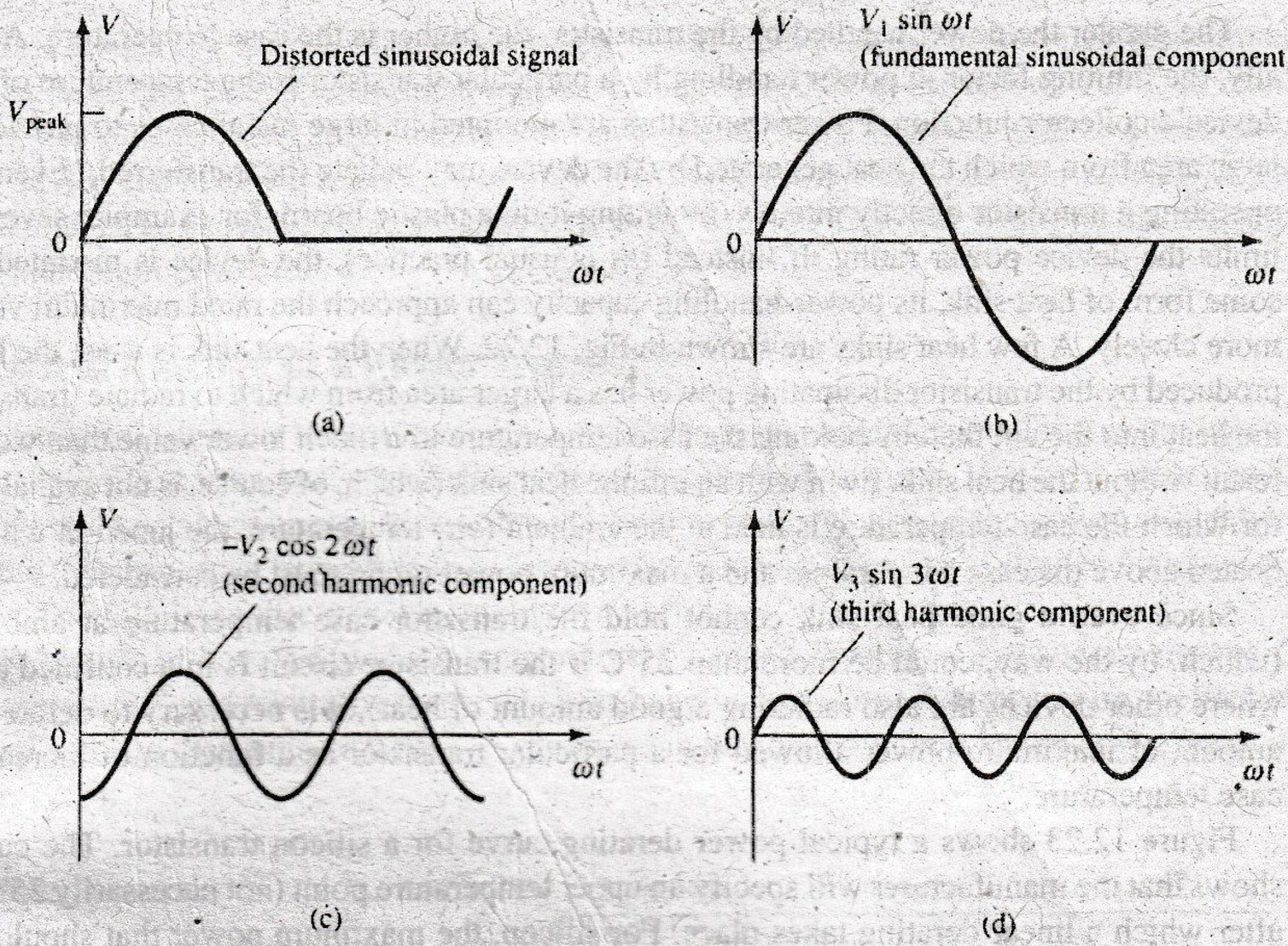


FIG. 12.21

Graphical representation of a distorted signal through the use of harmonic components.

12.7 POWER TRANSISTOR HEAT SINKING

Although integrated circuits are used for small-signal and low-power applications, most high-power applications still require individual power transistors. Improvements in production techniques have provided higher power ratings in small-sized packaging cases, have increased the maximum transistor breakdown voltage, and have provided faster-switching power transistors.

The maximum power handled by a particular device and the temperature of the transistor junctions are related since the power dissipated by the device causes an increase in temperature at the junction of the device. Obviously, a 100-W transistor will provide more power capability than a 10-W transistor. On the other hand, proper heat-sinking techniques will allow operation of a device at about one-half its maximum power rating.

Of the two types of bipolar transistors—germanium and silicon—silicon transistors provide greater maximum temperature ratings. Typically, the maximum junction temperature of these types of power transistors is as follows:

Silicon: 150–200°C
Germanium: 100–110°C

For many applications the average power dissipated may be approximated by

$$P_D = V_{CE} I_C \tag{12.38}$$

This power dissipation, however, is allowed only up to a maximum temperature. Above this temperature, the device power dissipation capacity must be reduced (or derated) so that at higher case temperatures the power-handling capacity is reduced, down to 0 W at the device maximum case temperature.

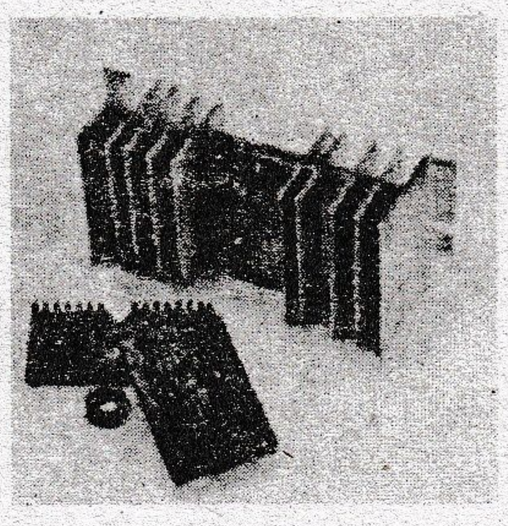


FIG. 12.22
Typical power heat sinks.

The greater the power handled by the transistor, the higher is the case temperature. Actually, the limiting factor in power handling by a particular transistor is the temperature of the device's collector junction. Power transistors are mounted in large metal cases to provide a large area from which the heat generated by the device may radiate (be transferred). Even so, operating a transistor directly into air (mounting it on a plastic board, for example) severely limits the device power rating. If, instead (as is usual practice), the device is mounted on some form of heat sink, its power-handling capacity can approach the rated maximum value more closely. A few heat sinks are shown in Fig. 12.22. When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temperature to a much lower value than would result without the heat sink. Even with an infinite heat sink (which, of course, is not available), for which the case temperature is held at the ambient (air) temperature, the junction will be heated above the case temperature and a maximum power rating must be considered.

Since even a good heat sink cannot hold the transistor case temperature at ambient (which, by the way, could be more than 25°C if the transistor circuit is in a confined area where other devices are also radiating a good amount of heat), it is necessary to derate the amount of maximum power allowed for a particular transistor as a function of increased case temperature.

Figure 12.23 shows a typical power derating curve for a silicon transistor. The curve shows that the manufacturer will specify an upper temperature point (not necessarily 25°C), after which a linear derating takes place. For silicon, the maximum power that should be handled by the device does not reduce to 0 W until the case temperature is 200°C.

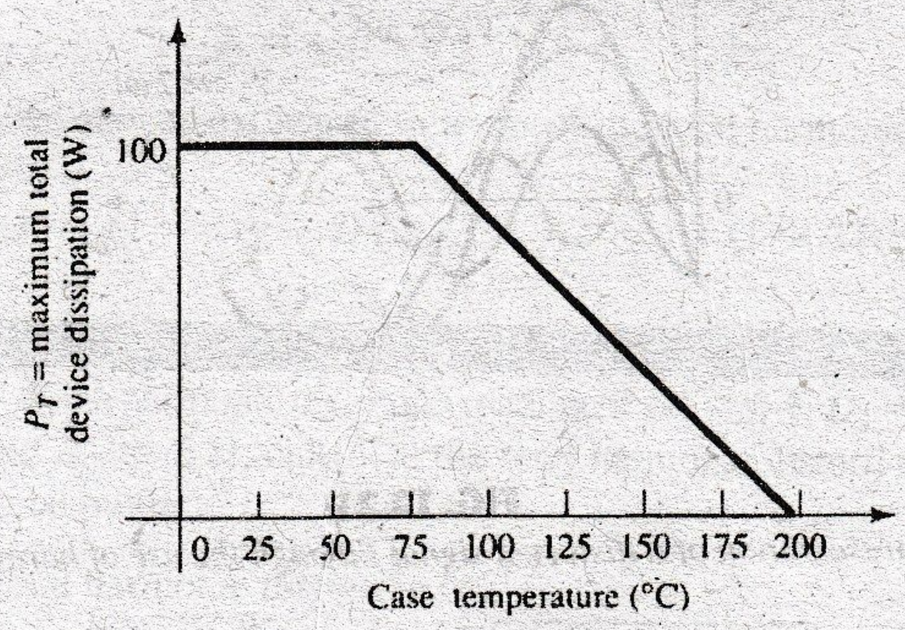


FIG. 12.23
Typical power derating curve for silicon transistors.

It is not necessary to provide a derating curve since the same information could be given simply as a listed derating factor on the device specification sheet. Stated mathematically, we have

$$P_D(\text{temp}_1) = P_D(\text{temp}_0) - (\text{Temp}_1 - \text{Temp}_0)(\text{derating factor}) \qquad \textbf{(12.39)}$$

where the value of Temp_0 is the temperature at which derating should begin, the value of Temp_1 is the particular temperature of interest (above the value Temp_0), $P_D(\text{temp}_0)$ and $P_D(\text{temp}_1)$ are the maximum power dissipations at the temperatures specified, and the derating factor is the value given by the manufacturer in units of watts (or milliwatts) per degree of temperature.

EXAMPLE 12.17 Determine what maximum dissipation will be allowed for an 80-W silicon transistor (rated at 25°C) if derating is required above 25°C by a derating factor of 0.5 W/°C at a case temperature of 125°C.

Solution:

$$P_D(125°\text{C}) = P_D(25°\text{C}) - (125°\text{C} - 25°\text{C})(0.5\ \text{W}/°\text{C})$$
$$= 80\ \text{W} - 100°\text{C}(0.5\ \text{W}/°\text{C}) = \mathbf{30\ W}$$

It is interesting to note what power rating results from using a power transistor without a heat sink. For example, a silicon transistor rated at 100 W at (or below) 100°C is rated only 4 W at (or below) 25°C, the free-air temperature. Thus, operated without a heat sink, the device can handle a maximum of only 4 W at the room temperature of 25°C. Using a heat sink large enough to hold the case temperature to 100°C at 100 W allows operating at the maximum power rating.

Thermal Analogy of a Power Transistor

Selection of a suitable heat sink requires a considerable amount of detail that is not appropriate to our present basic considerations of the power transistor. However, more detail about the thermal characteristics of the transistor and its relation to the power dissipation of the transistor may help provide a clearer understanding of power as limited by temperature. The following discussion should prove useful.

A picture of how the junction temperature T_J, case temperature T_C, and ambient (air) temperature T_A are related by the device heat-handling capacity—a temperature coefficient usually called thermal resistance—is presented in the thermal–electrical analogy shown in Fig. 12.24.

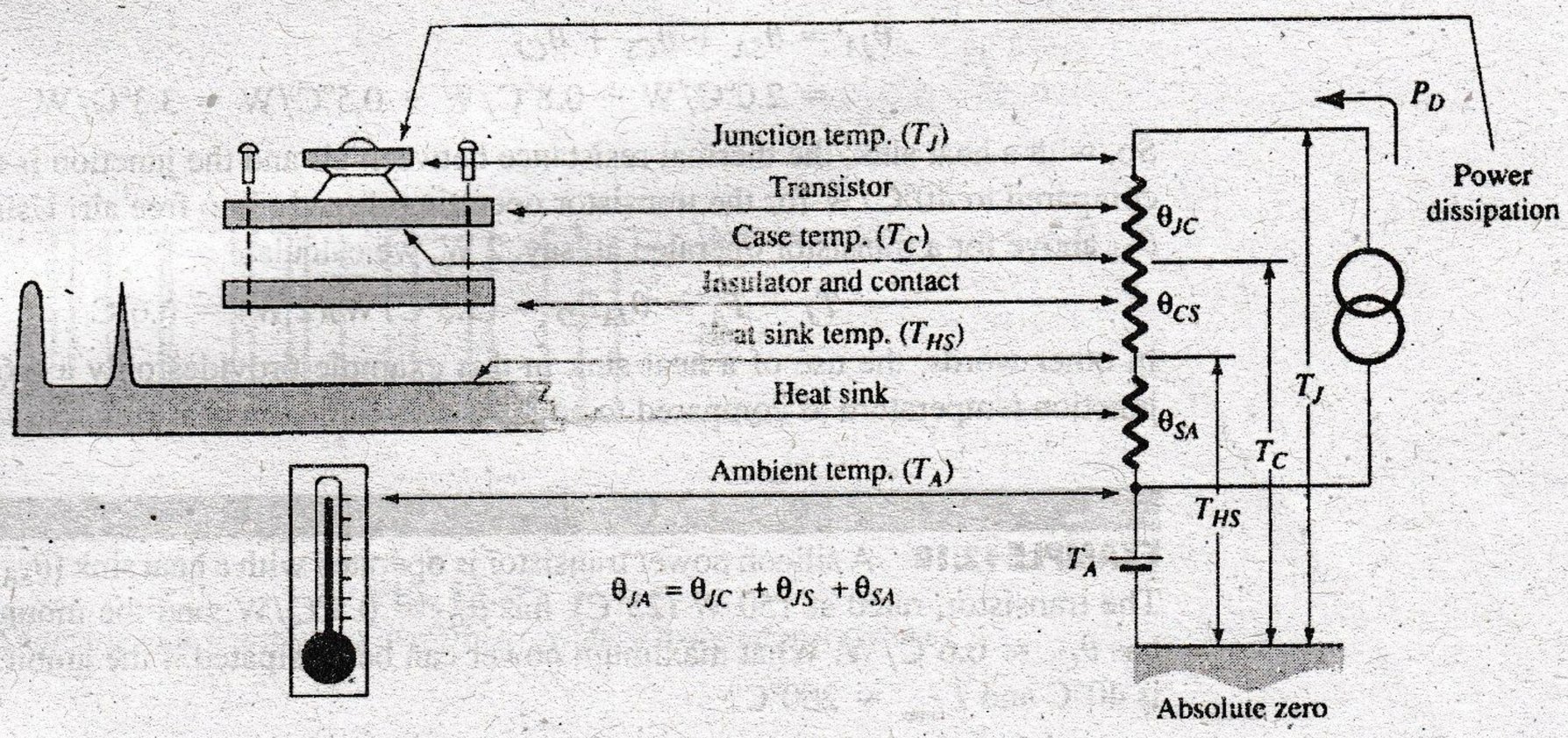


FIG. 12.24
Thermal-to-electrical analogy.

In providing a thermal–electrical analogy, the term *thermal resistance* is used to describe heat effects by an electrical term. The terms in Fig. 12.24 are defined as follows:

θ_{JA} = total thermal resistance (junction to ambient)
θ_{JC} = transistor thermal resistance (junction to case)
θ_{CS} = insulator thermal resistance (case to heat sink)
θ_{SA} = heat-sink thermal resistance (heat sink to ambient)

Using the electrical analogy for thermal resistances, we can write

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}} \tag{12.40}$$

The analogy can also be used in applying Kirchhoff's law to obtain

$$T_J = P_D\theta_{JA} + T_A \tag{12.41}$$

The last relation shows that the junction temperature "floats" on the ambient temperature, and that the higher the ambient temperature, the lower is the allowed value of device power dissipation.

The thermal factor θ provides information about how much temperature drop (or rise) results for a given amount of power dissipation. For example, the value of θ_{JC} is usually about 0.5°C/W. This means that for a power dissipation of 50 W, the difference in temperature

between case temperature (as measured by a thermocouple) and the inside junction temperature is only

$$T_J - T_C = \theta_{JC}P_D = (0.5°C/W)(50\ W) = 25°C$$

Thus, if the heat sink can hold the case at, say, 50°C, the junction is then only at 75°C. This is a relatively small temperature difference, especially at lower power-dissipation levels.

The value of thermal resistance from junction to free air (using no heat sink) is, typically,

$$\theta_{JA} = 40°C/W \qquad \text{(into free air)}$$

For this thermal resistance, only 1 W of power dissipation results in a junction temperature 40°C greater than the ambient.

A heat sink can now be seen to provide a low thermal resistance between case and air—much less than the 40°C/W value of the transistor case alone. Using a heat sink having

$$\theta_{SA} = 2°C/W$$

and with an insulating thermal resistance (from case to heat sink) of

$$\theta_{CS} = 0.8°C/W$$

and finally, for the transistor,

$$\theta_{CJ} = 0.5°C/W$$

we obtain

$$\theta_{JA} = \theta_{SA} + \theta_{CS} + \theta_{CJ}$$
$$= 2.0°C/W + 0.8°C/W + 0.5°C/W = 3.3°C/W$$

So, with a heat sink, the thermal resistance between air and the junction is only 3.3°C/W, compared to 40°C/W for the transistor operating directly into free air. Using the value of θ_{JA} above for a transistor operated at, say, 2 W, we calculate

$$T_J - T_A = \theta_{JA}P_D = (3.3°C/W)(2\ W) = 6.6°C$$

In other words, the use of a heat sink in this example provides only a 6.6°C increase in junction temperature as compared to an 80°C rise without a heat sink.

EXAMPLE 12.18 A silicon power transistor is operated with a heat sink ($\theta_{SA} = 1.5°C/W$). The transistor, rated at 150 W (25°C), has $\theta_{JC} = 0.5°C/W$, and the mounting insulation has $\theta_{CS} = 0.6°C/W$. What maximum power can be dissipated if the ambient temperature is 40°C and $T_{J_{max}} = 200°C$?

Solution:

$$P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{200°C - 40°C}{0.5°C/W + 0.6°C/W + 1.5°C/W} \approx \mathbf{61.5\ W}$$

12.8 CLASS C AND CLASS D AMPLIFIERS

Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, although not used as audio amplifiers, do find use in tuned circuits as in communications.

Class C Amplifier

A class C amplifier, such as that shown in Fig. 12.25, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.

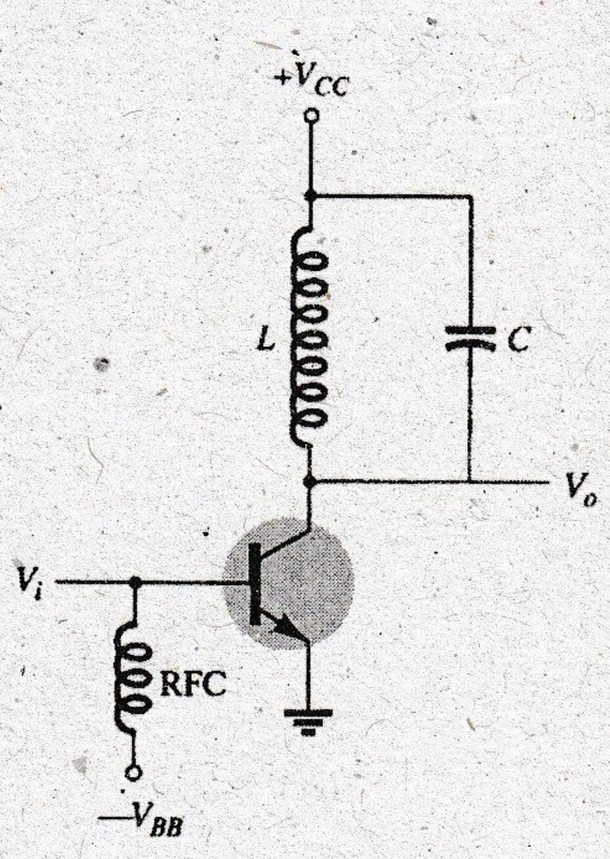


FIG. 12.25
Class C amplifier circuit.

Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power

amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back into a sinusoidal-type signal to recover the original signal. Fig. 12.26 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced. Although the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.

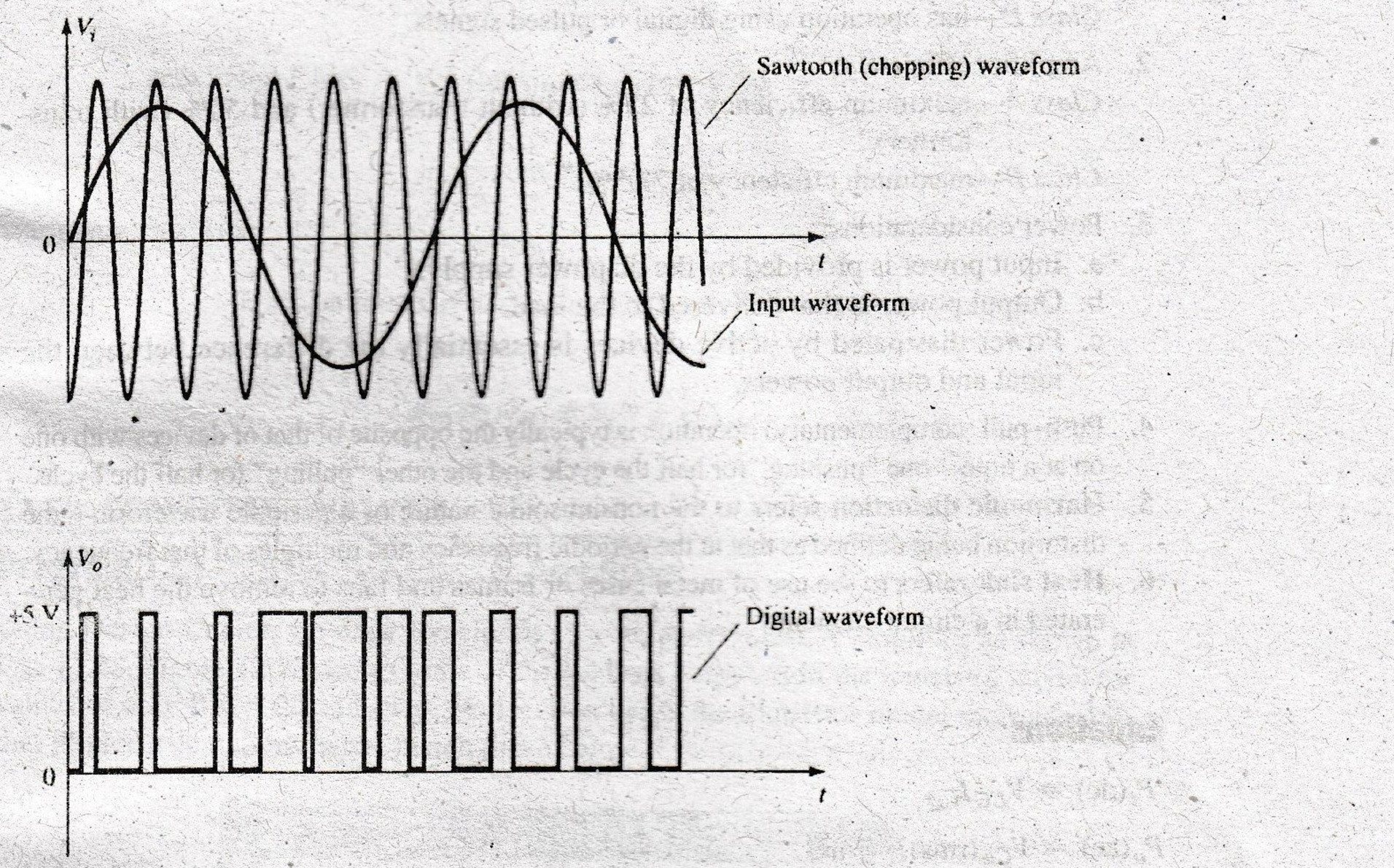


FIG. 12.26
Chopping of a sinusoidal waveform to produce a digital waveform.

Figure 12.27 shows a block diagram of the unit needed to amplify the class D signal and then convert back into the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to their low "on" voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.

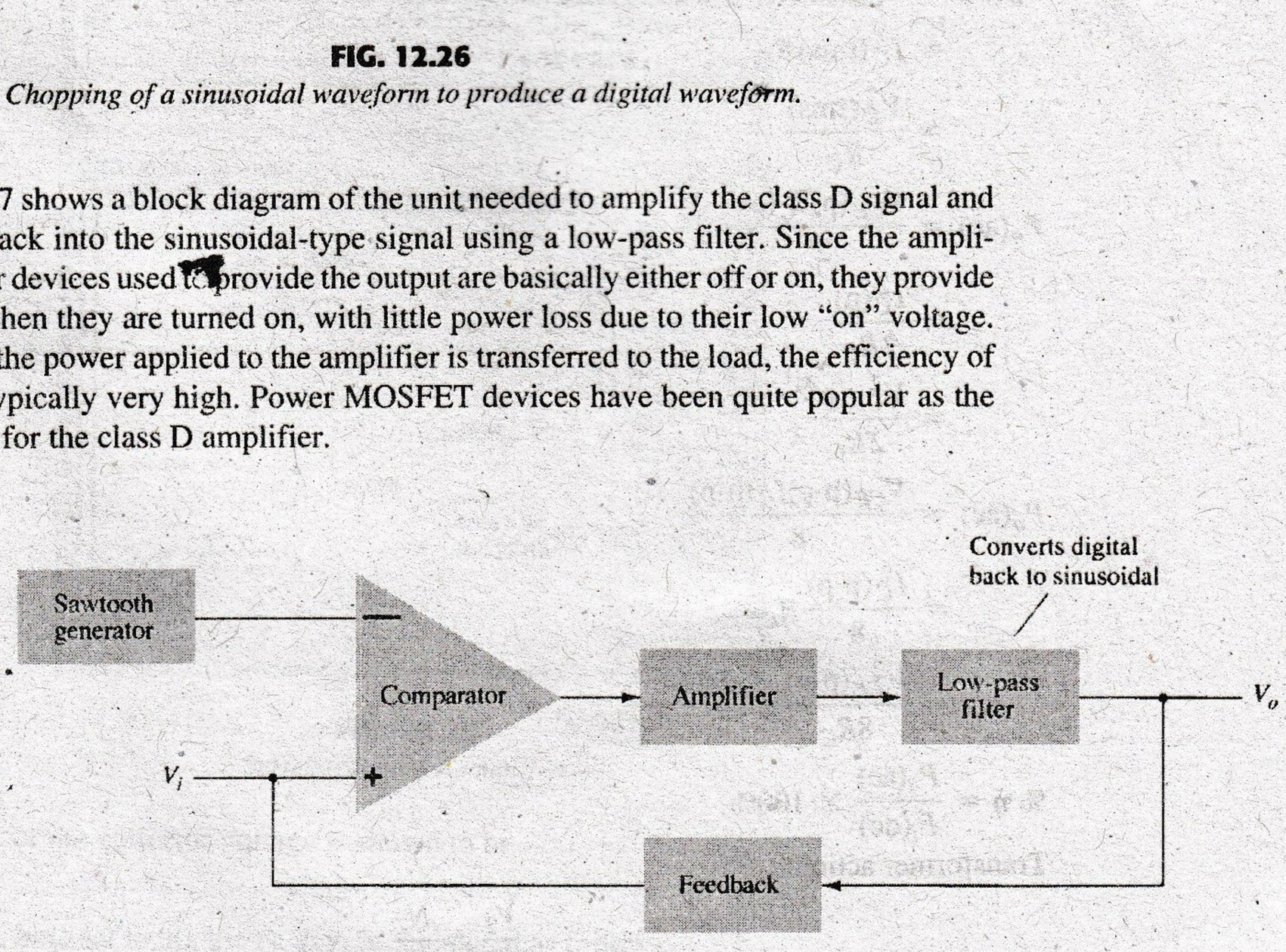


FIG. 12.27
Block diagram of class D amplifier.

12.9 SUMMARY

Important Conclusions and Concepts

1. Amplifier classes:
   Class A—the output stage conducts for a full 360° (a full waveform cycle).
   Class B—the output stages each conduct for 180° (together providing a full cycle).
   Class AB—the output stages each conduct between 180° and 360° (providing a full cycle at less efficiency).
   Class C—the output stage conducts for less than 180° (used in tuned circuits).
   Class D—has operation using digital or pulsed signals.
2. Amplifier efficiency:
   Class A—maximum efficiency of 25% (without transformer) and 50% (with transformer).
   Class B—maximum efficiency of 78.5%.
3. Power considerations:
   a. Input power is provided by the dc power supply.
   b. Output power is that delivered to the load.
   c. Power dissipated by active devices is essentially the difference between the input and output powers.
4. Push–pull (complementary) operation is typically the opposite of that of devices with one on at a time—one "pushing" for half the cycle and the other "pulling" for half the cycle.
5. **Harmonic distortion** refers to the nonsinusoidal nature of a periodic waveform—the distortion being defined as that at the periodic frequency and multiples of that frequency.
6. **Heat sink** refers to the use of metal cases or frames and fans to remove the heat generated in a circuit element.

Equations

$$P_i(\text{dc}) = V_{CC} I_{CQ}$$

$$P_o(\text{ac}) = V_{CE}(\text{rms}) I_C(\text{rms})$$
$$= I_C^2(\text{rms}) R_C$$
$$= \frac{V_C^2(\text{rms})}{R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p}) I_C(\text{p})}{2}$$
$$= \frac{I_C^2(\text{p})}{2R_C}$$
$$= \frac{V_{CE}^2(\text{p})}{2R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p-p}) I_C(\text{p-p})}{8}$$
$$= \frac{I_C^2(\text{p-p})}{8} R_C$$
$$= \frac{V_{CE}^2(\text{p-p})}{8R_C}$$

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Transformer action:

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Class B operation:

$$I_{dc} = \frac{2}{\pi} I(\text{p})$$

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi} I(\text{p})\right)$$

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L}$$

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}$$

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{dc}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}$$

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

Harmonic distortion:

$$\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

Heat sink:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

12.10 COMPUTER ANALYSIS

Program 12.1—Series-Fed Class A Amplifier

Using Design Center, we draw the circuit of a series-fed class A amplifier as shown in Fig. 12.28. Figure 12.29 shows some of the analysis output. Edit the transistor model for values of only **BF** = 90 and **IS** = 2E-15. This keeps the transistor model more ideal so that PSpice calculations better match those below.

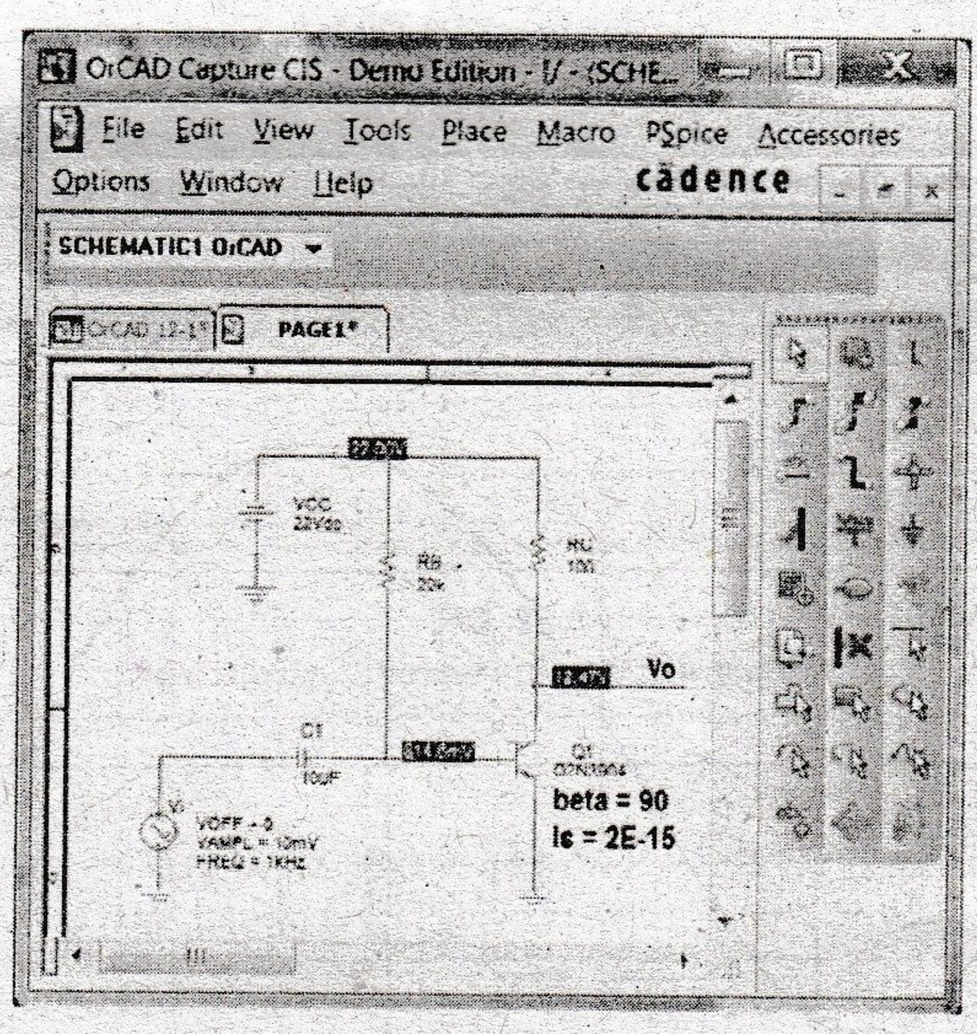


FIG. 12.28
Series-fed class A amplifier.

The dc bias of the collector voltage is shown to be

$$V_c(\text{dc}) = 12.47\ \text{V}$$

With transistor beta set to 90, the ac gain is calculated as follows:

$$I_E = I_c = 95\ \text{mA (from analysis output of PSpice)}$$

$$r_e = 26\ \text{mV}/95\ \text{mA} = 0.27\ \Omega$$

```
Series-fed Class-A Amplifier

****     CIRCUIT DESCRIPTION
******************************************************************************
****     BJT MODEL PARAMETERS
         Q2N3904
         NPN
      IS  2.000000E-15
      BF  90

****     SMALL SIGNAL BIAS SOLUTION
******************************************************************************
 NODE   VOLTAGE  NODE   VOLTAGE  NODE   VOLTAGE  NODE   VOLTAGE
(N00210) .8146  (N00214) 0.0000  (N00232) 22.0000 (N00286) 12.4670

  VOLTAGE SOURCE CURRENTS
  NAME      CURRENT
  V_VCC     -9.639E-02
  V_Vi       0.000E+00

TOTAL POWER DISSIPATION  2.12E+00  WATTS
```

FIG. 12.29

Analysis output for the circuit of Fig. 12.28.

For a gain of

$$A_v = -R_c/r_e = -100/0.27 = -370$$

The output voltage is then

$$V_o = A_v V_i = (-370) \cdot 10\,\text{mV} = -3.7\,\text{V(peak)}$$

The output waveform obtained using **probe** is shown in Fig. 12.30. For a peak-to-peak output of

$$V_o\text{(p-p)} = 15.6\,\text{V} - 8.75\,\text{V} = 6.85\,\text{V}$$

the peak output is

$$V_o\text{(p)} = 6.85\,\text{V}/2 = 3.4\,\text{V}$$

which compares well with that calculated below.

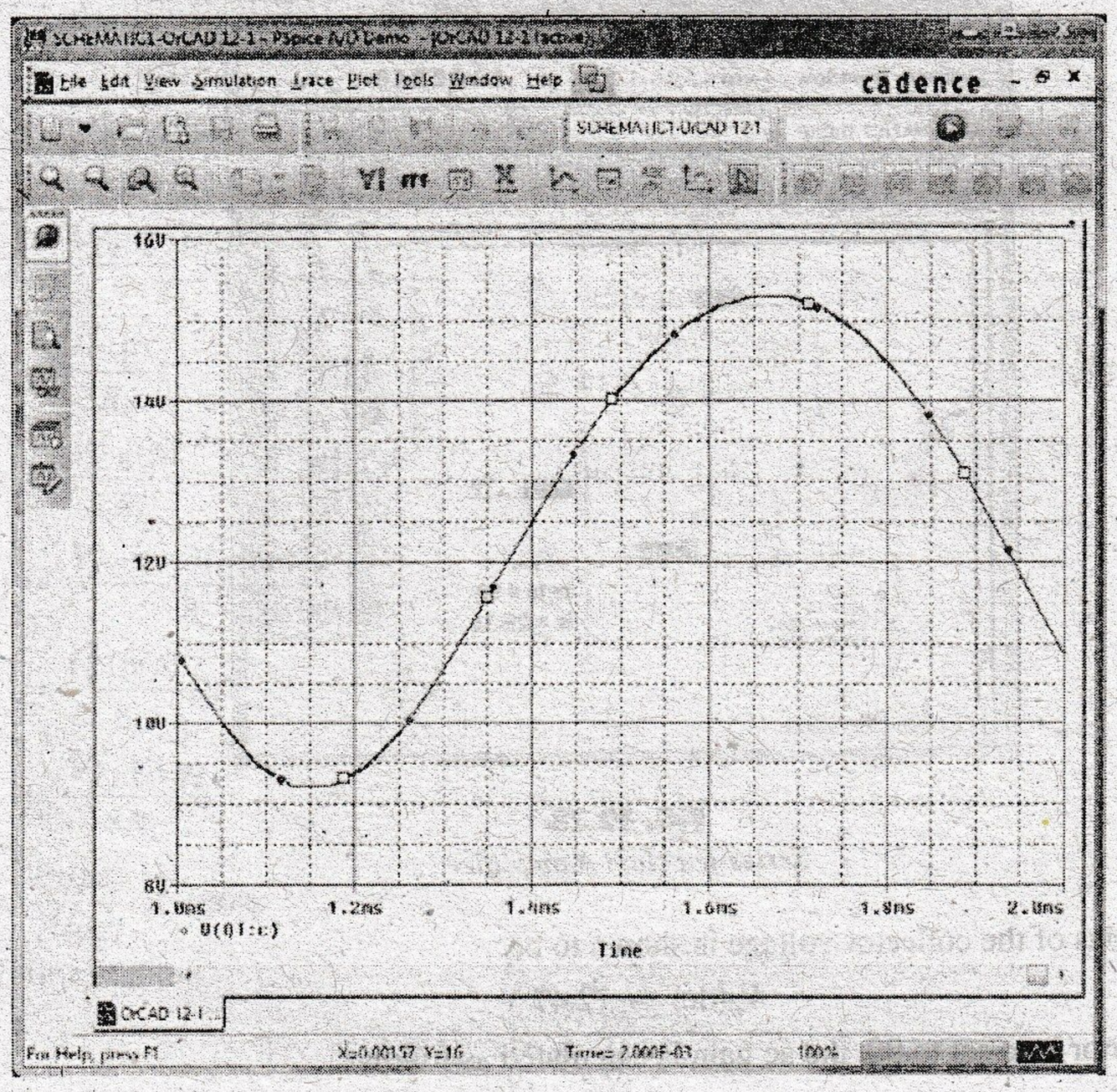


FIG. 12.30

Probe output for the circuit of Fig. 12.28.

From the circuit output analysis, the input power is

$$P_i = V_{CC}I_C = (22\text{ V}) \cdot (95\text{ mA}) = 2.09\text{ W}$$

From the probe ac data, the output power is

$$P_o(\text{ac}) = V_o(\text{p-p})^2/[8 \cdot R_L] = (6.85)^2/[8 \cdot 100] = 58\text{ mW}$$

The efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (58\text{ mW}/2.09\text{ W}) \cdot 100\% = 2.8\%$$

A larger input signal would increase the ac power delivered to the load and increase the efficiency (the maximum being 25%).

Program 12.2–Quasi-Complementary Push–Pull Amplifier

Figure 12.31 shows a quasi-complementary push–pull class B power amplifier. For the input of $V_i = 20\text{ V(p)}$, the output waveform obtained using **probe** is shown in Fig. 12.32.

The resulting ac output voltage is seen to be

$$V_o(\text{p-p}) = 33.7\text{ V}$$

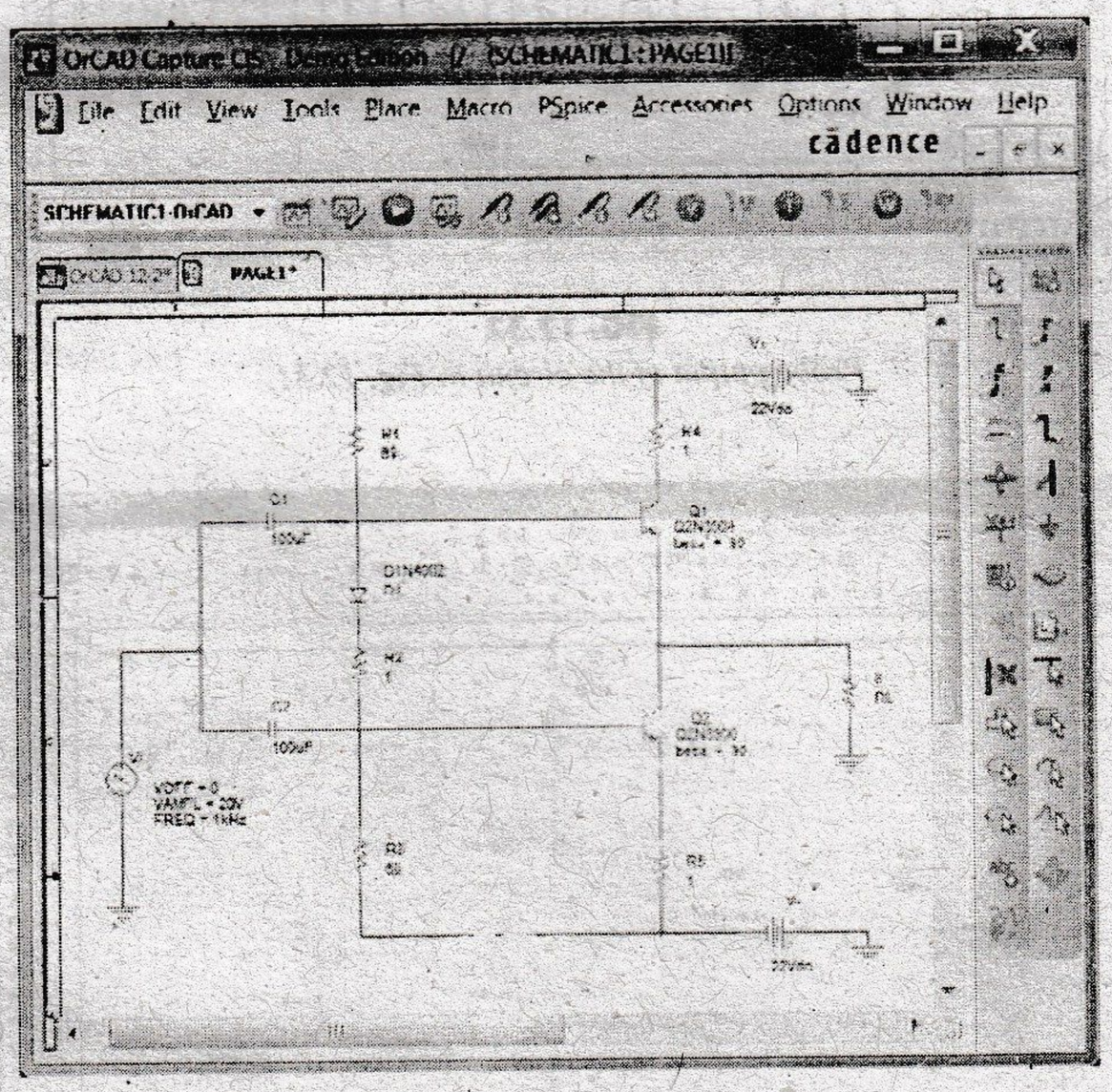


FIG. 12.31

Quasi-complementary class B power amplifier.

so that

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (33.7\text{ V})^2/(8 \cdot 8\ \Omega) = 17.7\text{ W}$$

The input power for that amplitude signal is

$$P_i = V_{CC}I_{dc} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)/R_L]$$
$$= (22\text{ V}) \cdot [(2/\pi)(33.7\text{ V}/2)/8] = 29.5\text{ W}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (17.7\text{ W}/29.5\text{ W}) \cdot 100\% = 60\%$$

Program 12.3–Op-Amp Push–Pull Amplifier

Figure 12.33 shows an op-amp push–pull amplifier providing ac output to an 8-Ω load. As shown, the op-amp provides a gain of

$$A_v = -R_F/R_1 = -47\text{ k}\Omega/18\text{ k}\Omega = -2.6$$

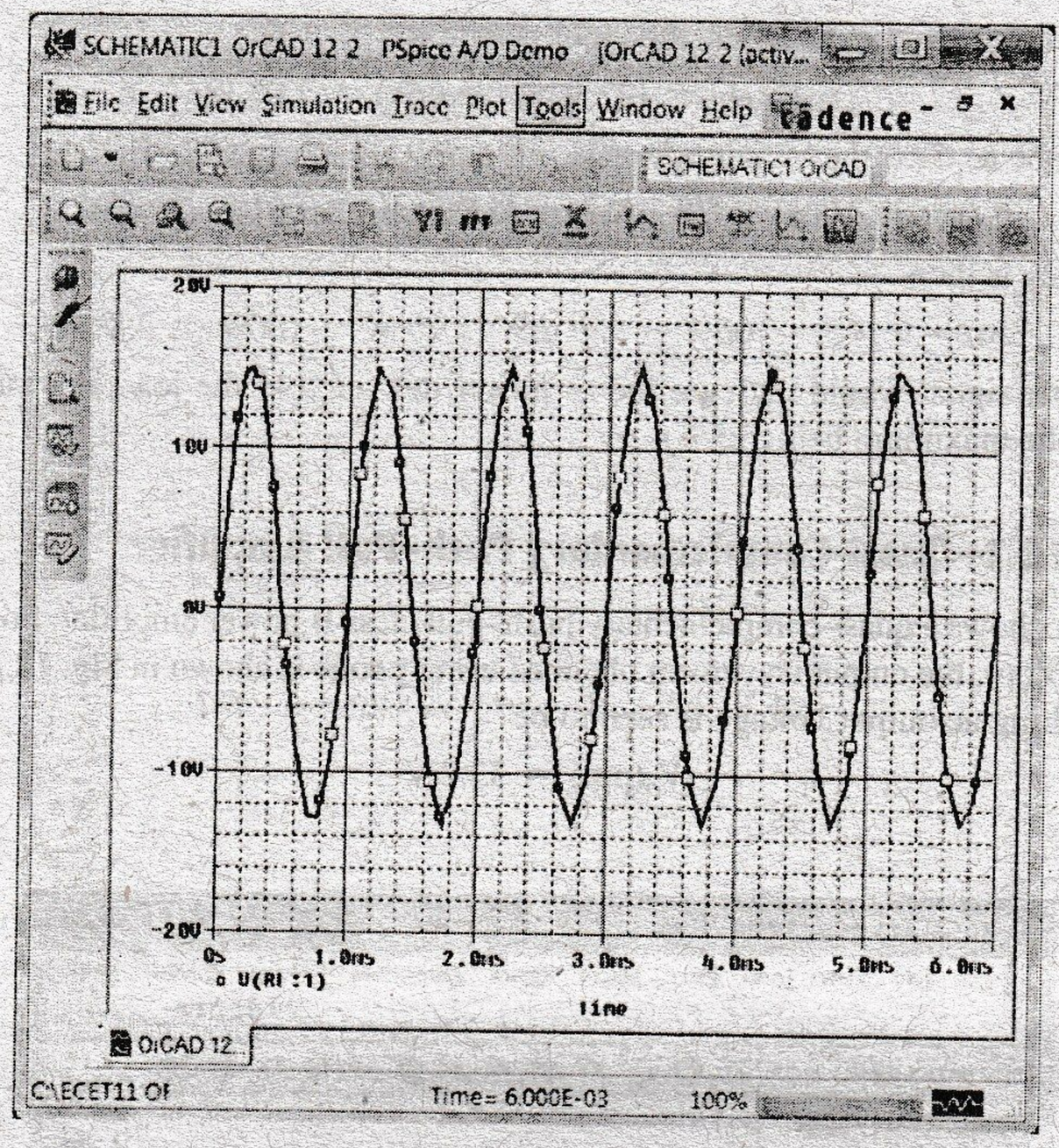


FIG. 12.32

Probe output of the circuit in Fig. 12.31.

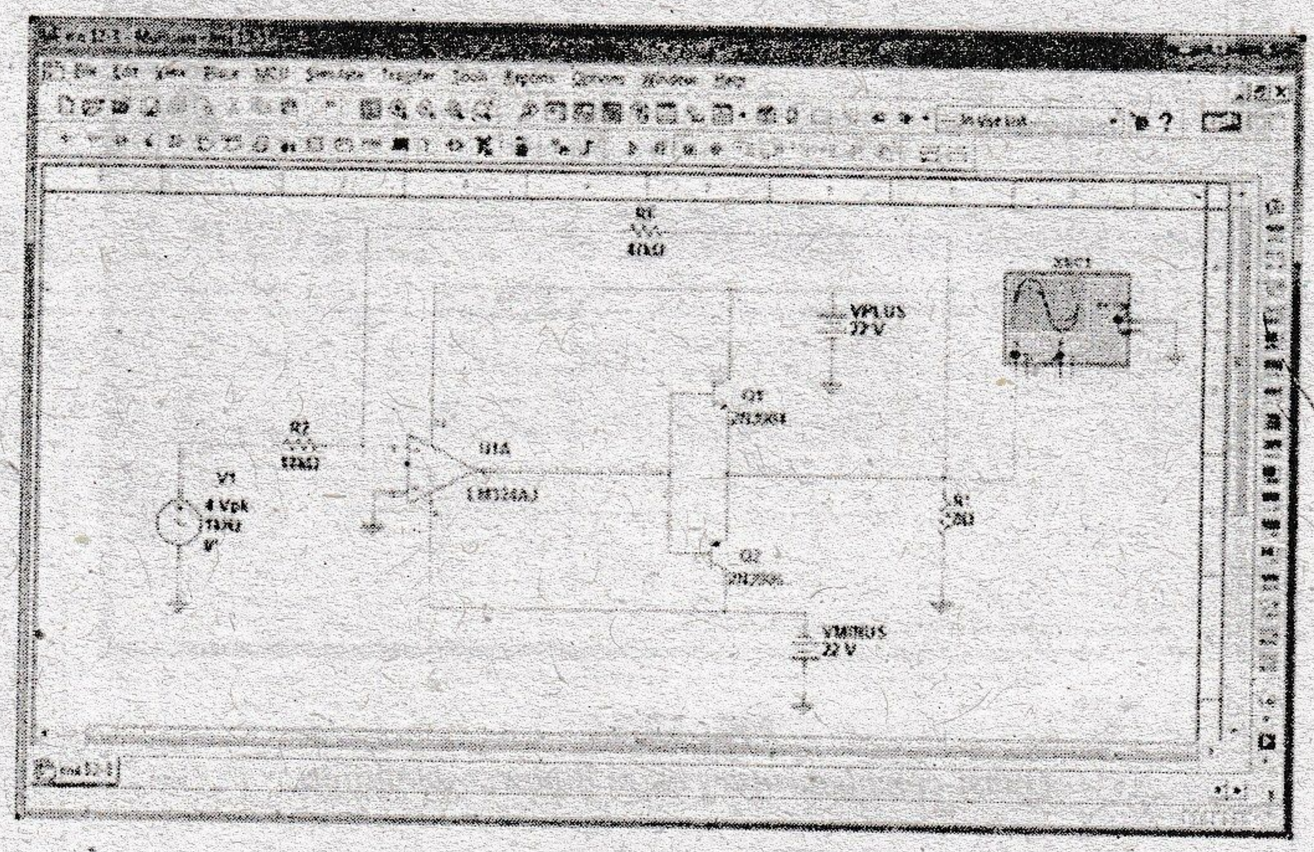


FIG. 12.33

Op-amp class B amplifier.

For the input $V_i = 1$ V, the output is

$$V_o(\text{p}) = A_v V_i = -2.6 \cdot (1\text{ V}) = -2.6\text{ V}$$

Figure 12.34 shows the oscilloscope display of the output voltage.

The output power is then calculated to be

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (20.4\text{ V})^2/(8 \cdot 8\ \Omega) = 6.5\text{ W}$$

The input power for that amplitude signal is

$$P_i = V_{CC} I_{dc} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)/R_L]$$
$$= (12\text{ V}) \cdot [(2/\pi) \cdot (20.4\text{ V}/2)/8] = 9.7\text{ W}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (6.5\text{ W}/9.7\text{ W}) \cdot 100\% = 67\%$$

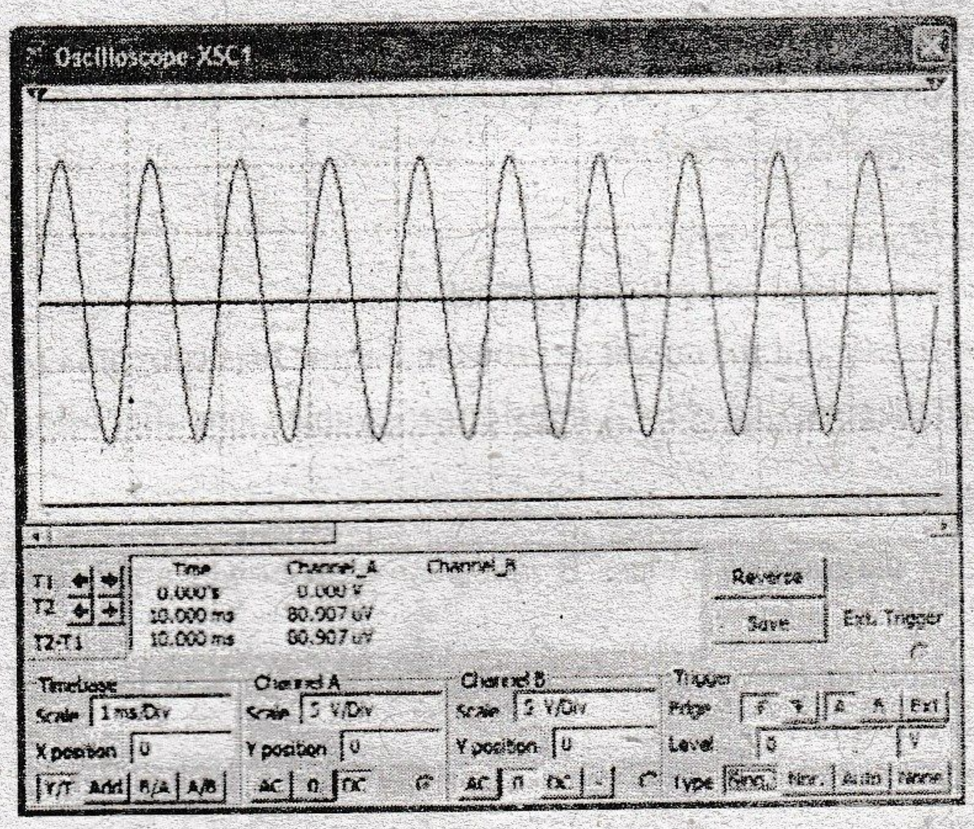


FIG. 12.34
Probe output for the circuit of Fig. 12.33.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

12.2 Series-Fed Class A Amplifier

1. Calculate the input and output power for the circuit of Fig. 12.35. The input signal results in a base current of 5 mA rms.

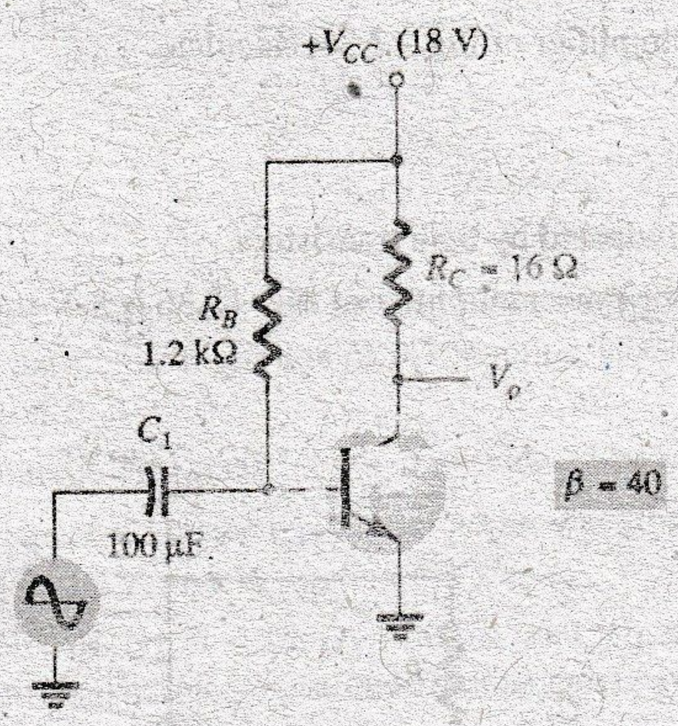


FIG. 12.35
Problems 1 to 4 and 26.

2. Calculate the input power dissipated by the circuit of Fig. 12.35 if R_B is changed to 1.5 kΩ.
3. What maximum output power can be delivered by the circuit of Fig. 12.35 if R_B is changed to 1.5 kΩ?
4. If the circuit of Fig. 12.35 is biased at its center voltage and center collector operating point, what is the input power for a maximum output power of 1.5 W?

12.3 Transformer-Coupled Class A Amplifier

5. A class A transformer-coupled amplifier uses a 25:1 transformer to drive a 4-Ω load. Calculate the effective ac load (seen by the transistor connected to the larger turns side of the transformer).
6. What turns ratio transformer is needed to couple to an 8-Ω load so that it appears as an 8-kΩ effective load?
7. Calculate the transformer turns ratio required to connect four parallel 16-Ω speakers so that they appear as an 8-kΩ effective load.

*8. A transformer-coupled class A amplifier drives a 16-Ω speaker through a 3.87:1 transformer. Using a power supply of $V_{CC} = 36$ V, the circuit delivers 2 W to the load. Calculate:
   a. P(ac) across transformer primary.
   b. V_L(ac).
   c. V(ac) at transformer primary.
   d. The rms values of load and primary current.

9. Calculate the efficiency of the circuit of Problem 8 if the bias current is $I_{C_Q} = 150$ mA.

10. Draw the circuit diagram of a class A transformer-coupled amplifier using an *npn* transistor.

12.4 Class B Amplifier Operation

11. Draw the circuit diagram of a class B *npn* push–pull power amplifier using transformer-coupled input.

12. For a class B amplifier providing a 22-V peak signal to an 8-Ω load and a power supply of $V_{CC} = 25$ V, determine:
   a. Input power.
   b. Output power.
   c. Circuit efficiency.

13. For a class B amplifier with $V_{CC} = 25$ V driving an 8-Ω load, determine:
   a. Maximum input power.
   b. Maximum output power.
   c. Maximum circuit efficiency.

*14. Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 22$ V driving a 4-Ω load with peak output voltages of:
   a. $V_L(\text{p}) = 20$ V.
   b. $V_L(\text{p}) = 4$ V.

12.5 Class B Amplifier Circuits

15. Sketch the circuit diagram of a quasi-complementary amplifier, showing voltage waveforms in the circuit.

16. For the class B power amplifier of Fig. 12.36, calculate:
   a. Maximum P_o(ac).
   b. Maximum P_i(dc).
   c. Maximum $\%\eta$.
   d. Maximum power dissipated by both transistors.

*17. If the input voltage to the power amplifier of Fig. 12.36 is 8-V rms, calculate:
   a. P_i(dc).
   b. P_o(ac).

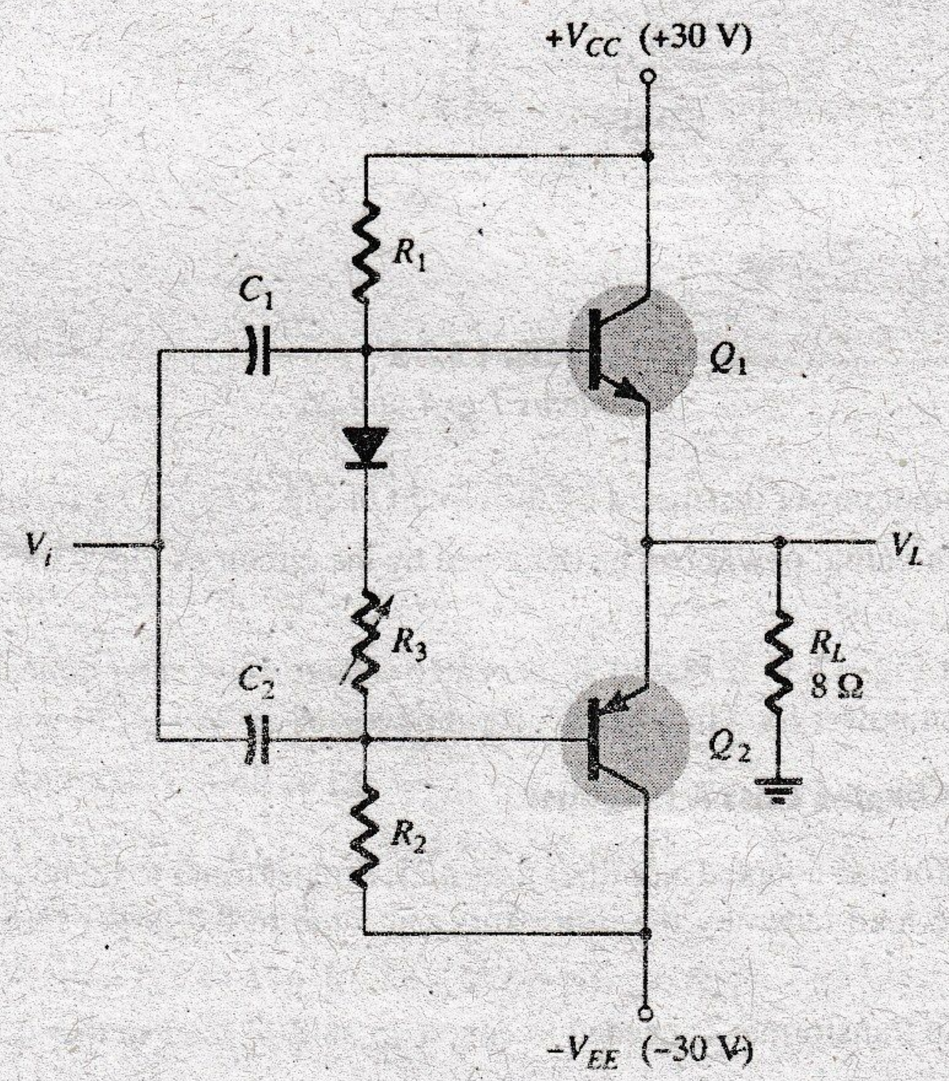


FIG. 12.36
Problems 16, 17, and 27.

c. $\%\eta$.
d. Power dissipated by both power output transistors.

*18. For the power amplifier of Fig. 12.37, calculate:
a. P_o(ac).
b. P_i(dc).
c. $\%\eta$.
d. Power dissipated by both output transistors.

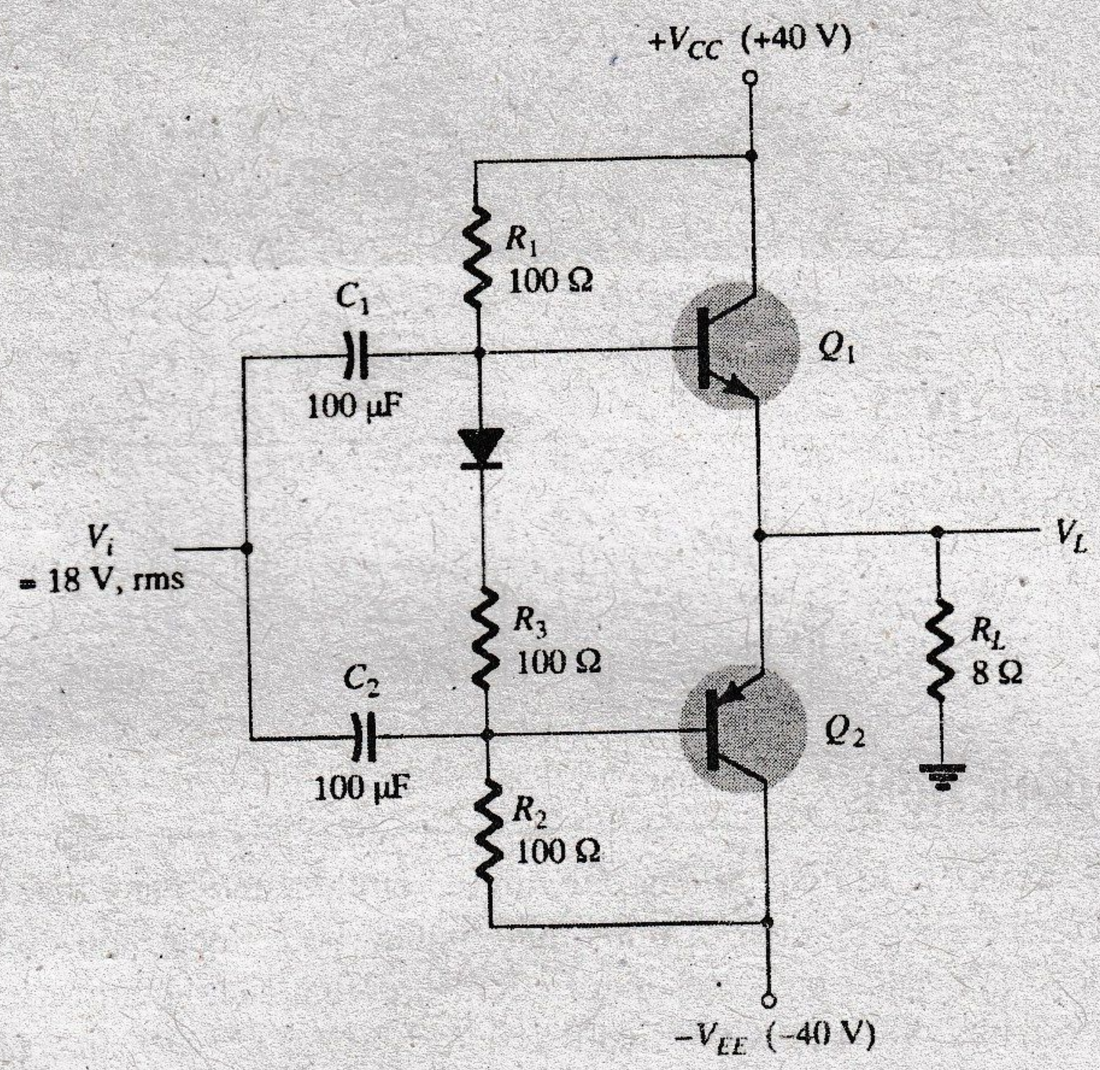


FIG. 12.37
Problem 18.

12.6 Amplifier Distortion

19. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.1 V, second harmonic amplitude of 0.3 V, third harmonic component of 0.1 V, and fourth harmonic component of 0.05 V.

20. Calculate the total harmonic distortion for the amplitude components of Problem 19.

21. Calculate the second harmonic distortion for an output waveform having measured values of $V_{CE_{min}} = 2.4$ V, $V_{CE_Q} = 10$ V, and $V_{CE_{max}} = 20$ V.

22. For distortion readings of $D_2 = 0.15$, $D_3 = 0.01$, and $D_4 = 0.05$, with $I_1 = 3.3$ A and $R_C = 4\ \Omega$, calculate the total harmonic distortion fundamental power component and total power.

12.7 Power Transistor Heat Sinking

23. Determine the maximum dissipation allowed for a 100-W silicon transistor (rated at 25°C) for a derating factor of 0.6 W/°C at a case temperature of 150°C.

*24. A 160-W silicon power transistor operated with a heat sink ($\theta_{SA} = 1.5$°C/W) has $\theta_{JC} = 0.5$°C/W and a mounting insulation of $\theta_{CS} = 0.8$°C/W. What maximum power can be handled by the transistor at an ambient temperature of 80°C? (The junction temperature should not exceed 200°C.)

25. What maximum power can a silicon transistor ($T_{J_{max}} = 200$°C) dissipate into free air at an ambient temperature of 80°C?

12.9 Computer Applications

*26. Use Design Center to draw the schematic of Fig. 12.35 with $V_i = 9.1$ mV.

*27. Use Design Center to draw the schematic of Fig. 12.36 with $V_i = 25$ V(p). Determine the circuit efficiency.

*28. Use Multisim to draw the schematic of an op-amp class B amplifier as in Fig. 12.33. Use $R_1 = 10\ \text{k}\Omega$, $R_F = 50\ \text{k}\Omega$, and $V_i = 2.5$ V(p). Determine the circuit efficiency.