13 Linear-Digital ICs

CHAPTER OBJECTIVES

- About analog-to-digital conversion
- About digital-to-analog conversion
- Operation of a timer circuit
- Operation of phase-locked loops

13.1 INTRODUCTION

Although there are many ICs containing only digital circuits and many that contain only linear circuits, there are a number of units that contain both linear and digital circuits. Among the linear/digital ICs are comparator circuits, digital/analog converters, interface circuits, timer circuits, voltage-controlled oscillator (VCO) circuits, and phase-locked loops (PLLs).

The comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing whether the input voltage exceeded the reference voltage.

Circuits that convert digital signals into an analog or linear voltage and those that convert a linear voltage into a digital value are popular in aerospace equipment, automotive equipment, and compact disk (CD) players, among many other applications.

Interface circuits are used to enable connecting signals of different digital voltage levels, from different types of output devices, or from different impedances so that both the driver stage and the receiver stage operate properly.

Timer ICs provide linear and digital circuits to use in various timing operations, as in a car alarm, a home timer to turn lights on or off, and a circuit in electromechanical equipment to provide proper timing to match the intended unit operation. The 555 timer has long been a popular IC unit. A voltage-controlled oscillator provides an output clock signal whose frequency can be varied or adjusted by an input voltage. One popular application of a VCO is in a phase-locked loop unit, as used in various communication transmitters and receivers.

13.2 COMPARATOR UNIT OPERATION

A comparator circuit accepts input of linear voltages and provides a digital output that indicates when one input is less than or greater than the second. A basic comparator circuit can be represented as in Fig. 13.1a. The output is a digital signal that stays at a high voltage

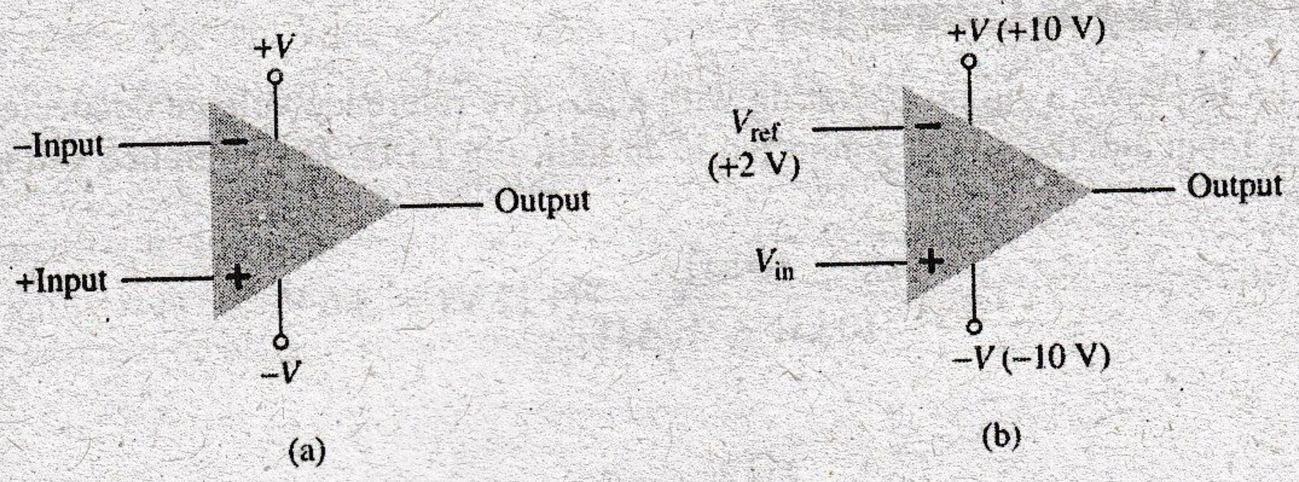


FIG. 13.1
Comparator unit: (a) basic unit; (b) typical application.

level when the noninverting (+) input is greater than the voltage at the inverting (−) input and switches to a lower voltage level when the noninverting input voltage goes below the inverting input voltage.

Figure 13.1b shows a typical connection with one input (the inverting input in this example) connected to a reference voltage of 2 V, the non-inverting input terminal connected as the input signal voltage. As long as V_{in} is less than the reference voltage level of +2 V, the output remains at a low voltage level (near −10 V). When the input rises just above +2 V, the output quickly switches to a high-voltage level (near +10 V). Thus the high output indicates that the input signal is greater than +2 V.

Because the internal circuit used to build a comparator contains essentially an op-amp circuit with very high voltage gain, we can examine the operation of a comparator using a 741 op-amp, as shown in Fig. 13.2. With reference input (at pin 2) set to 0 V, a sinusoidal signal applied to the noninverting input (pin 3) will cause the output to switch between its two output states, as shown in Fig. 13.2b. The input V_i going even a fraction of a millivolt above the 0-V reference level will be amplified by the very high voltage gain (typically over 100,000), so that the output rises to its positive output saturation level and remains there, while the input stays above $V_{ref} = 0$ V. When the input drops just below the 0-V reference level, the output is driven to its lower saturation level and stays there, while the input remains below $V_{ref} = 0$ V. Figure 13.2b clearly shows that the input signal is linear, whereas the output is digital.

In general use, the reference voltage need not be 0 V but can be any desired positive or negative voltage. Also, the reference voltage may be connected to either plus or minus input and the input signal then applied to the other input.

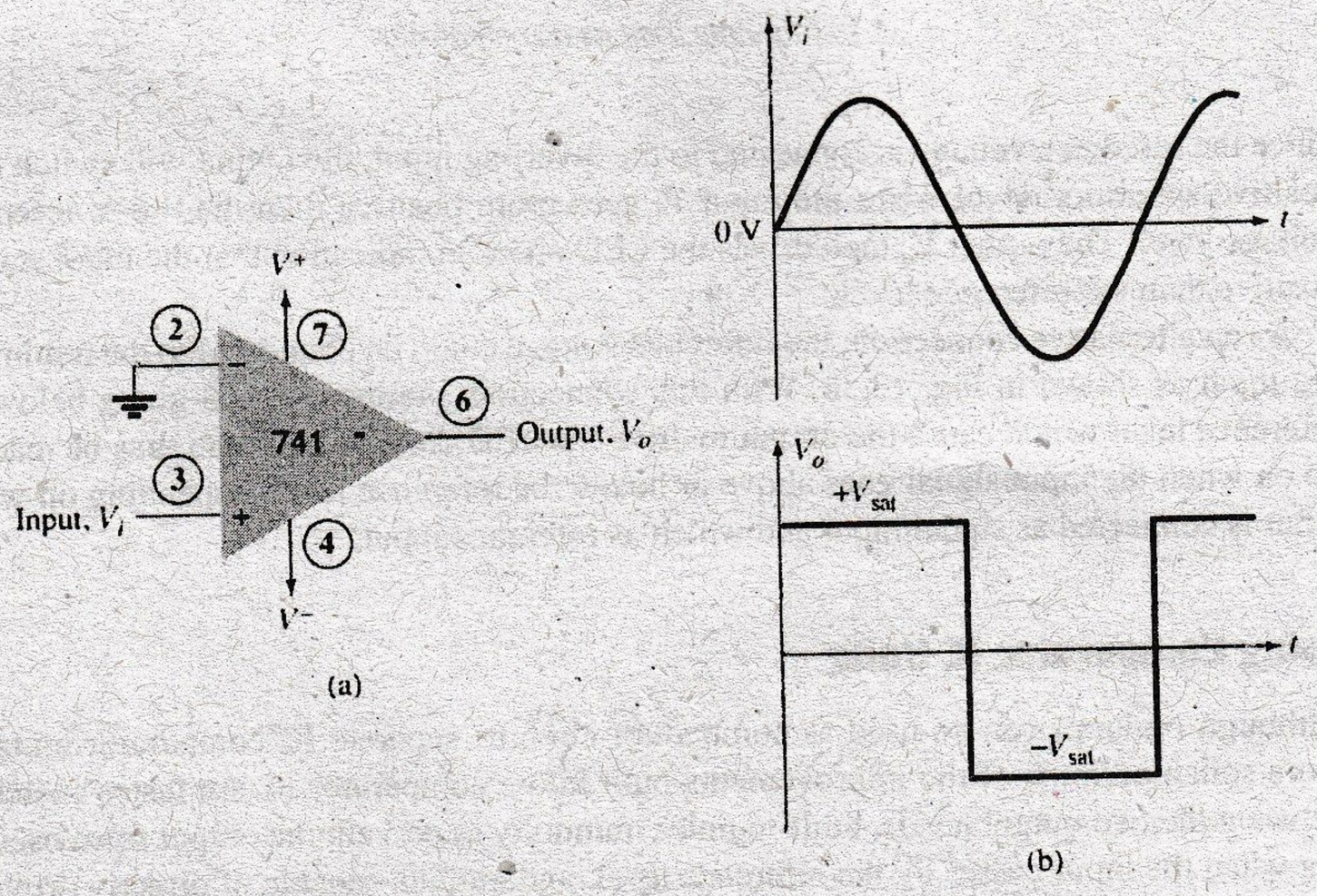


FIG. 13.2
Operation of a 741 op-amp as a comparator.

Use of Op-Amp as Comparator

Figure 13.3a shows a circuit operating with a positive reference voltage connected to the inverting input and the output connected to an indicator LED. The reference voltage level is set at

$$V_{ref} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega + 10\,\text{k}\Omega}(+12\,\text{V}) = +6\,\text{V}$$

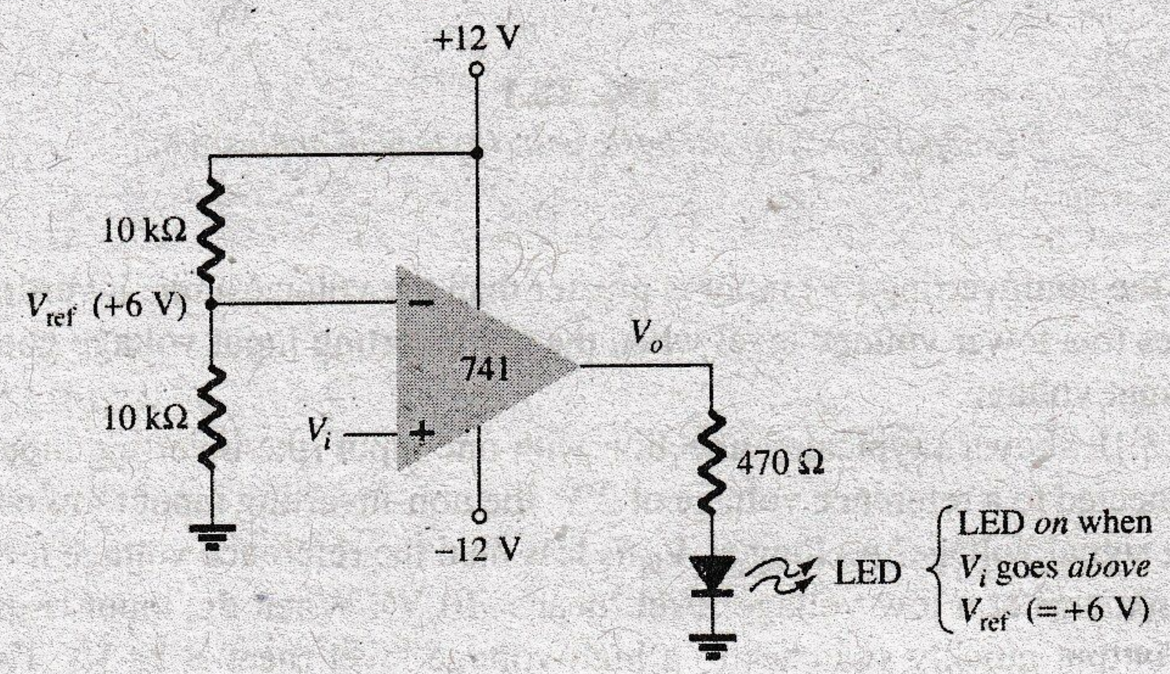


FIG. 13.3
A 741 op-amp used as a comparator.

Since the reference voltage is connected to the inverting input, the output will switch to its positive saturation level when the input V_i goes more positive than the +6-V reference voltage level. The output V_o then drives the LED on as an indication that the input is more positive than the reference level.

As an alternative connection, the reference voltage could be connected to the noninverting input as shown in Fig. 13.3b. With this connection, the input signal going below the reference level would cause the output to drive the LED on. The LED can thus be made to go on when the input signal goes above or below the reference level, depending on which input is connected as signal input and which as reference input.

Using Comparator IC Units

Although op-amps can be used as comparator circuits, separate IC comparator units are more suitable. Some of the improvements built into a comparator IC are faster switching between the two output levels, built-in noise immunity to prevent the output from oscillating when the input passes by the reference level, and outputs capable of directly driving a variety of loads. A few popular IC comparators are covered next, describing their pin connections and how they may be used.

311 Comparator The 311 voltage comparator shown in Fig. 13.4 contains a comparator circuit that can operate as well from dual power supplies of ±15 V as from a single +5-V supply (as used in digital logic circuits). The output can provide a voltage at one of two distinct levels or can be used to drive a lamp or a relay. Notice that the output is taken from a bipolar transistor to allow driving a variety of loads. The unit also has balance and strobe inputs, the strobe input allowing gating of the output. A few examples will show how this comparator unit can be used in some common applications.

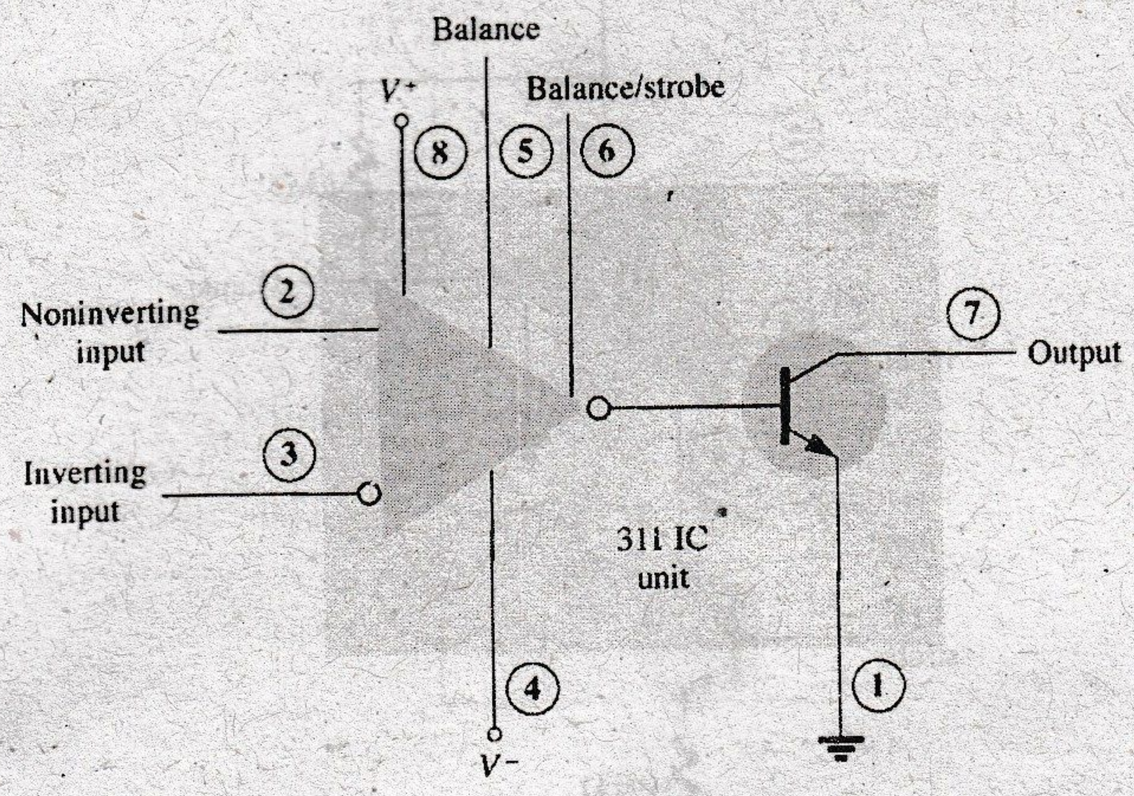


FIG. 13.4
A 311 comparator (eight-pin DIP unit).

A zero-crossing detector that senses (detects) the input voltage crossing through 0 V is shown using the 311 IC in Fig. 13.5. The inverting input is connected to ground (the reference voltage). The input signal going positive drives the output transistor on, with the output then going low (−10 V in this case). The input signal going negative (below 0 V) will drive the output transistor off, the output then going high (to +10 V). The output is thus an indication of whether the input is above or below 0 V. When the input is any positive voltage, the output is low, whereas any negative voltage will result in the output going to a high voltage level.

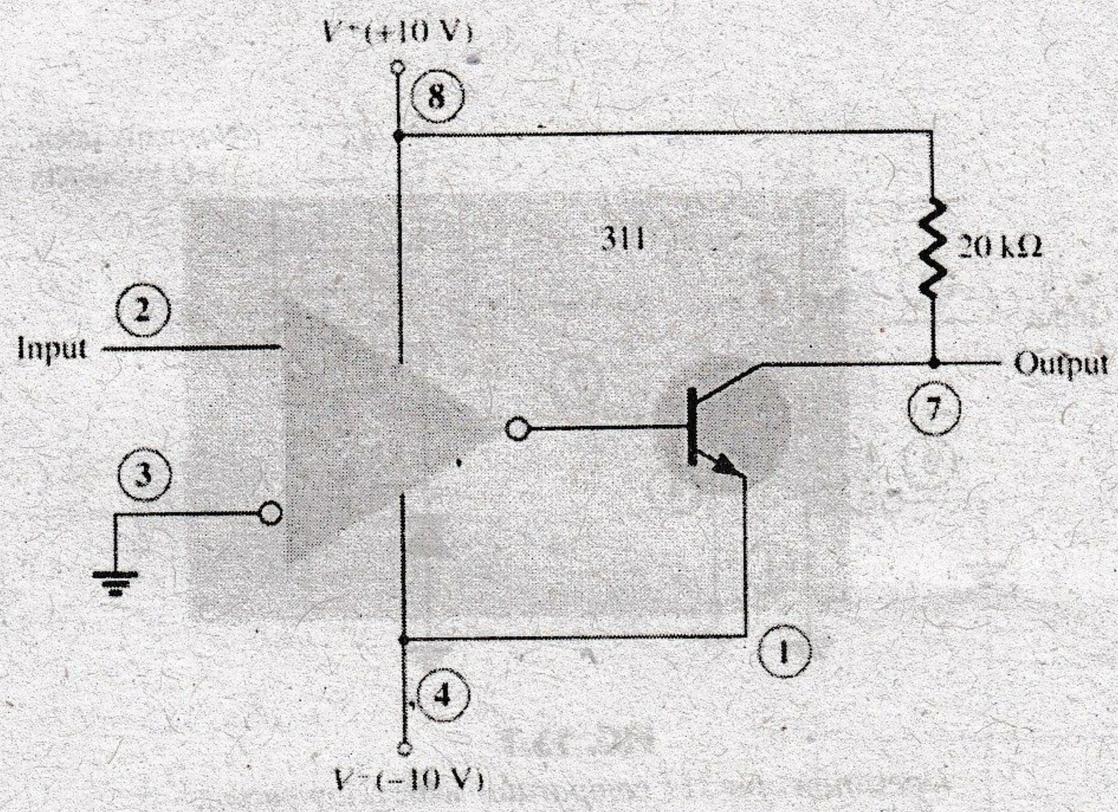


FIG. 13.5
Zero-crossing detector using a 311 IC.

Figure 13.6 shows how a 311 comparator can be used with strobing. In this example, the output will go high when the input goes above the reference level—but only if the TTL strobe input is off (or 0 V). If the TTL strobe input goes high, it drives the 311 strobe input

at pin 6 low, causing the output to remain in the "off" state (with output high) regardless of the input signal. In effect, the output remains high unless strobed. If strobed, the output then acts normally, switching from high to low depending on the input signal level. In operation, the comparator output will respond to the input signal only during the time the strobe signal allows such operation.

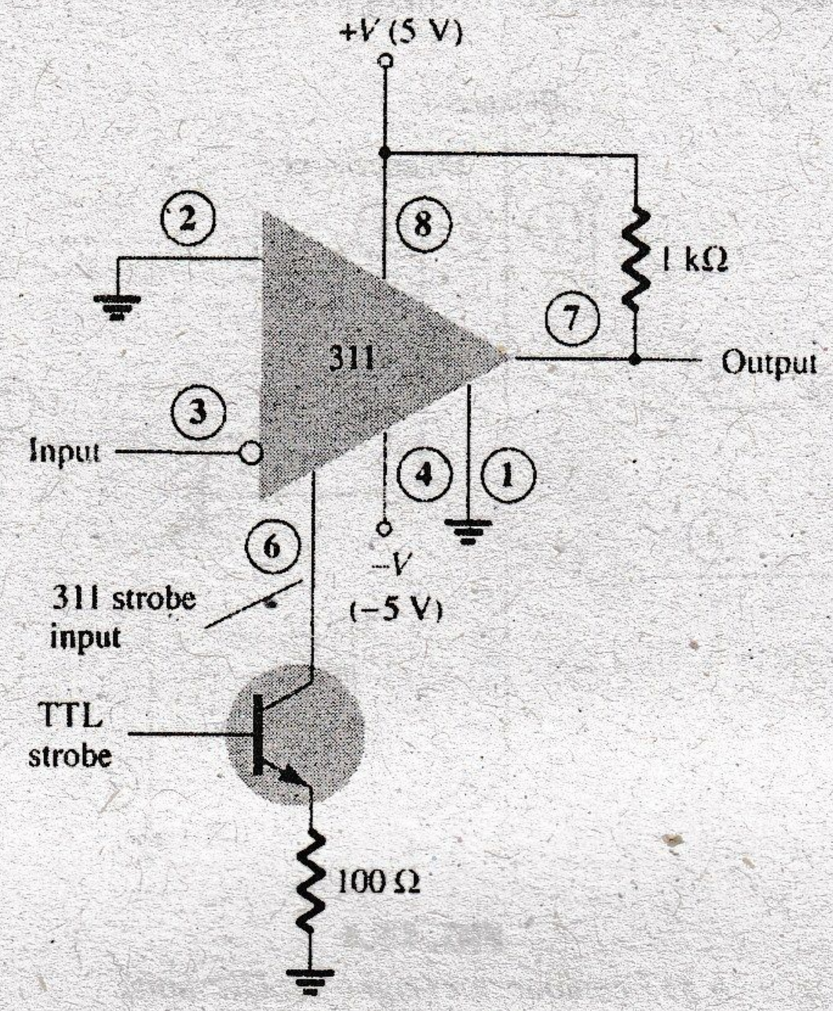


FIG. 13.6
Operation of a 311 comparator with strobe input.

Figure 13.7 shows the comparator output driving a relay. When the input goes below 0 V, driving the output low, the relay is activated, closing the normally open (N.O.) contacts at that time. These contacts can then be connected to operate a large variety of devices. For example, a buzzer or a bell wired to the contacts can be driven on whenever the input voltage drops below 0 V. As long as the voltage is present at the input terminal, the buzzer will remain off.

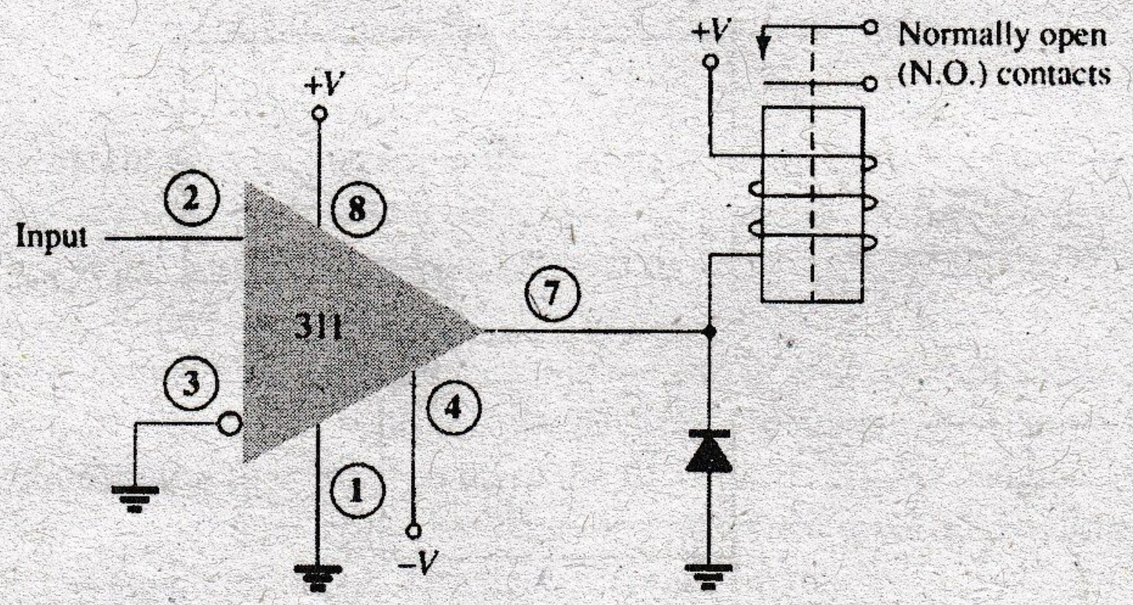


FIG. 13.7
Operation of a 311 comparator with relay output.

339 Comparator The 339 IC is a quad comparator containing four independent voltage comparator circuits connected to external pins as shown in Fig. 13.8. Each comparator has inverting and noninverting inputs and a single output. The supply voltage applied to a pair of pins powers all four comparators. Even if one wishes to use one comparator, all four will be drawing power.

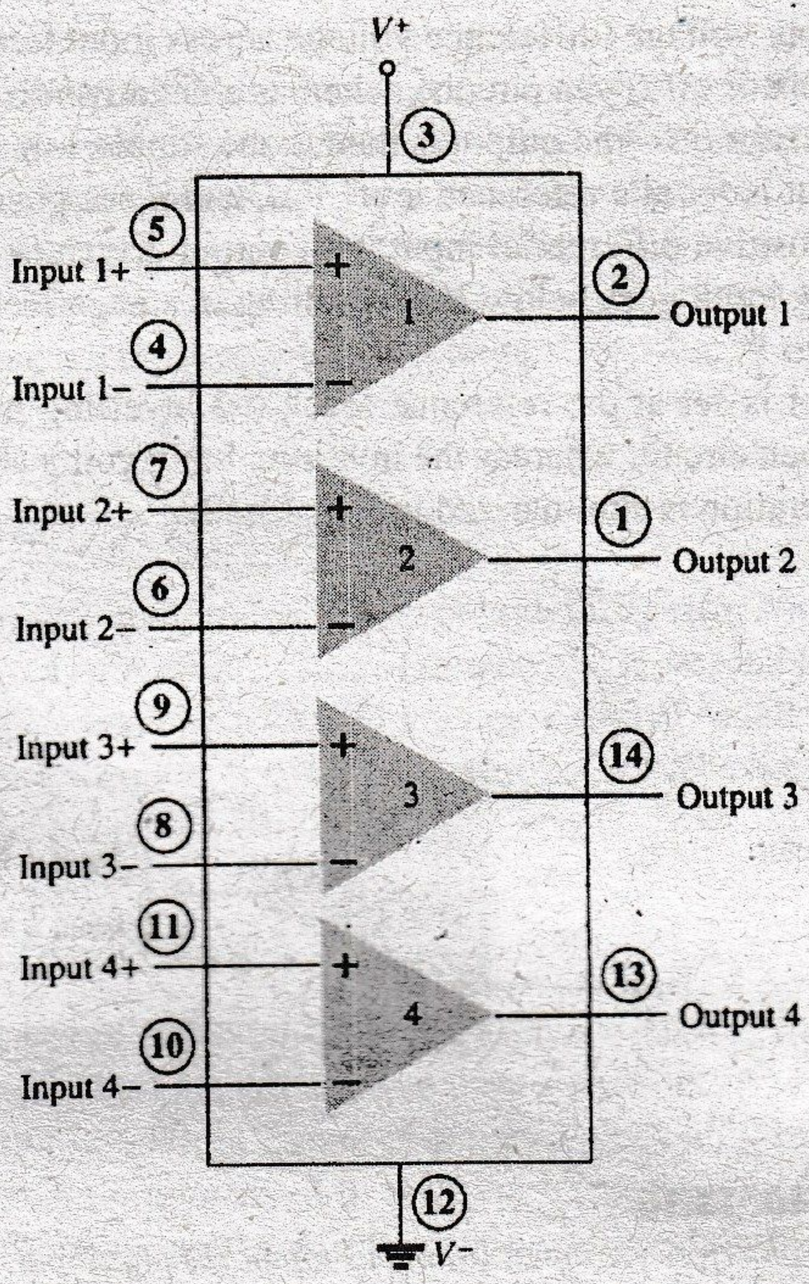


FIG. 13.8
Quad comparator IC (339).

To see how these comparator circuits can be used, Fig. 13.9 shows one of the 339 comparator circuits connected as a zero-crossing detector. Whenever the input signal goes above 0 V, the output switches to V^+. The input switches to V^- only when the input goes below 0 V. The circled numbers show the IC pins.

A reference level other than 0 V can also be used, and either input terminal could be used as the reference, the other terminal then being connected to the input signal. The operation of one of the comparator circuits is described next.

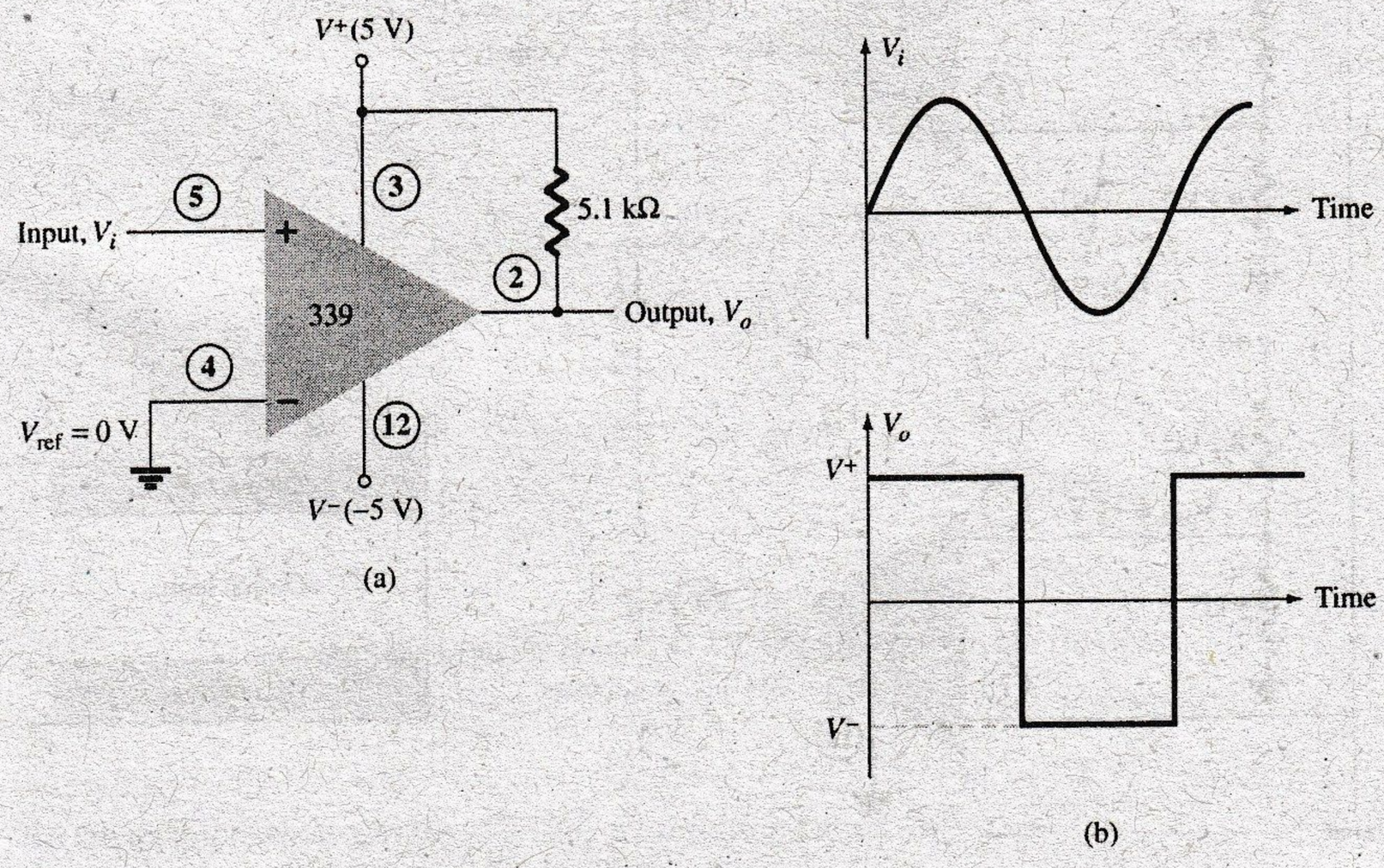


FIG. 13.9
Operation of one 339 comparator circuit as a zero-crossing detector.

The differential input voltage (difference voltage across input terminals) going positive drives the output transistor off (open circuit), whereas a negative differential input voltage drives the output transistor on—the output is then at the supply low level.

If the negative input is set at a reference level V_{ref}, and if the positive input goes above V_{ref}, this results in a positive differential input with output driven to the open-circuit state. When the noninverting input goes below V_{ref}, resulting in a negative differential input, the output will be driven to V^-.

If the positive input is set at the reference level, the inverting input going below V_{ref} results in the output open circuit, whereas the inverting input going above V_{ref} results in the output at V^-. This operation is summarized in Fig. 13.10.

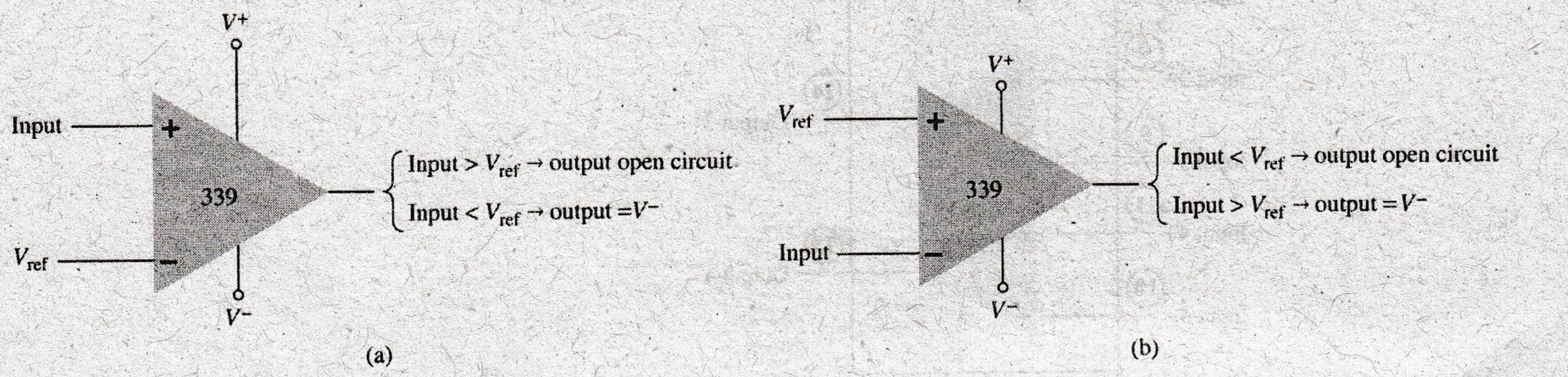


FIG. 13.10

Operation of a 339 comparator circuit with reference input: (a) minus input; (b) plus input.

Since the output of one of these comparator circuits is from an open-circuit collector, applications in which the outputs from more than one circuit can be wire-ORed are possible. Figure 13.11 shows two comparator circuits connected with common output and also with common input. Comparator 1 has a +5-V reference voltage input connected to the

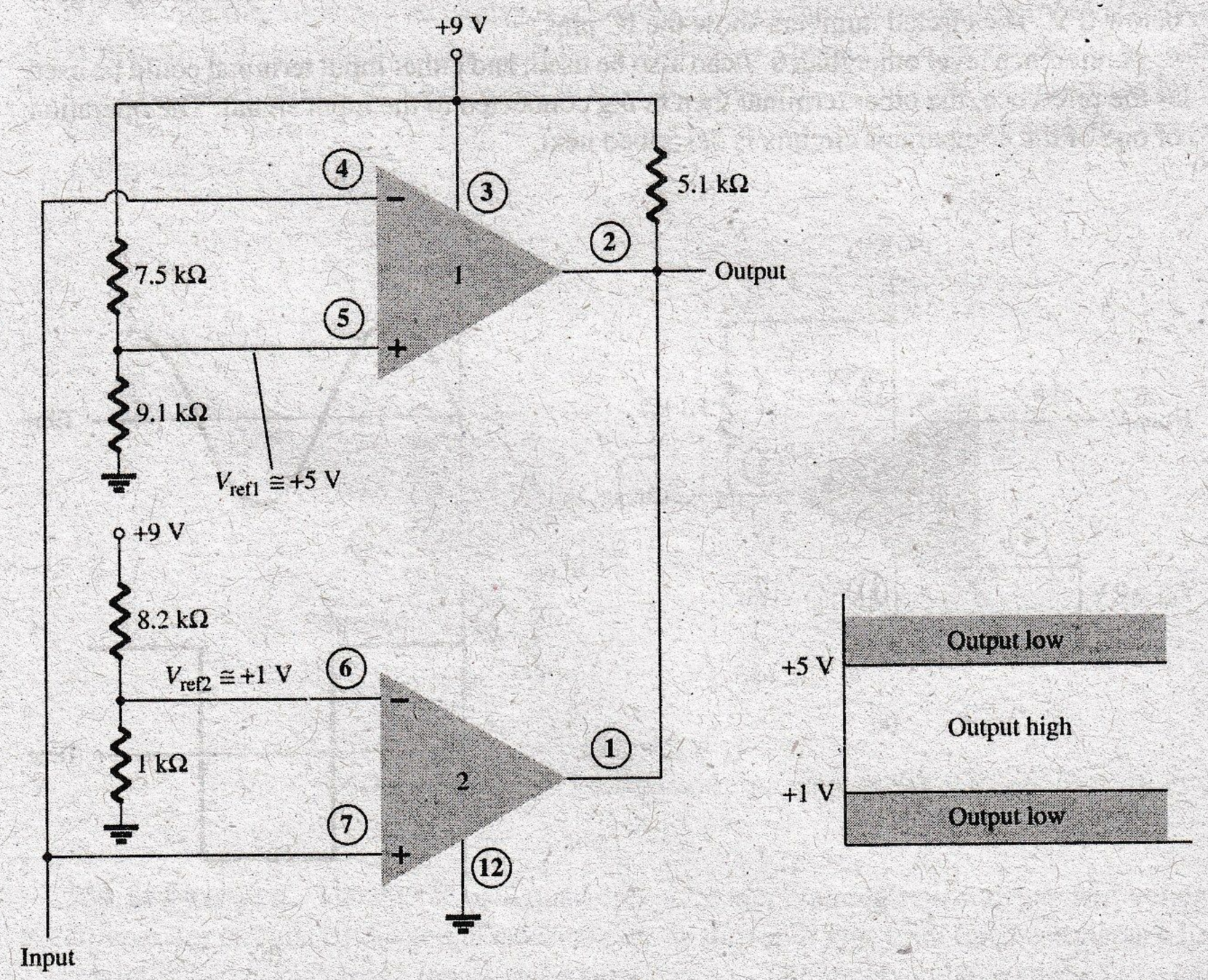


FIG. 13.11

Operation of two 339 comparator circuits as a window detector.

noninverting input. The output will be driven low by comparator 1 when the input signal goes above +5 V. Comparator 2 has a reference voltage of +1 V connected to the inverting input. The output of comparator 2 will be driven low when the input signal goes below +1 V. In total, the output will go low whenever the input is below +1 V or above +5 V, as shown in Fig. 13.11, the overall operation being that of a voltage window detector. The high output indicates that the input is within a voltage window of +1 to +5 V (these values being set by the reference voltage levels used).

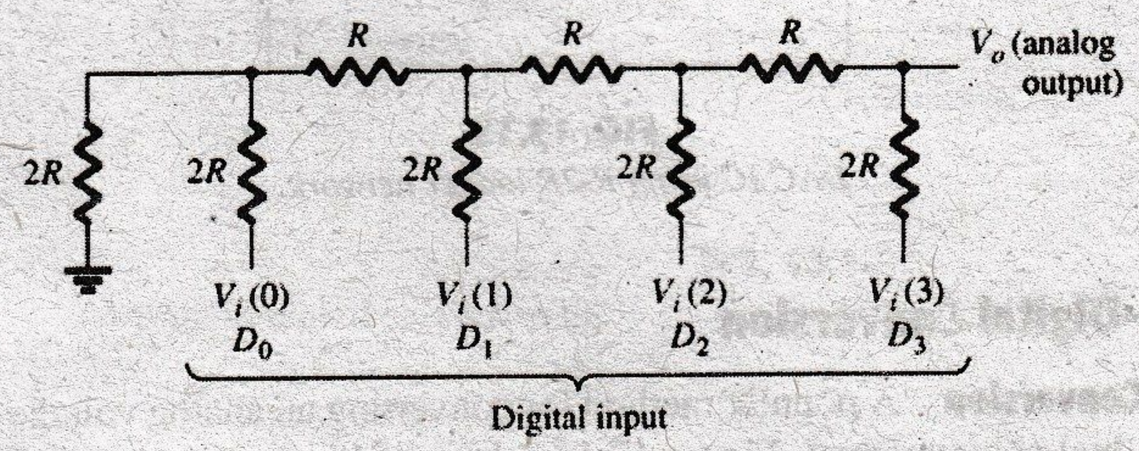
13.3 DIGITAL–ANALOG CONVERTERS

Many voltages and currents in electronics vary continuously over some range of values. In digital circuitry the signals are at either one of two levels, representing the binary values of 1 or 0. An analog–digital converter (ADC) obtains a digital value representing an input analog voltage, whereas a digital–analog converter (DAC) changes a digital value back into an analog voltage.

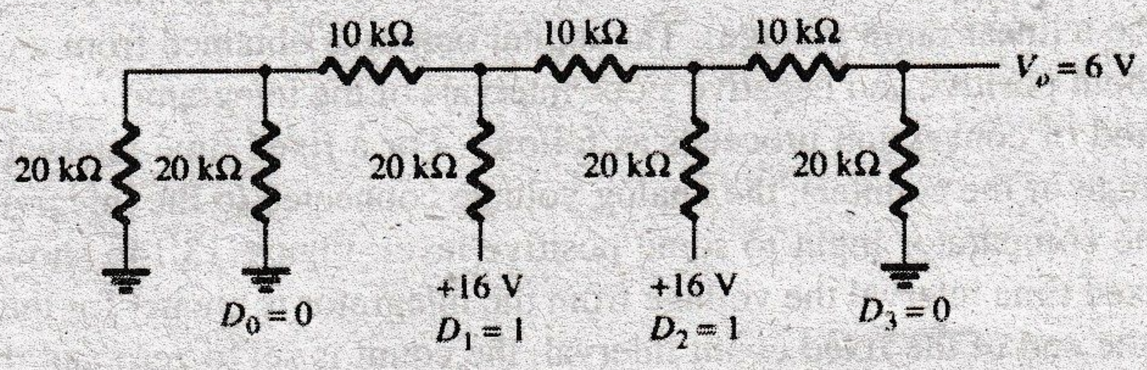
Digital-to-Analog Conversion

Ladder Network Conversion Digital-to-analog conversion can be achieved using a number of different methods. One popular scheme uses a network of resistors called a *ladder network.* A ladder network accepts inputs of binary values at, typically, 0 V or V_{ref} and provides an output voltage proportional to the binary input value. Figure 13.12a shows a ladder network with four input voltages, representing 4 bits of digital data and a dc voltage output. The output voltage is proportional to the digital input value as given by the relation

$$V_o = \frac{D_0 \times 2^0 + D_1 \times 2^1 \times D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{ref} \qquad \textbf{(13.1)}$$



(a)



(b)

FIG. 13.12
Four-stage ladder network used as a DAC: (a) basic circuit; (b) circuit example with 0110 input.

In the example shown in Fig. 13.12b, the resulting output voltage is

$$V_o = \frac{0 \times 1 + 1 \times 2 + 1 \times 4 + 0 \times 8}{16}(16\text{ V}) = 6\text{ V}$$

Therefore, 0110_2 digital converts to 6 V analog.

The function of the ladder network is to convert the 16 possible binary values from 0000 to 1111 into one of 16 voltage levels in steps of $V_{ref}/16$. Using more sections of the ladder allows us to have more binary inputs and a greater quantization for each step. For example, a 10-stage ladder network could extend the number of voltage steps or the voltage resolution to $V_{ref}/2^{10}$, or $V_{ref}/1024$. A reference voltage of $V_{ref} = 10$ V would then provide output voltage steps of 10 V/1024, or approximately 10 mV. More ladder stages provide greater voltage resolution. In general, the voltage resolution for n ladder stages is

$$\boxed{\frac{V_{ref}}{2^n}} \tag{13.2}$$

Figure 13.13 shows a block diagram of a typical DAC using a ladder network. The ladder network, referred to in the diagram as an *R-2R ladder*, is sandwiched between the reference current supply and current switches connected to each binary input, the resulting output current being proportional to the input binary value. The binary input turns on selected legs of the ladder, the output current being a weighted summing of the reference current. Connecting the output current through a resistor will produce an analog voltage if desired.

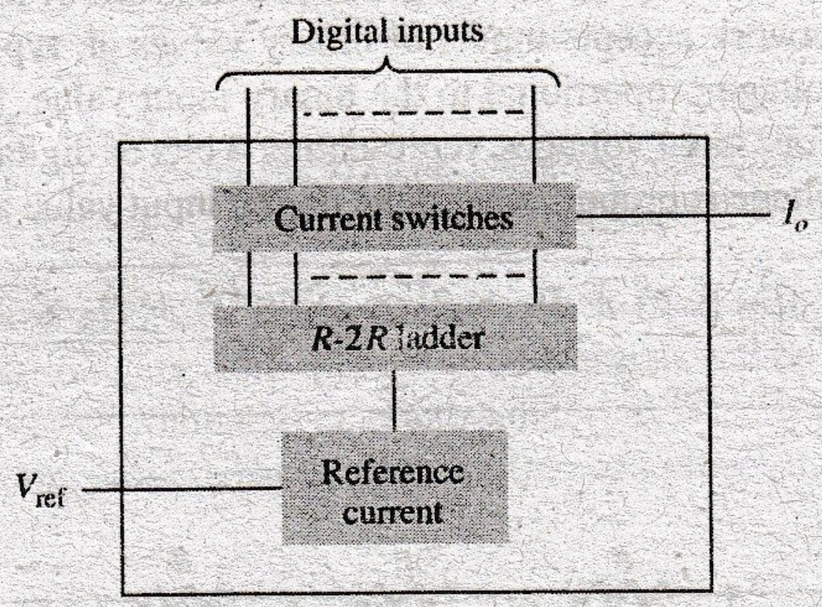


FIG. 13.13
DAC IC using R-2R ladder network.

Analog-to-Digital Conversion

Dual-Slope Conversion A popular method for converting an analog voltage into a digital value is the dual-slope method. Figure 13.14a shows a block diagram of the basic dual-slope converter. The analog voltage to be converted is applied through an electronic switch to an integrator or ramp-generator circuit (essentially a constant current charging a capacitor to produce a linear ramp voltage). The digital output is obtained from a counter operated during both positive and negative slope intervals of the integrator.

The method of conversion proceeds as follows. For a fixed time interval (usually the full count range of the counter), the analog voltage connected to the integrator raises the voltage at the comparator input to some positive level. Figure 13.14b shows that at the end of the fixed time interval the voltage from the integrator is greater for the larger input voltage. At the end of the fixed count interval, the count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage. The integrator output (or capacitor input) then decreases at a fixed rate. The counter advances during this time, whereas the integrator's output decreases at a fixed rate until it drops below the comparator reference voltage, at which time the control logic receives a signal (the comparator output) to stop the count. The digital value stored in the counter is then the digital output of the converter.

Using the same clock and integrator to perform the conversion during positive and negative slope intervals tends to compensate for clock frequency drift and integrator accuracy limitations. Setting the reference input value and clock rate can scale the counter output as desired. The counter can be a binary, BCD, or other form of digital counter, if desired.

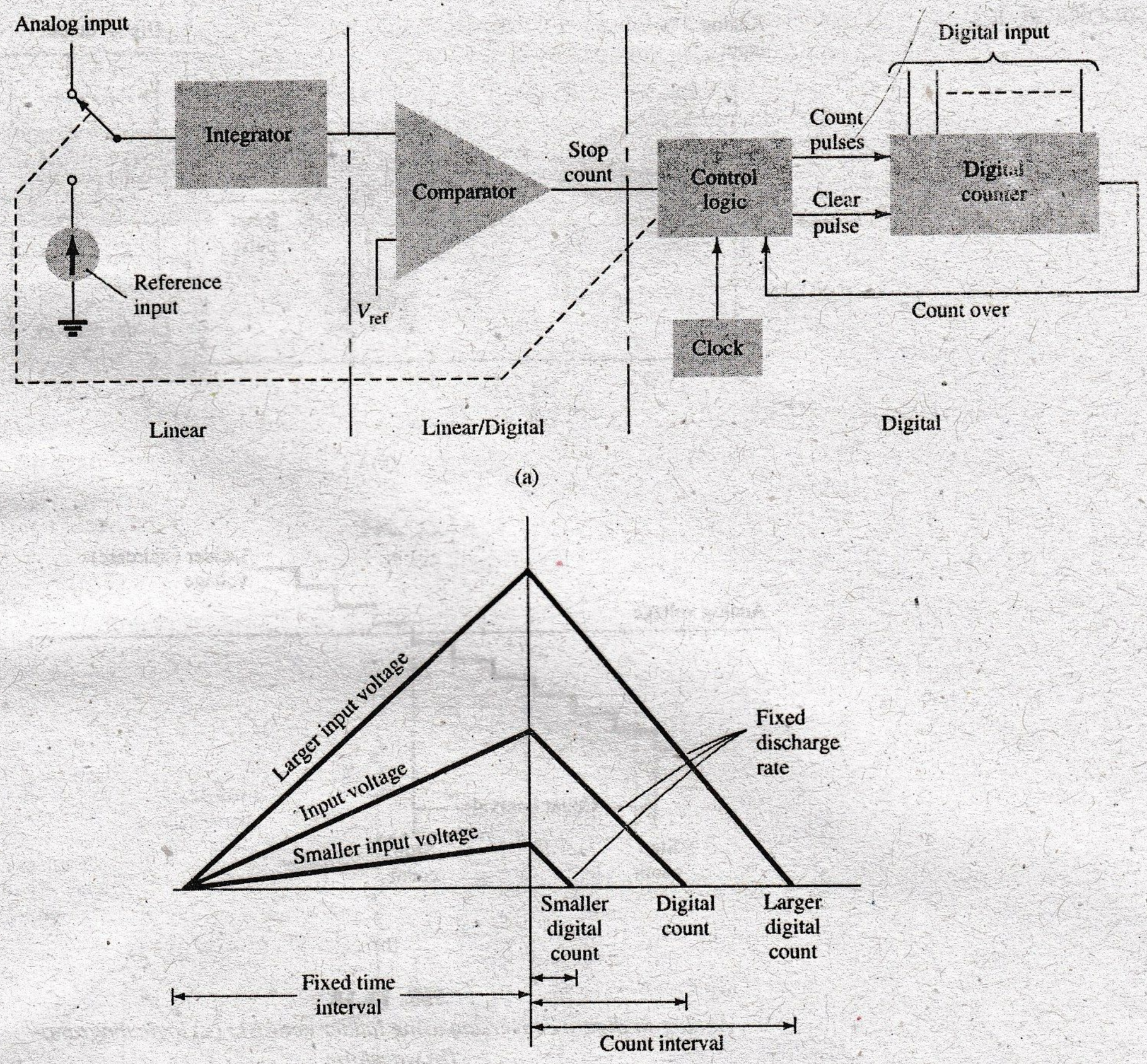


FIG. 13.14

Analog-to-digital conversion using dual-slope method: (a) logic diagram; (b) waveform.

Ladder-Network Conversion Another popular method of analog-to-digital conversion uses a ladder network along with counter and comparator circuits (see Fig. 13.15). A digital counter advances from a zero count while a ladder network driven by the counter outputs a staircase voltage, as shown in Fig. 13.15b, which increases one voltage increment for each count step. A comparator circuit, receiving both staircase voltage and analog input voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage. The counter value at that time is the digital output.

The amount of voltage change stepped by the staircase signal depends on the number of count bits used. A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V steps each count by a voltage of

$$\frac{V_{ref}}{2^{12}} = \frac{10\text{ V}}{4096} = 2.4\text{ mV}$$

This results in a conversion resolution of 2.4 mV. The clock rate of the counter affects the time required to carry out a conversion. A clock rate of 1 MHz operating a 12-stage counter needs a maximum conversion time of

$$4096 \times 1\ \mu\text{s} = 4096\ \mu\text{s} \approx 4.1\text{ ms}$$

The minimum number of conversions that could be carried out each second is then

$$\text{number of conversions} = 1/4.1\text{ ms} \approx 244\text{ conversions/second}$$

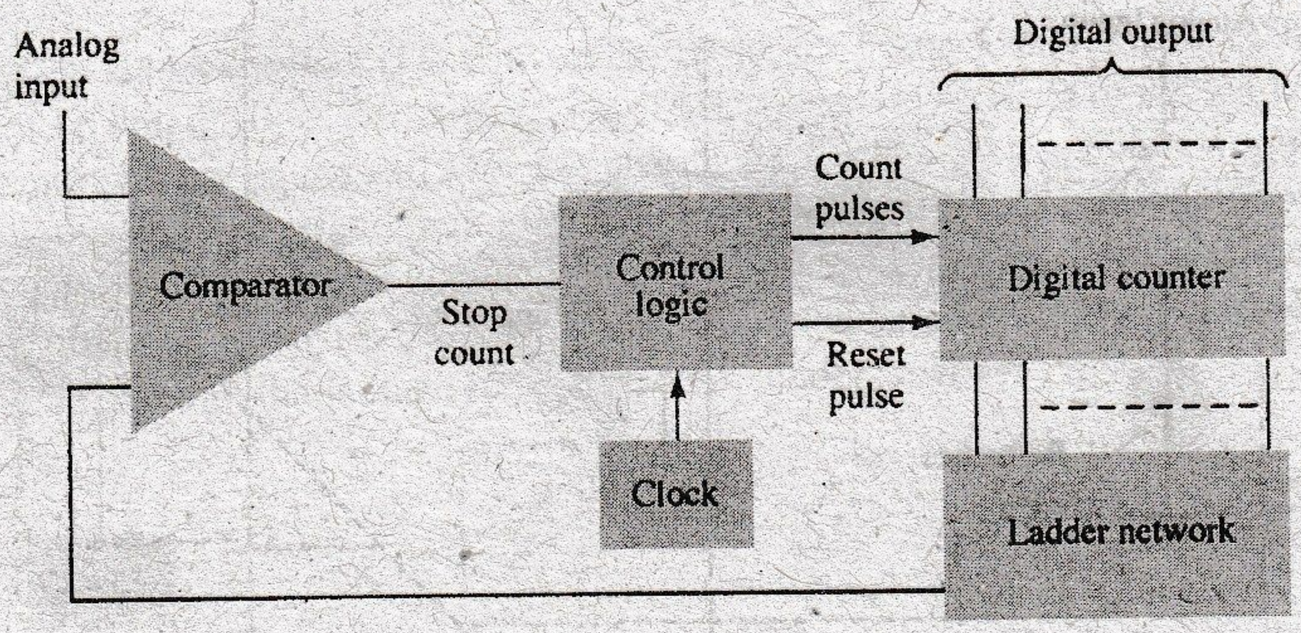


FIG. 13.15
Analog-to-digital conversion using ladder network: (a) logic diagram; (b) waveform.

Since on the average, with some conversions requiring little count time and others near-maximum count time, a conversion time of 4.1 ms/2 = 2.05 ms is needed, and the average number of conversions is 2 × 244 = 488 conversions/second. A slower clock rate would result in fewer conversions per second. A converter using fewer count stages (and less conversion resolution) would carry out more conversions per second. The conversion accuracy depends on the accuracy of the comparator.

13.4 TIMER IC UNIT OPERATION

Another popular analog–digital integrated circuit is the versatile 555 timer. The IC is made of a combination of linear comparators and digital flip-flops as described in Fig. 13.16. The entire circuit is usually housed in an eight-pin package as specified in Fig. 13.16. A series connection of three resistors sets the reference voltage levels to the two comparators at $2V_{CC}/3$ and $V_{CC}/3$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output amplifier stage. The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor.

Astable Operation

One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. The following analysis of the operation of the 555 as an astable circuit includes details of the different parts of the unit and how the various inputs and outputs are used. Figure 13.17 shows an astable circuit built using an external resistor and capacitor to set the timing interval of the output signal.

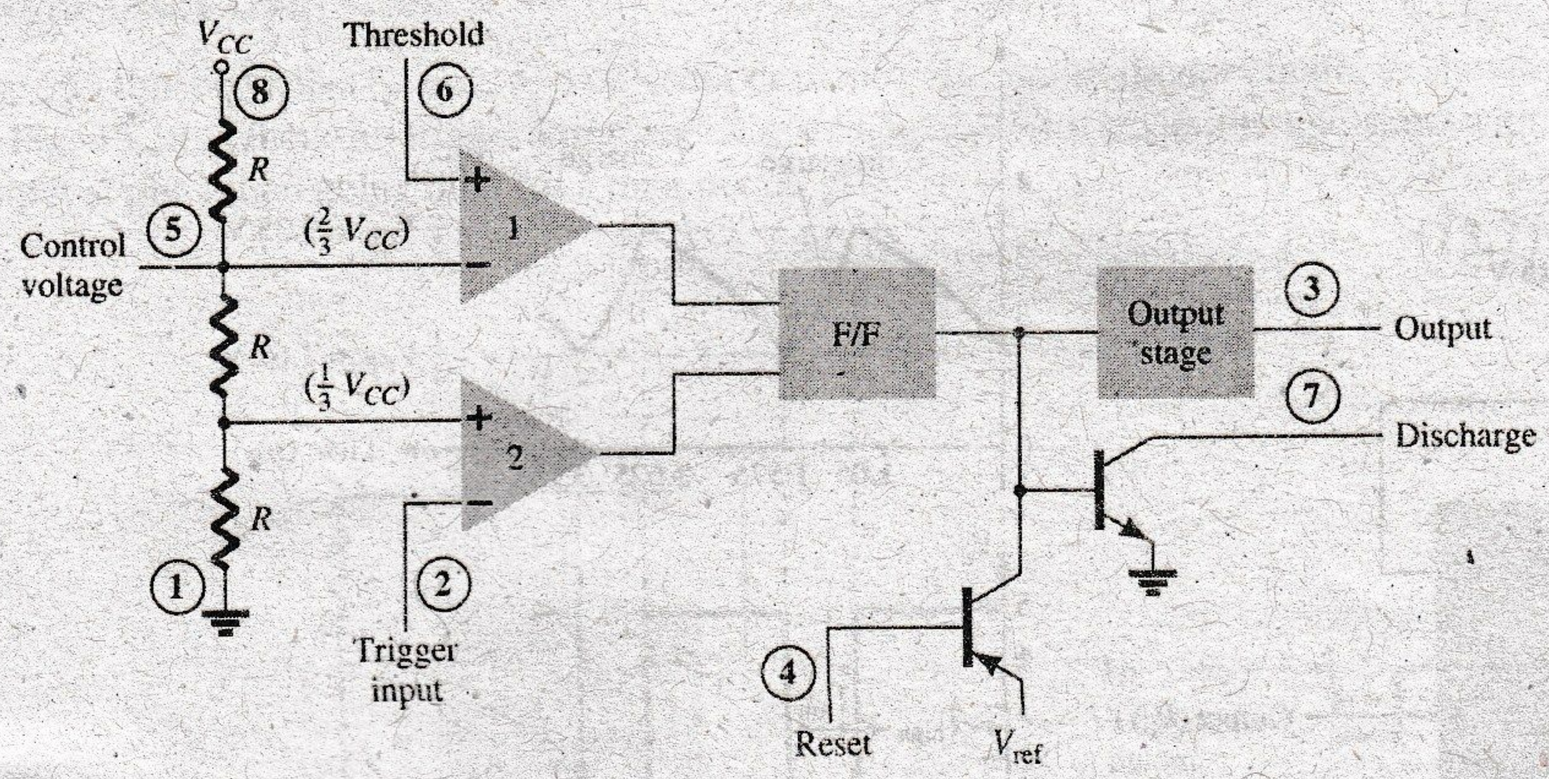


FIG. 13.16
Details of 555 timer IC.

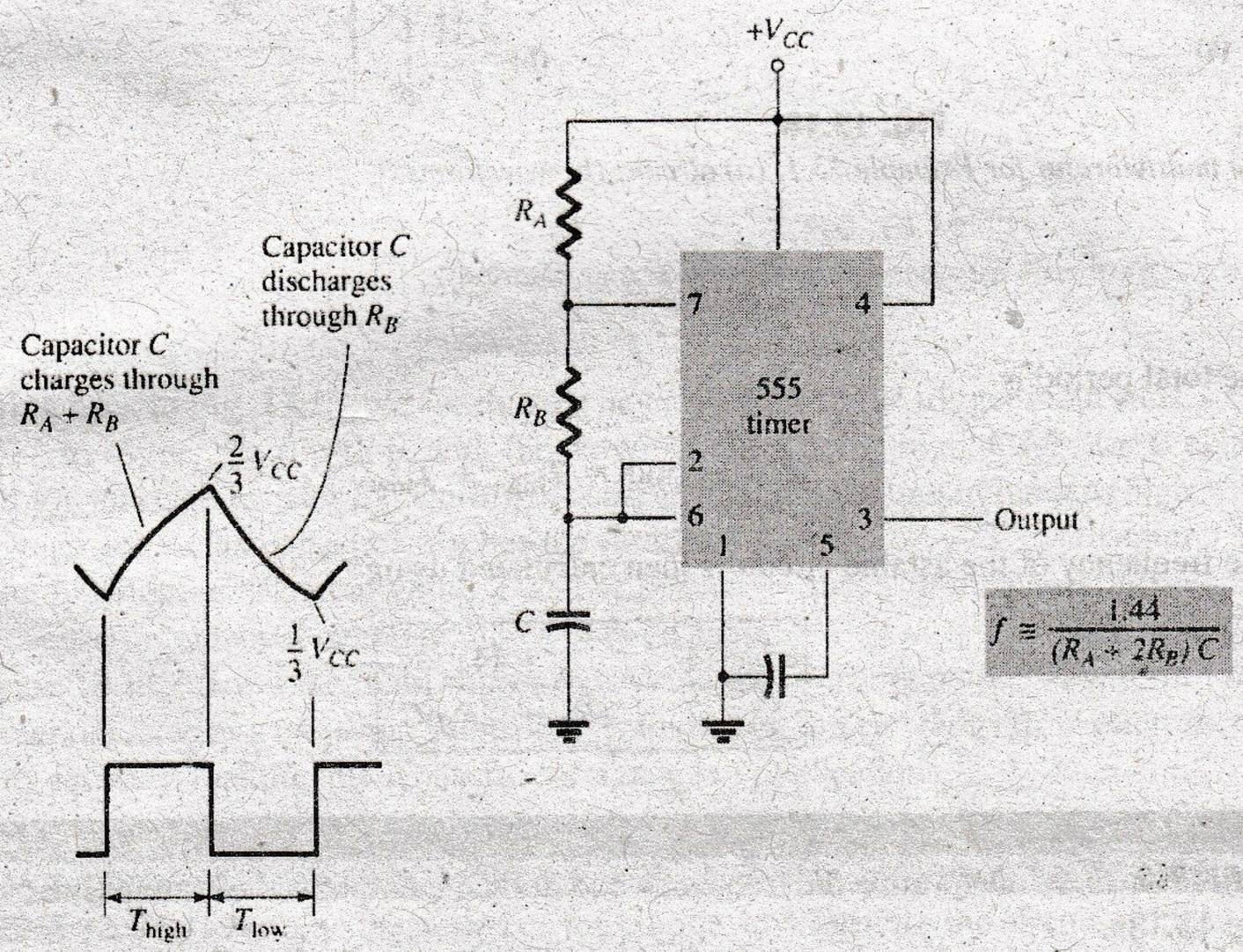


FIG. 13.17
Astable multivibrator using 555 IC.

Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to Fig. 13.17, we see that the capacitor voltage rises until it goes above $2V_{CC}/3$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level ($V_{CC}/3$). The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B toward V_{CC}.

Figure 13.18a shows the capacitor and output waveforms resulting from the astable circuit. Calculation of the time intervals during which the output is high and low can be made using the relations

$$T_{high} \approx 0.7(R_A + R_B)C \tag{13.3}$$

$$T_{low} \approx 0.7R_BC \tag{13.4}$$

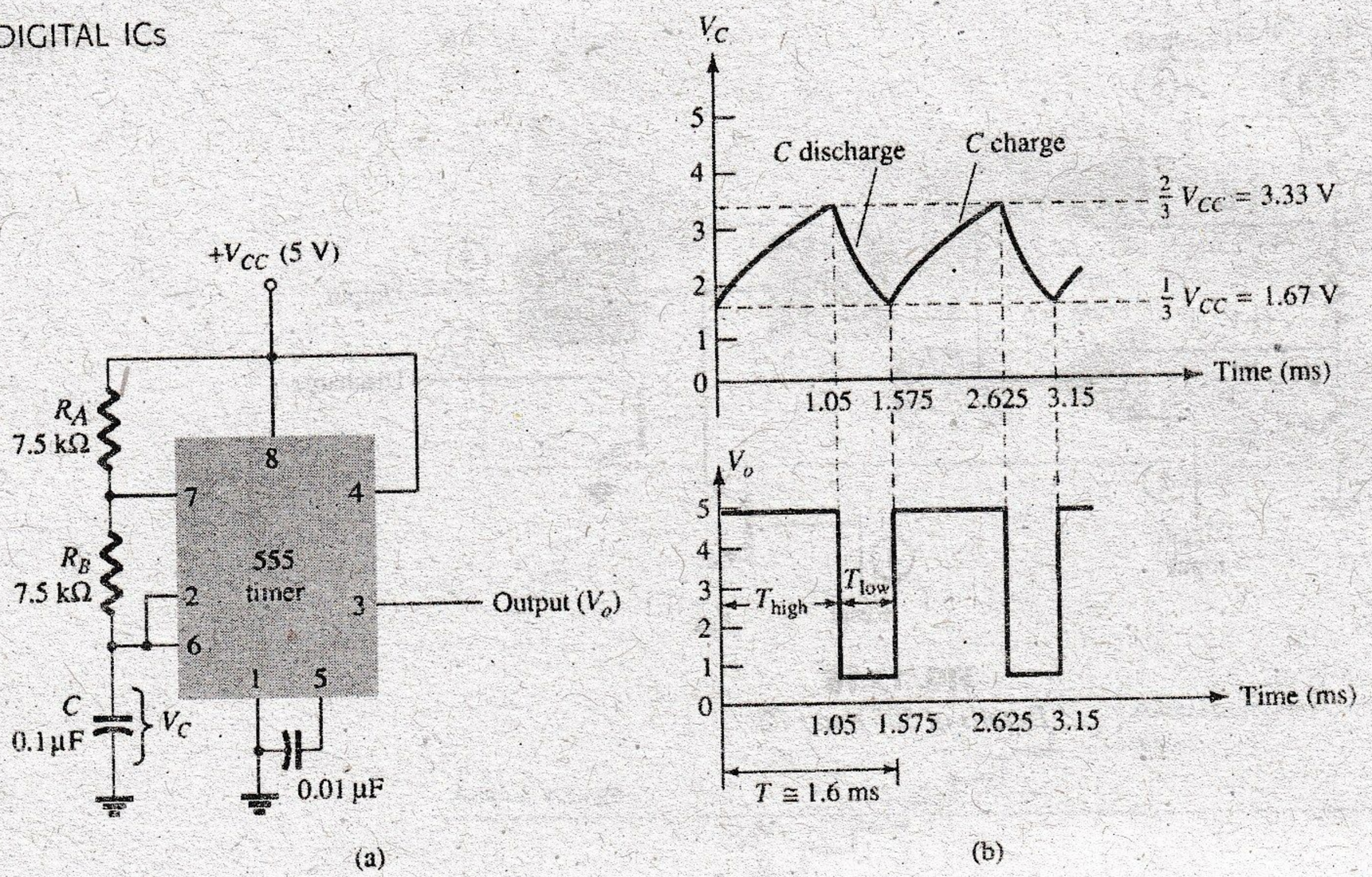


FIG. 13.18
Astable multivibrator for Example 13.1: (a) circuit; (b) waveforms.

The total period is

$$T = \text{period} = T_{\text{high}} + T_{\text{low}} \tag{13.5}$$

The frequency of the astable circuit is then calculated using*

$$f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B)C} \tag{13.6}$$

EXAMPLE 13.1 Determine the frequency and draw the output waveform for the circuit of Fig. 13.18a.

Solution: Using Eqs. (13.3) through (13.6) yields

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5 \times 10^3 + 7.5 \times 10^3)(0.1 \times 10^{-6})$$
$$= 1.05 \text{ ms}$$
$$T_{\text{low}} = 0.7R_BC = 0.7(7.5 \times 10^3)(0.1 \times 10^{-6}) = 0.525 \text{ ms}$$
$$T = T_{\text{high}} + T_{\text{low}} = 1.05 \text{ ms} + 0.525 \text{ ms} = 1.575 \text{ ms}$$
$$f = \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} \approx \mathbf{635 \text{ Hz}}$$

The waveforms are drawn in Fig. 13.18b.

*The period can be directly calculated from

$$T = 0.693(R_A + 2R_B)C \approx 0.7(R_A + 2R_B)C$$

and the frequency from

$$f \approx \frac{1.44}{(R_A + 2R_B)C}$$

Monostable Operation

The 555 timer can also be used as a one-shot or monostable multivibrator circuit, as shown in Fig. 13.19. When the trigger input signal goes negative, it triggers the one-shot, with output at pin 3 then going high for a time period given by

$$T_{high} = 1.1R_AC \tag{13.7}$$

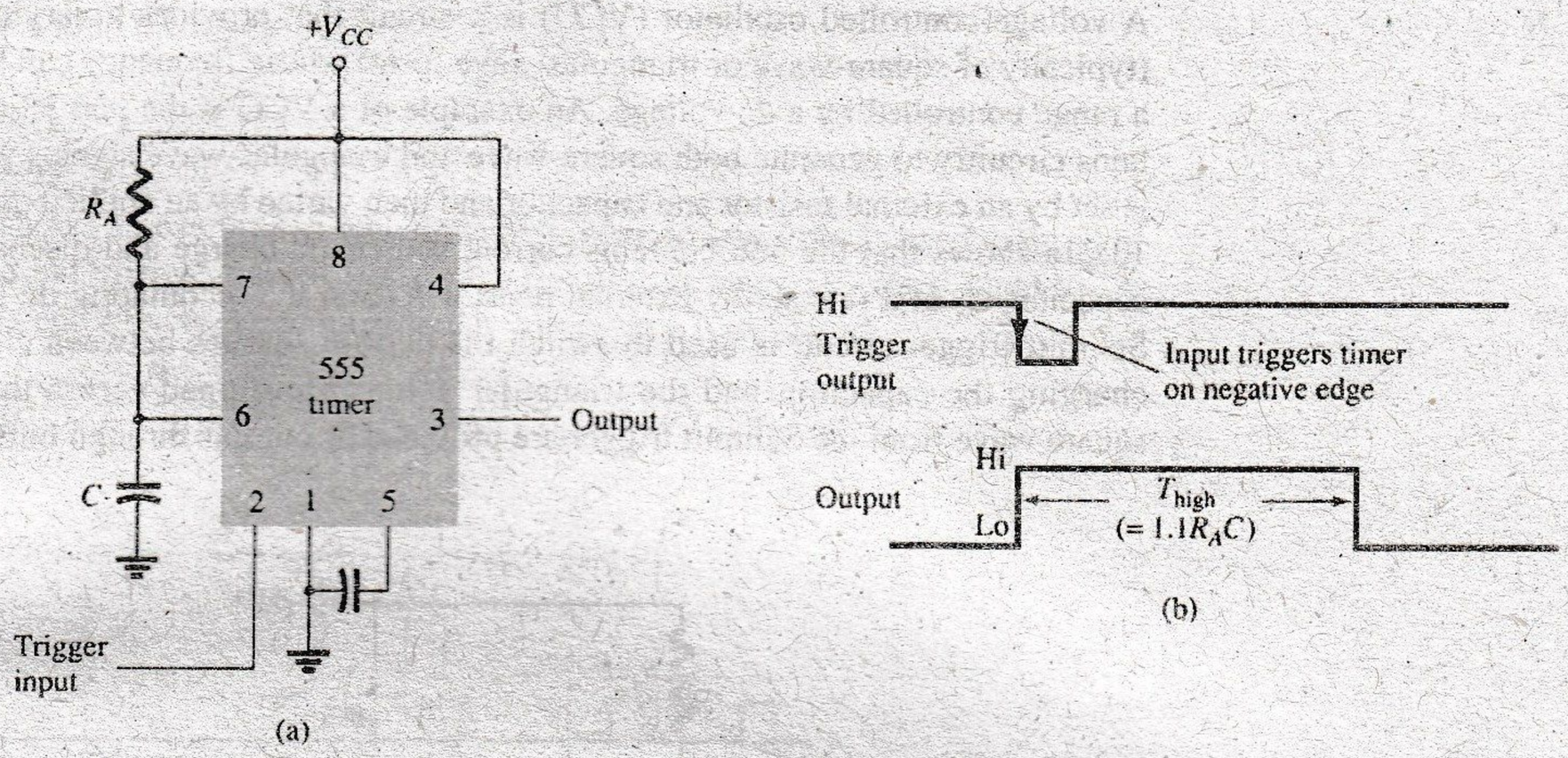


FIG. 13.19
Operation of 555 timer as a one-shot: (a) circuit; (b) waveforms.

Referring back to Fig. 13.16, we see that the negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high. Capacitor C charges toward V_{CC} through resistor R_A. During the charge interval, the output remains high. When the voltage across the capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers the flip-flop, with output going low. The discharge transistor also goes low, causing the capacitor to remain at near 0 V until triggered again.

Figure 13.19b shows the input trigger signal and the resulting output waveform for the 555 timer operated as a one-shot. Time periods for this circuit can range from microseconds to many seconds, making this IC useful for a range of applications.

EXAMPLE 13.2 Determine the period of the output waveform for the circuit of Fig. 13.20 when triggered by a negative pulse.

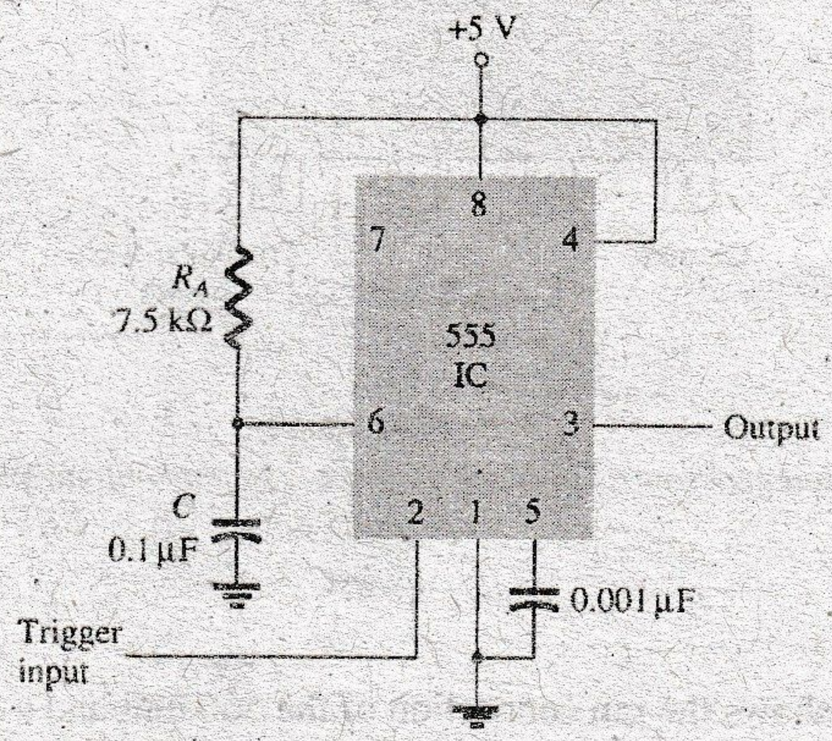


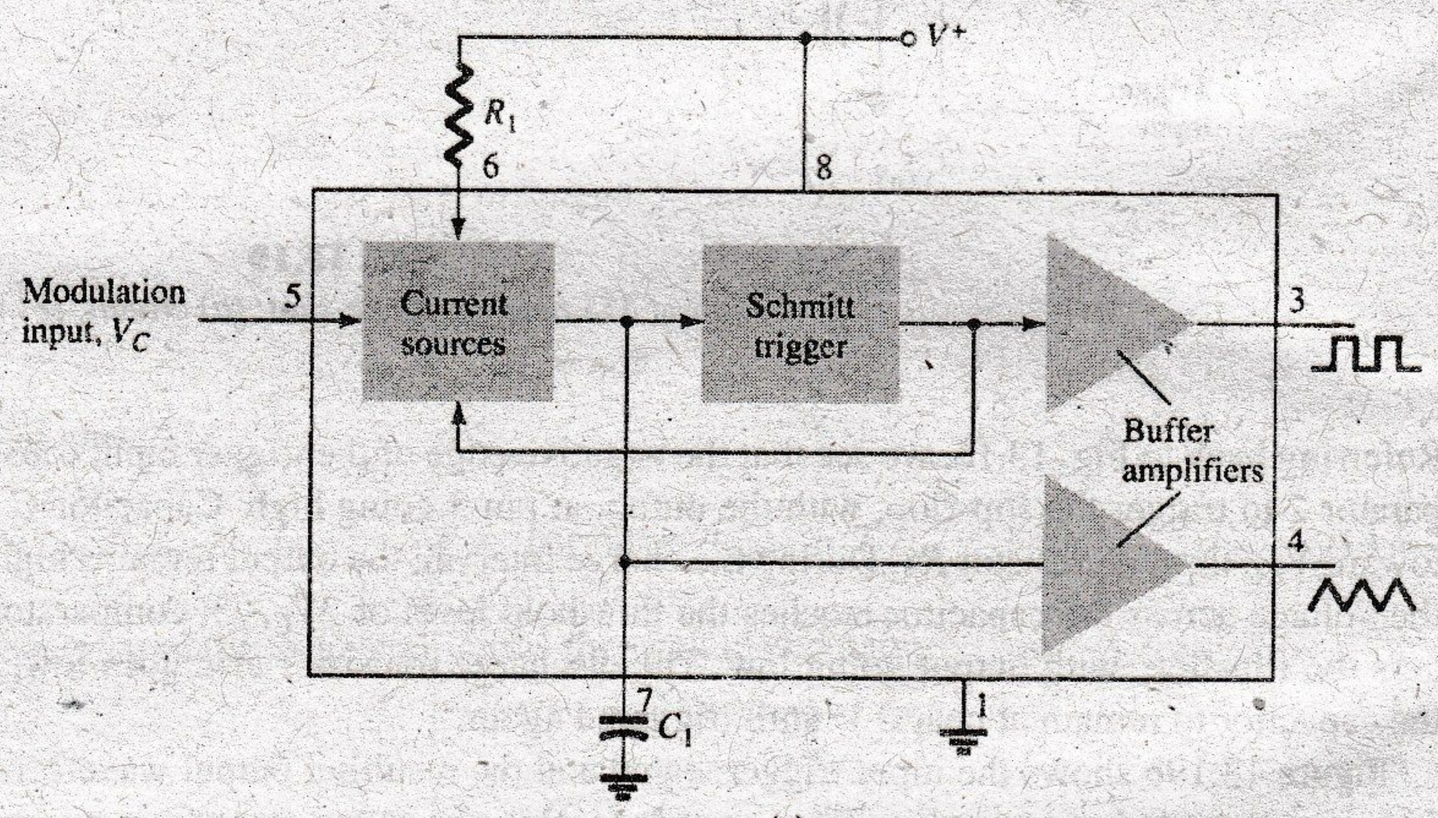
FIG. 13.20
Monostable circuit for Example 13.2.

Solution: Using Eq. (13.7), we obtain

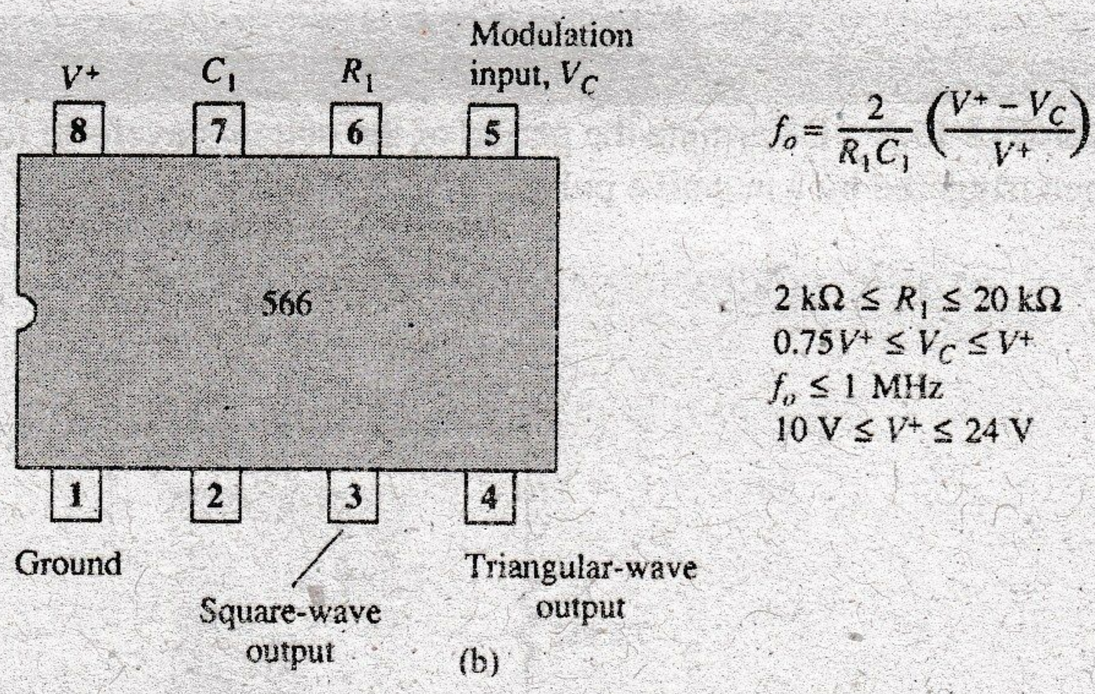
$$T_{\text{high}} = 1.1R_AC = 1.1(7.5 \times 10^3)(0.1 \times 10^{-6}) = \mathbf{0.825\ ms}$$

13.5 VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage. An example of a VCO is the 566 IC unit, which contains circuitry to generate both square-wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage. Figure 13.21a shows that the 566 contains current sources to charge and discharge an external capacitor C_1 at a rate set by external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is used to switch the current sources between charging and discharging the capacitor, and the triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers.



(a)



(b)

$$f_o = \frac{2}{R_1C_1}\left(\frac{V^+ - V_C}{V^+}\right)$$

$2\ \text{k}\Omega \le R_1 \le 20\ \text{k}\Omega$
$0.75V^+ \le V_C \le V^+$
$f_o \le 1\ \text{MHz}$
$10\ \text{V} \le V^+ \le 24\ \text{V}$

FIG. 13.21

A 566 function generator: (a) block diagram; (b) pin configuration and summary of operating data.

Figure 13.21b shows the pin connection of the 566 unit and a summary of formula and value limitations. The oscillator can be programmed over a 10-to-1 frequency range by proper selection of an external resistor and capacitor, and then modulated over a 10-to-1 frequency range by a control voltage V_C.

A free-running or center-operating frequency f_o can be calculated from

$$f_o = \frac{2}{R_1 C_1}\left(\frac{V^+ - V_C}{V^+}\right) \tag{13.8}$$

with the following practical circuit value restrictions:

1. R_1 should be within the range $2\,\text{k}\Omega \leq R_1 \leq 20\,\text{k}\Omega$.
2. V_C should be within the range $\frac{3}{4}V^+ \leq V_C \leq V^+$.
3. f_o should be below 1 MHz.
4. V^+ should range between 10 V and 24 V.

Figure 13.22 shows an example in which the 566 function generator is used to provide both square-wave and triangular-wave signals at a fixed frequency set by R_1, C_1, and V_C. A resistor divider R_2 and R_3 sets the dc modulating voltage at a fixed value

$$V_C = \frac{R_3}{R_2 + R_3}V^+ = \frac{10\,\text{k}\Omega}{1.5\,\text{k}\Omega + 10\,\text{k}\Omega}(12\,\text{V}) = 10.4\,\text{V}$$

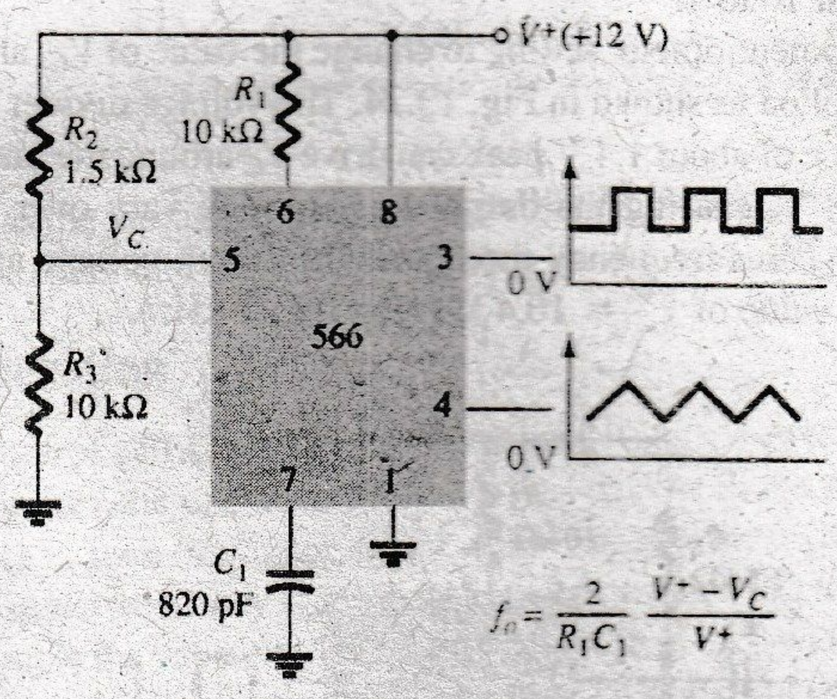


FIG. 13.22
Connection of a 566 VCO unit.

(which falls properly in the voltage range $0.75V^+ = 9\,\text{V}$ and $V^+ = 12\,\text{V}$). Using Eq. (13.8) yields

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})}\left(\frac{12 - 10.4}{12}\right) \approx 32.5\,\text{kHz}$$

The circuit of Fig. 13.23 shows how the output square-wave frequency can be adjusted using the input voltage V_C to vary the signal frequency. Potentiometer R_3 allows varying V_C

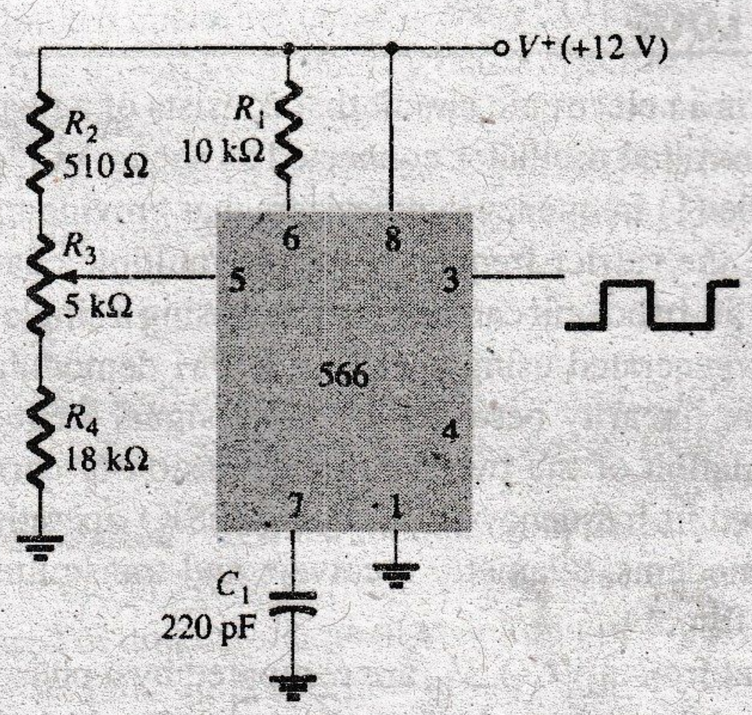


FIG. 13.23
Connection of a 566 as a VCO unit.

from about 9 V to near 12 V, over the full 10-to-1 frequency range. With the potentiometer wiper set at the top, the control voltage is

$$V_C = \frac{R_3 + R_4}{R_2 + R_3 + R_4}(V^+) = \frac{5\,\text{k}\Omega + 18\,\text{k}\Omega}{510\,\Omega + 5\,\text{k}\Omega + 18\,\text{k}\Omega}(+12\,\text{V}) = 11.74\,\text{V}$$

resulting in a lower output frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 11.74}{12}\right) \approx 19.7\,\text{kHz}$$

With the wiper arm of R_3 set at the bottom, the control voltage is

$$V_C = \frac{R_4}{R_2 + R_3 + R_4}(V^+) = \frac{18\,\text{k}\Omega}{510\,\Omega + 5\,\text{k}\Omega + 18\,\text{k}\Omega}(+12\,\text{V}) = 9.19\,\text{V}$$

resulting in an upper frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 9.19}{12}\right) \approx 212.9\,\text{kHz}$$

The frequency of the output square wave can then be varied using potentiometer R_3 over a frequency range of at least 10 to 1.

Rather than varying a potentiometer setting to change the value of V_C, an input modulating voltage V_{in} can be applied as shown in Fig. 13.24. The voltage divider sets V_C at about 10.4 V. An input ac voltage of about 1.4 V peak can drive V_C around the bias point between voltages of 9 V and 11.8 V, causing the output frequency to vary over about a 10-to-1 range. The input signal V_{in} thus frequency-modulates the output voltage around the center frequency set by the bias value of $V_C = 10.4$ V ($f_o = 121.2$ kHz).

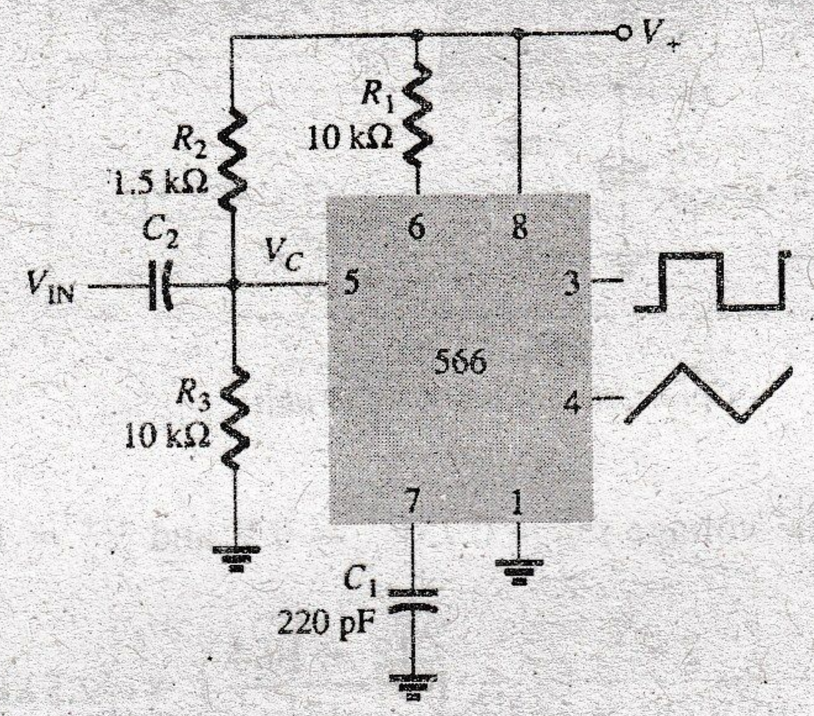


FIG. 13.24
Operation of a VCO with frequency-modulating input.

13.6 PHASE-LOCKED LOOP

A phase-locked loop (PLL) is an electronic circuit that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator connected as shown in Fig. 13.25. Common applications of a PLL include (1) frequency synthesizers that provide multiples of a reference signal frequency [e.g., the carrier frequency for the multiple channels of a citizens band (CB) unit or marine-radio-band unit can be generated using a single-crystal-controlled frequency and its multiples generated using a PLL], (2) FM demodulation networks for FM operation with excellent linearity between the input signal frequency and the PLL output voltage, (3) demodulation of the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (FSK) operation, and (4) a wide variety of areas including modems, telemetry receivers and transmitters, tone decoders, AM detectors, and tracking filters.

An input signal V_i and that from a VCO, V_o, are compared by a phase comparator (refer to Fig. 13.25), providing an output voltage V_e that represents the phase difference between the two signals. This voltage is then fed to a low-pass filter, which provides an output voltage (amplified if necessary) that can be taken as the output voltage from the PLL and is

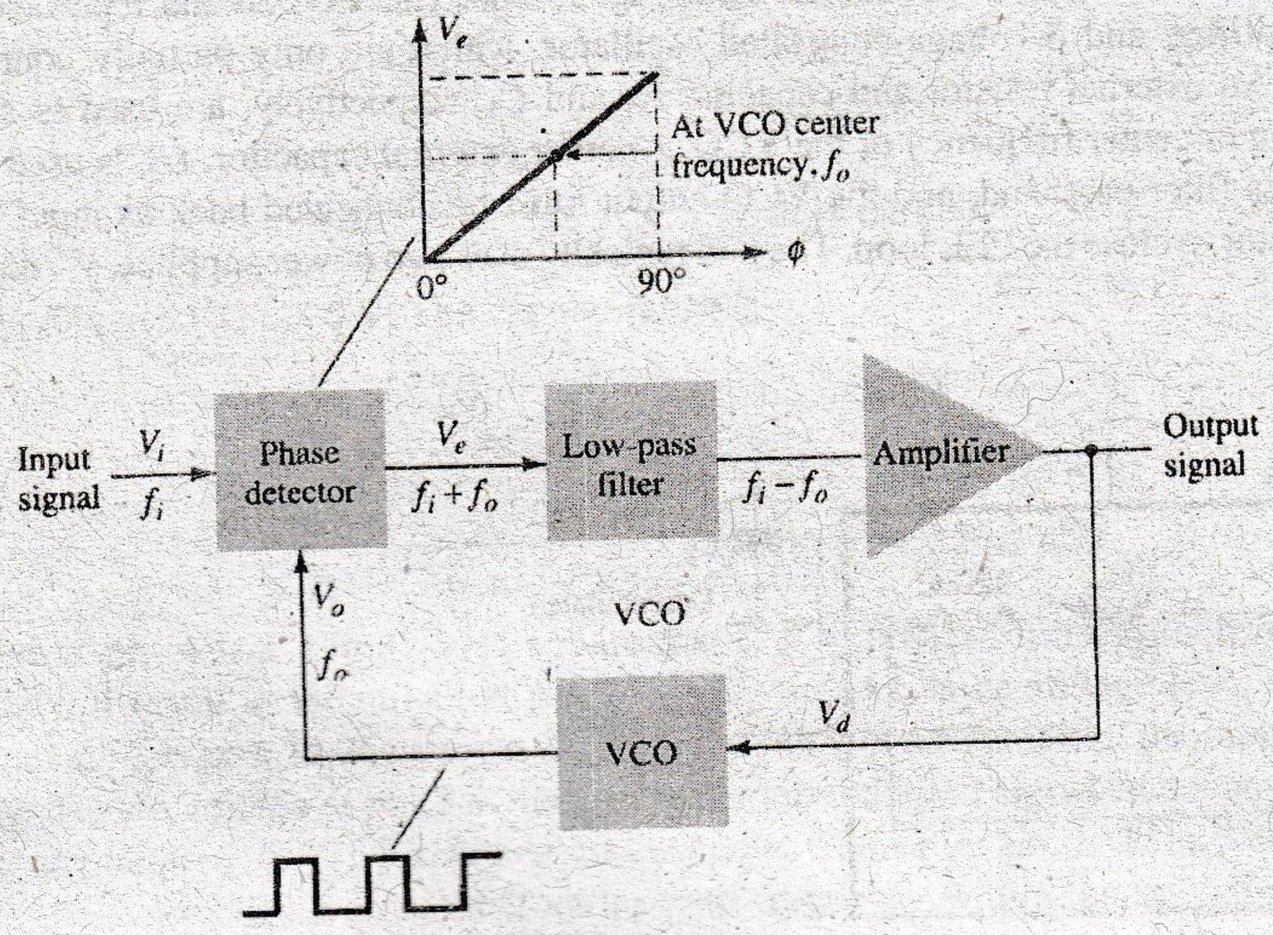


FIG. 13.25
Block diagram of basic phase-locked loop (PLL).

used internally as the voltage to modulate the VCO's frequency. The closed-loop operation of the circuit is to maintain the VCO frequency locked to that of the input signal frequency.

Basic PLL Operation

The basic operation of a PLL circuit can be explained using the circuit of Fig. 13.25 as reference. We will first consider the operation of the various circuits in the phase-locked loop when the loop is operating in lock (the input signal frequency and the VCO frequency are the same). When the input signal frequency is the same as that from the VCO to the comparator, the voltage V_d taken as output is the value needed to hold the VCO in lock with the input signal. The VCO then provides output of a fixed-amplitude square-wave signal at the frequency of the input. Best operation is obtained if the VCO center frequency f_o is set with the dc bias voltage midway in its linear operating range. The amplifier allows this adjustment in dc voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the comparator are of the same frequency, although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO. Changes in the input signal frequency then result in change in the dc voltage to the VCO. Within a capture-and-lock frequency range, the dc voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the phase comparator contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower frequency component of the signal, so that the loop can obtain lock between input and VCO signals.

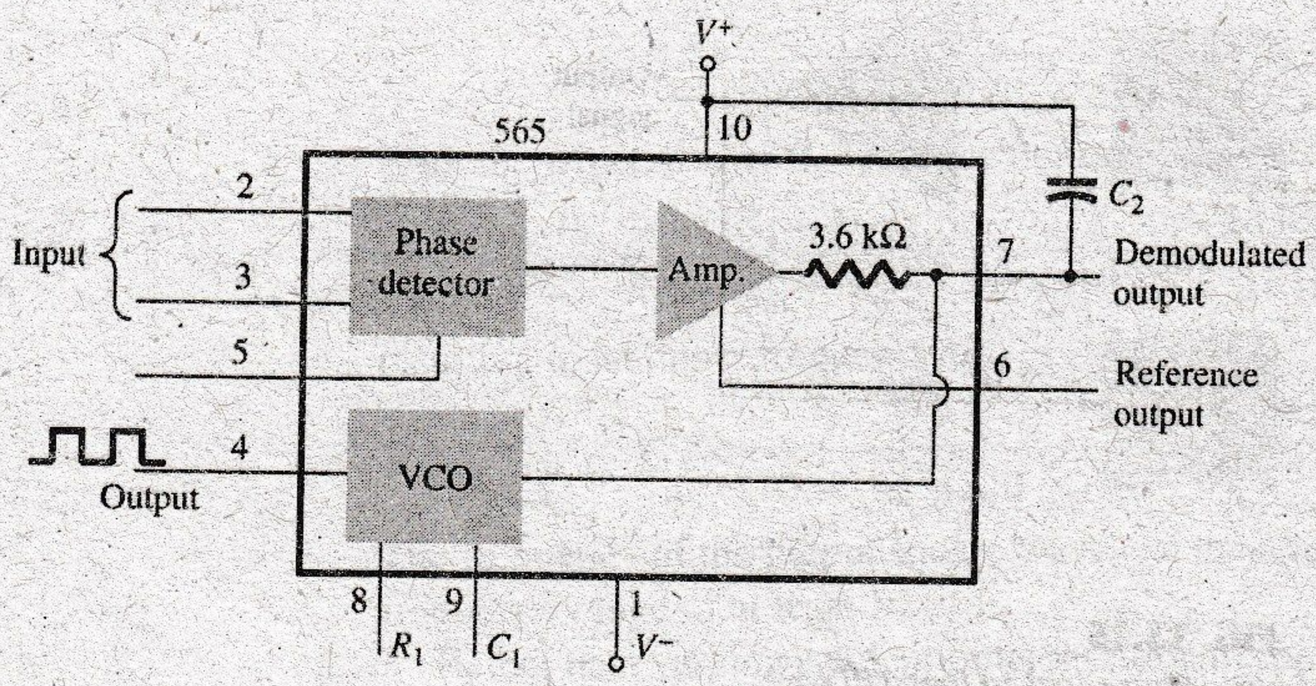
Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the frequency range centered about the VCO free-running frequency f_o over which the loop can acquire lock with the input signal. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the *lock range*.

Applications

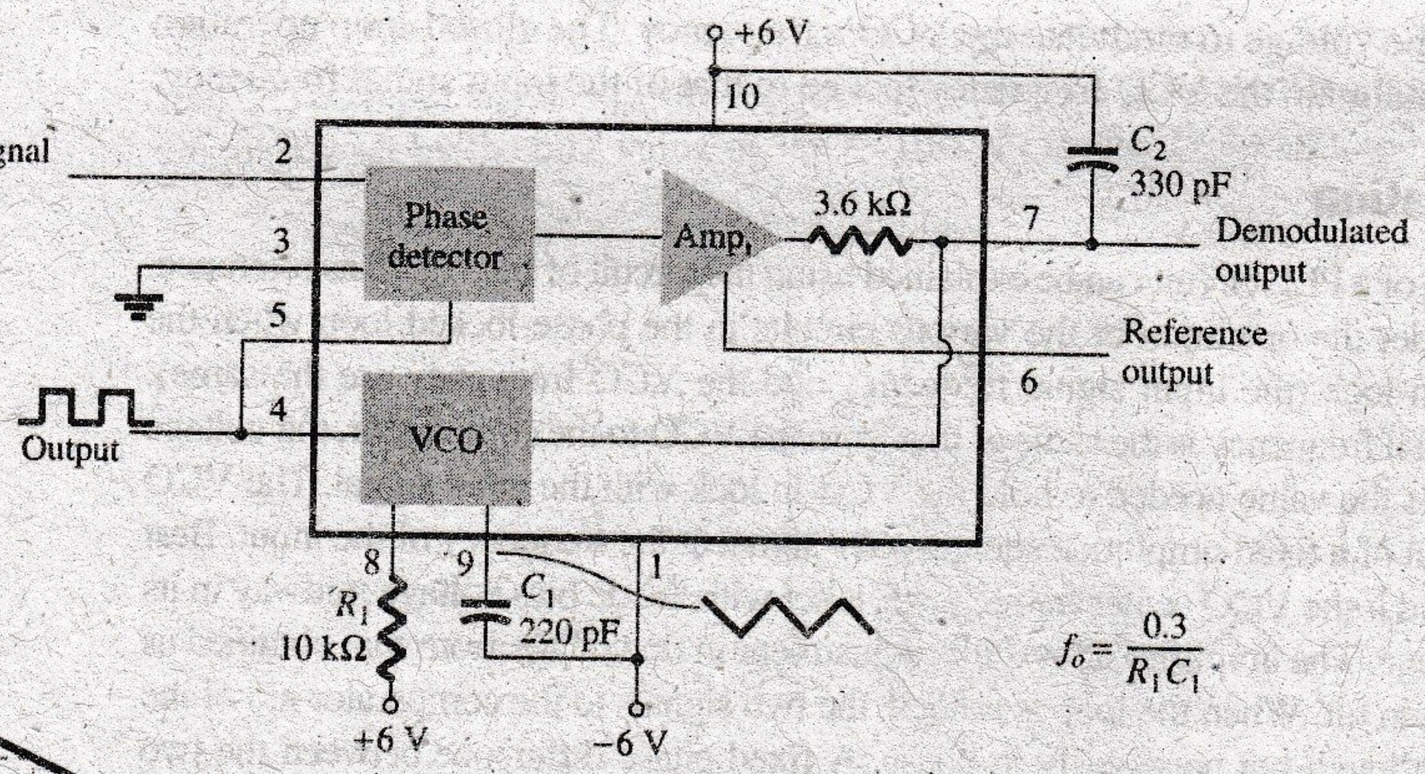
The PLL can be used in a wide variety of applications, including (1) frequency demodulation, (2) frequency synthesis, and (3) FSK decoders. Examples of each of these follow.

Frequency Demodulation FM demodulation or detection can be directly achieved using the PLL circuit. If the PLL center frequency is selected or designed at the FM carrier frequency, the filtered or output voltage of the circuit of Fig. 13.25 is the desired demodulated voltage, varying in value in proportion to the variation of the signal frequency. The PLL circuit thus operates as a complete intermediate-frequency (IF) strip, limiter, and demodulator as used in FM receivers.

One popular PLL unit is the 565, shown in Fig. 13.26a. The 565 contains a phase detector, an amplifier, and a voltage-controlled oscillator, which are only partially connected internally. An external resistor and capacitor R_1 and C_1, respectively, are used to set the free-running or center frequency of the VCO. Another external capacitor, C_2, is used to set the low-pass filter passband, and the VCO output must be connected back as input to the phase detector to close the PLL loop. The 565 typically uses two power supplies, V^+ and V^-.

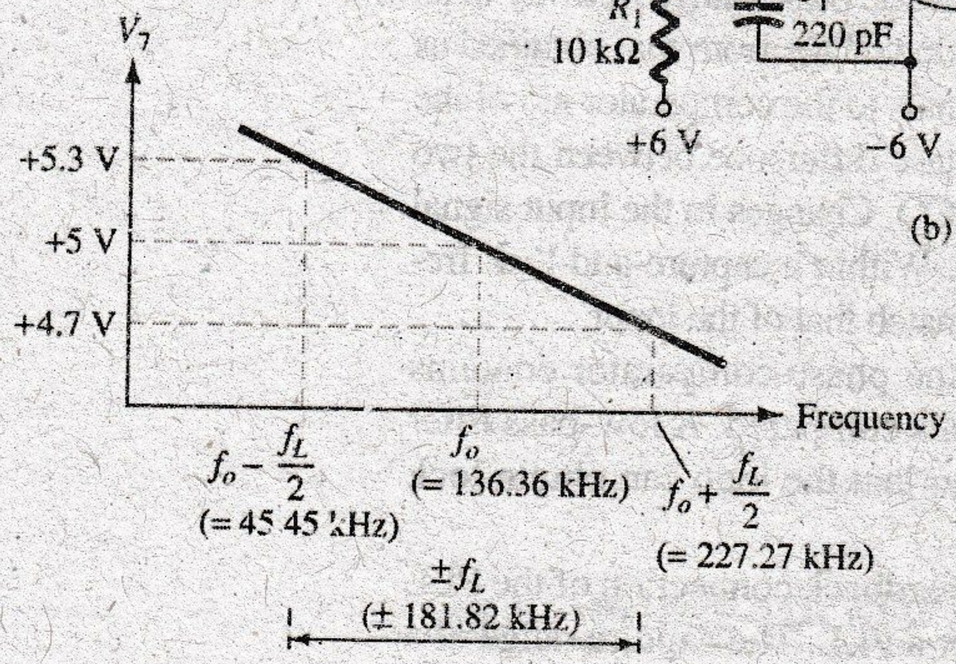


(a)



$$f_o = \frac{0.3}{R_1 C_1}$$

(b)



(c)

FIG. 13.26

Phase-locked loop (PLL): (a) basic block diagram; (b) PLL connected as a frequency demodulator; (c) output voltage versus frequency plot.

Figure 13.26b shows the PLL connected to work as an FM demodulator. Resistor R_1 and capacitor C_1 set the free-running frequency f_o as follows:

$$\boxed{f_o = \frac{0.3}{R_1 C_1}} \tag{13.9}$$

$$= \frac{0.3}{(10 \times 10^3)(220 \times 10^{-12})} = 136.36 \text{ kHz}$$

with limitation $2\,\text{k}\Omega \le R_1 \le 20\,\text{k}\Omega$. The lock range is

$$f_L = \pm\frac{8f_o}{V}$$

$$= \pm\frac{8(136.36 \times 10^3)}{6} = \pm 181.8\,\text{kHz}$$

for supply voltages $V = \pm 6$ V. The capture range is

$$f_C = \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_2 C_2}}$$

$$= \pm\frac{1}{2\pi}\sqrt{\frac{2\pi(181.8 \times 10^3)}{(3.6 \times 10^3)(330 \times 10^{-12})}} = 156.1\,\text{kHz}$$

The signal at pin 4 is a 136.36-kHz square wave. An input within the lock range of 181.8 kHz will result in the output at pin 7 varying around its dc voltage level set with input signal at f_o. Figure 13.26c shows the output at pin 7 as a function of the input signal frequency. The dc voltage at pin 7 is linearly related to the input signal frequency within the frequency range $f_L = 181.8$ kHz around the center frequency 136.36 kHz. The output voltage is the demodulated signal that varies with frequency within the operating range specified.

Frequency Synthesis A frequency synthesizer can be built around a PLL as shown in Fig. 13.27. A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o and the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. The input

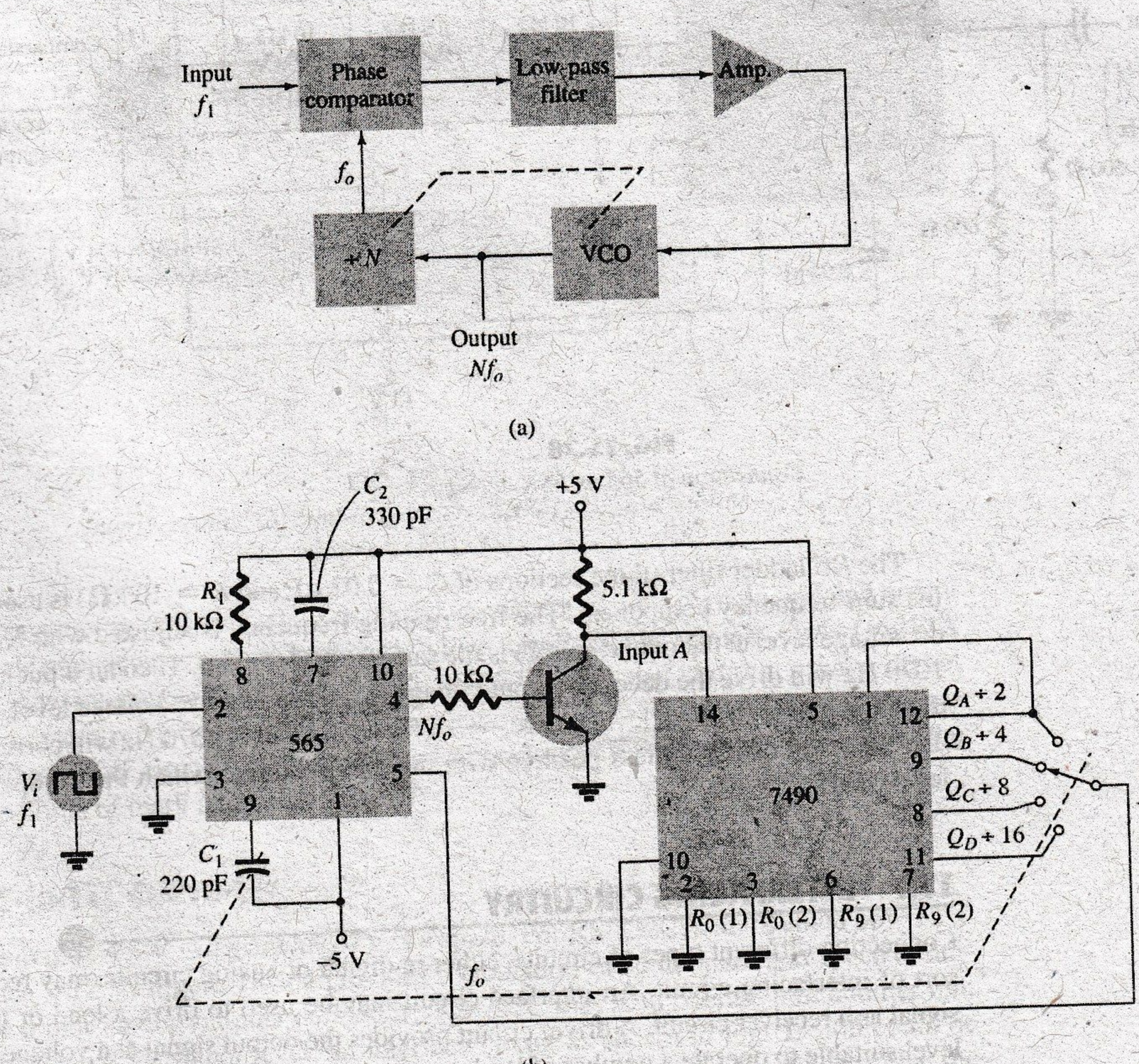


FIG. 13.27

Frequency synthesizer: (a) block diagram; (b) implementation using 565 PLL unit.

signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set up to lock at the fundamental frequency (when $f_o = f_1$). Figure 13.27b shows an example using a 565 PLL as frequency multiplier and a 7490 as divider. The input V_i at frequency f_1 is compared to the input (frequency f_o) at pin 5. An output at Nf_o ($4f_o$ in the present example) is connected through an inverter circuit to provide an input at pin 14 of the 7490, which varies between 0 V and +5V. Using the output at pin 9, which is one-fourth that at the input to the 7490, we find that the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock. Since the VCO can vary over only a limited range from its center frequency, it may be necessary to change the VCO frequency whenever the divider value is changed. As long as the PLL circuit is in lock, the VCO output frequency will be exactly N times the input frequency. It is only necessary to readjust f_o to be within the capture-and-lock range, the closed loop then resulting in the VCO output becoming exactly Nf_1 at lock.

FSK Decoders An FSK (frequency-shift keyed) signal decoder can be built as shown in Fig. 13.28. The decoder receives a signal at one of two distinct carrier frequencies, 1270 Hz or 1070 Hz, representing the RS-232C logic levels or mark (−5 V) or space (+14 V), respectively. As the signal appears at the input, the loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output.

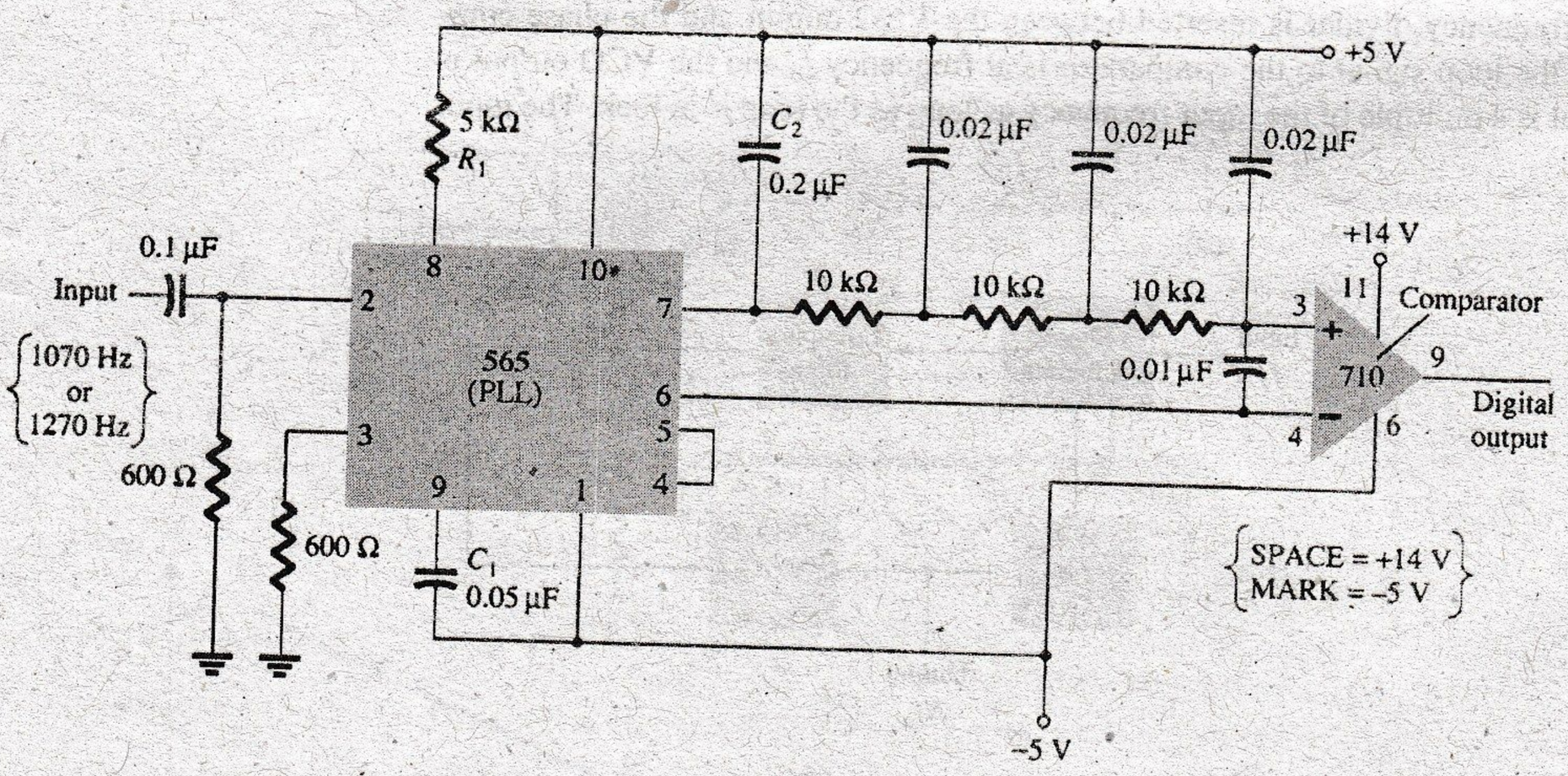


FIG. 13.28
Connection of 565 as FSK decoder.

The *RC* ladder filter (three sections of $C = 0.02\ \mu F$ and $R = 10\ k\Omega$) is used to remove the sum-frequency component. The free-running frequency is adjusted with R_1 so that the dc voltage level at the output (pin 7) is the same as that at pin 6. Then an input at frequency 1070 Hz will drive the decoder output voltage to a more positive voltage level, driving the digital output to the high level (space, or +14 V). An input at 1270 Hz will correspondingly drive the 565 dc output less positive with the digital output, which then drops to the low level (mark, or −5 V).

13.7 INTERFACING CIRCUITRY

Connecting different types of circuits, either in digital or analog circuits, may require some sort of interfacing circuit. An interface circuit may be used to drive a load or to obtain a signal as a receiver circuit. A driver circuit provides the output signal at a voltage or current level suitable to operate a number of loads, or to operate such devices as relays, displays, or power units. A receiver circuit essentially accepts an input signal, providing high input impedance to minimize loading of the input signal. Furthermore, the interface circuits may

include strobing, which provides connecting the interface signals during specific time intervals established by the strobe.

Figure 13.29a shows a dual-line driver, each driver accepting input of TTL signals, providing output capable of driving TTL or MOS device circuits. This type of interface circuit comes in various forms, some as inverting and others as noninverting units. The circuit of Fig. 13.29b shows a dual-line receiver having both inverting and noninverting inputs so that either operating condition can be selected. As an example, connection of an input signal to the inverting input would result in an inverted output from the receiver unit. Connecting the input to the noninverting input would provide the same interfacing except that the output obtained would have the same polarity as the received signal. The driver–receiver unit of Fig. 13.29 provides an output when the strobe signal is present (high in this case).

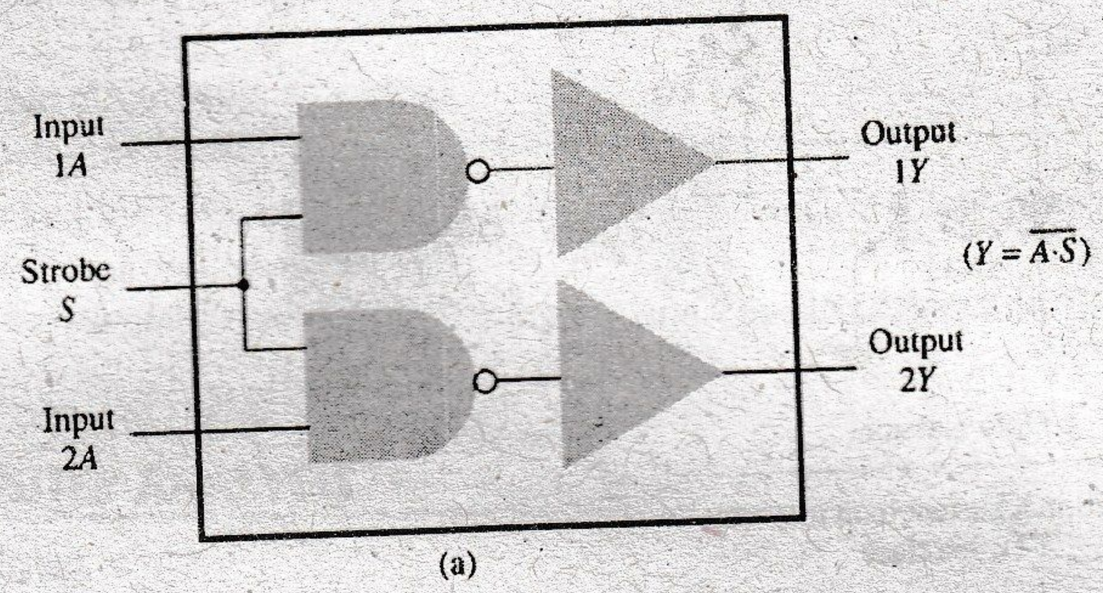


FIG. 13.29
Interface units: (a) dual-line drivers (SN75150); (b) dual-line receivers (SN75152).

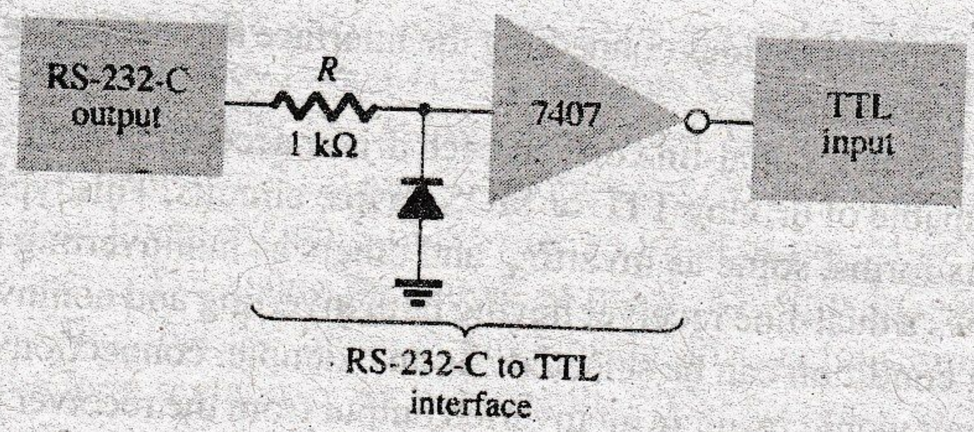
Another type of interface circuit is that used to connect various digital input and output units, signals with devices such as keyboards, video terminals, and printers. One of the EIA electronic industry standards is referred to as RS-232C. This standard states that a digital signal represents a mark (logic-1) and a space (logic-0). The definitions of mark and space vary with the type of circuit used (although a full reading of the standard will spell out the acceptable limits of mark and space signals).

RS-232C-to-TTL Converter

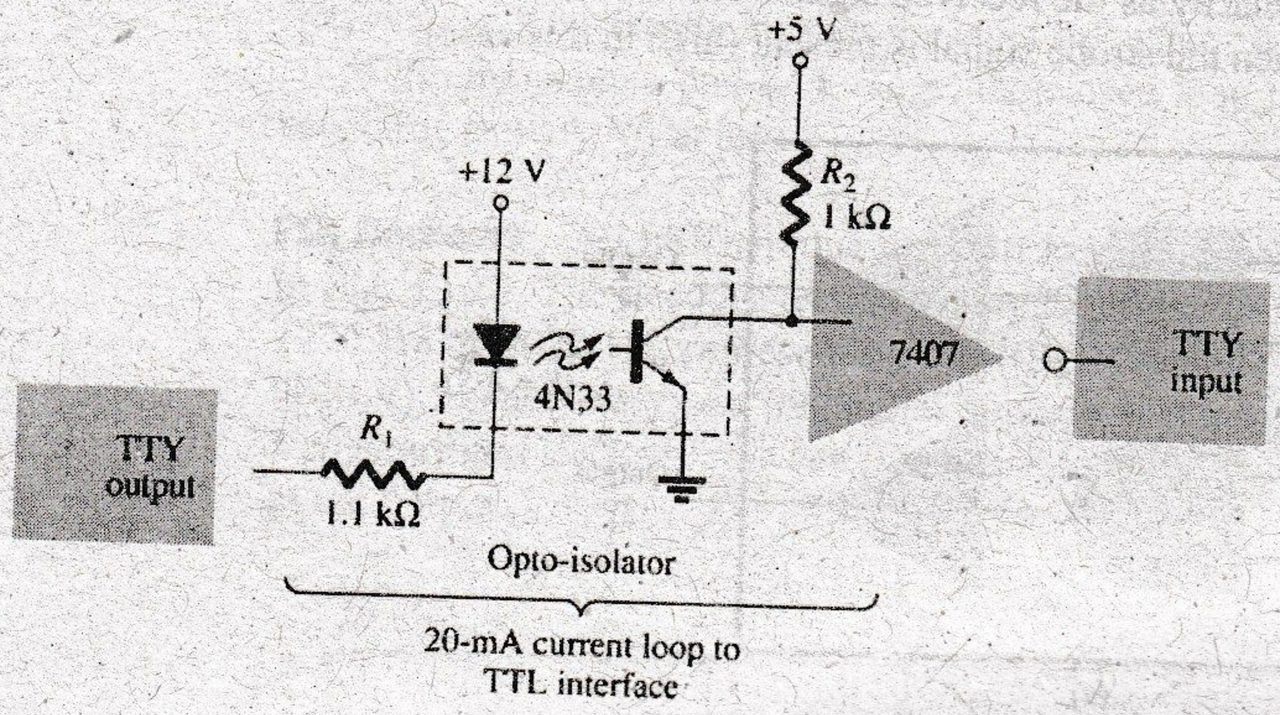
For TTL circuits, +5 V is a mark and 0 V is a space. For RS-232C, a mark could be −12 V and a space +12 V. Figure 13.30a provides a tabulation of some mark and space definitions. For a unit having outputs defined by RS-232C that is to operate into another unit operating with a TTL signal level, an interface circuit as shown in Fig. 13.30b could be used. A mark output from the driver (at −12 V) would be clipped by the diode so that the input to the inverter circuit is near 0 V, resulting in an output of +5 V (TTL mark). A space output at +12 V would drive the inverter output low for a 0-V output (a space).

	Current Loop	RS-232-C	TTL
MARK	20 mA	−12 V	+5 V
SPACE	0 mA	+12 V	0 V

(a)



(b)

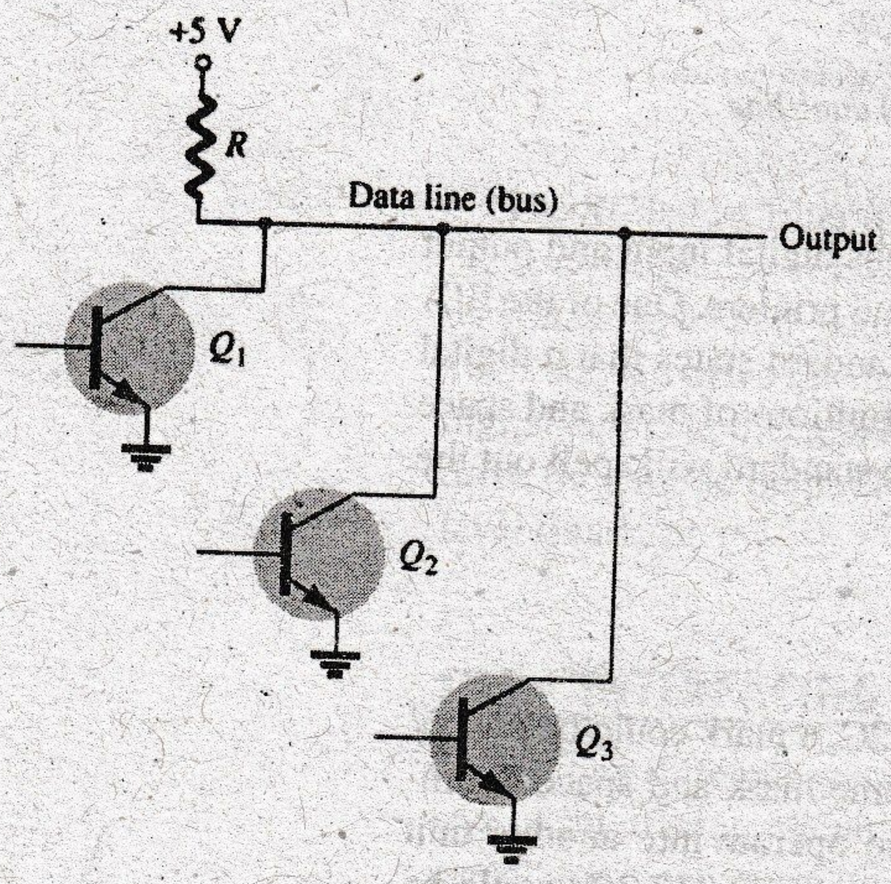


(c)

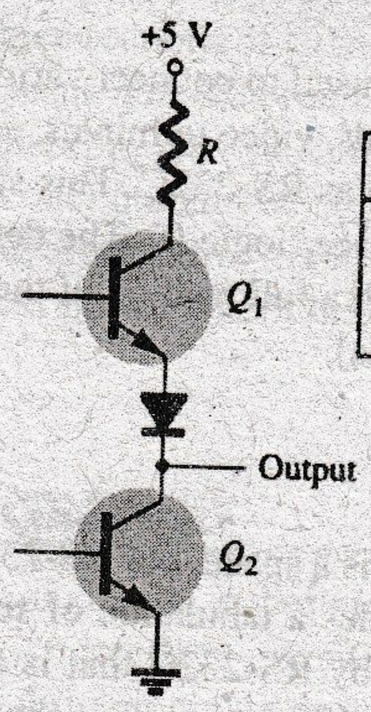
FIG. 13.30
Interfacing signal standards and converter circuits.

Another example of an interface circuit converts the signals from a TTY current loop into TTL levels as shown in Fig. 13.30c. An input mark results when 20 mA of current is drawn from the source through the output line of the teletype (TTY). This current then goes through the diode element of an opto-isolator, driving the output transistor on. The input to the inverter going low results in a +5-V signal from the 7407 inverter output so that a mark from the teletype results in a mark to the TTL input. A space from the teletype current loop provides no current, with the opto-isolator transistor remaining off and the inverter output then 0 V, which is a TTL space signal.

Another means of interfacing digital signals is made using open-collector output or tri-state output. When a signal is output from a transistor collector (see Fig. 13.31) that is not



(a)



Q_1	Q_2	Output
Off	Off	Open circuit
Off	On	0 V
On	Off	+5 V

(b)

FIG. 13.31
Connections to data lines: (a) open-collector output; (b) tri-state output.

connected to any other electronic component, the output is open-collector. This permits connecting a number of signals to the same wire or bus. Any transistor going on then provides a low output voltage, whereas all transistors remaining off provides a high output voltage.

13.8 SUMMARY

Important Conclusions and Concepts

1. A comparator provides an output of either maximum-high or maximum low when one input goes above or below the other.
2. A DAC is a digital-to-analog converter.
3. An ADC is an analog-to-digital converter.
4. Timer IC:
   a. An astable circuit acts as a clock.
   b. A monostable circuit acts as a one-shot or timer.
5. A phase-locked loop (PLL) circuit contains a phase detector, a low-pass filter, and a voltage-controlled oscillator (VCO).
6. There are two standard types of interfacing circuits: **the RS-232-C and the TTL.**

13.9 COMPUTER ANALYSIS

PSpice Windows

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems can display the resulting dc bias, or one can use **PROBE** to display resulting waveforms.

Program 13.1—Comparator Circuit Used to Drive an LED Using PSpice, draw the circuit of a comparator circuit with output driving an LED indicator as shown in Fig. 13.32. To be able to view the magnitude of the dc output voltage, place a **VPRINT1** component at V_o with **DC** and **MAG** selected. To view the dc current through the LED, place an **IPRINT** component in series with the **LED** current meter as shown in Fig. 13.32. The **Analysis Setup** provides for a dc sweep as shown in Fig. 13.33. The **DC Sweep** is set, as shown, for V_i from 4 V to 8 V in 1-V steps. After running the simulation, some of the resulting analysis output obtained is as shown in Fig. 13.34.

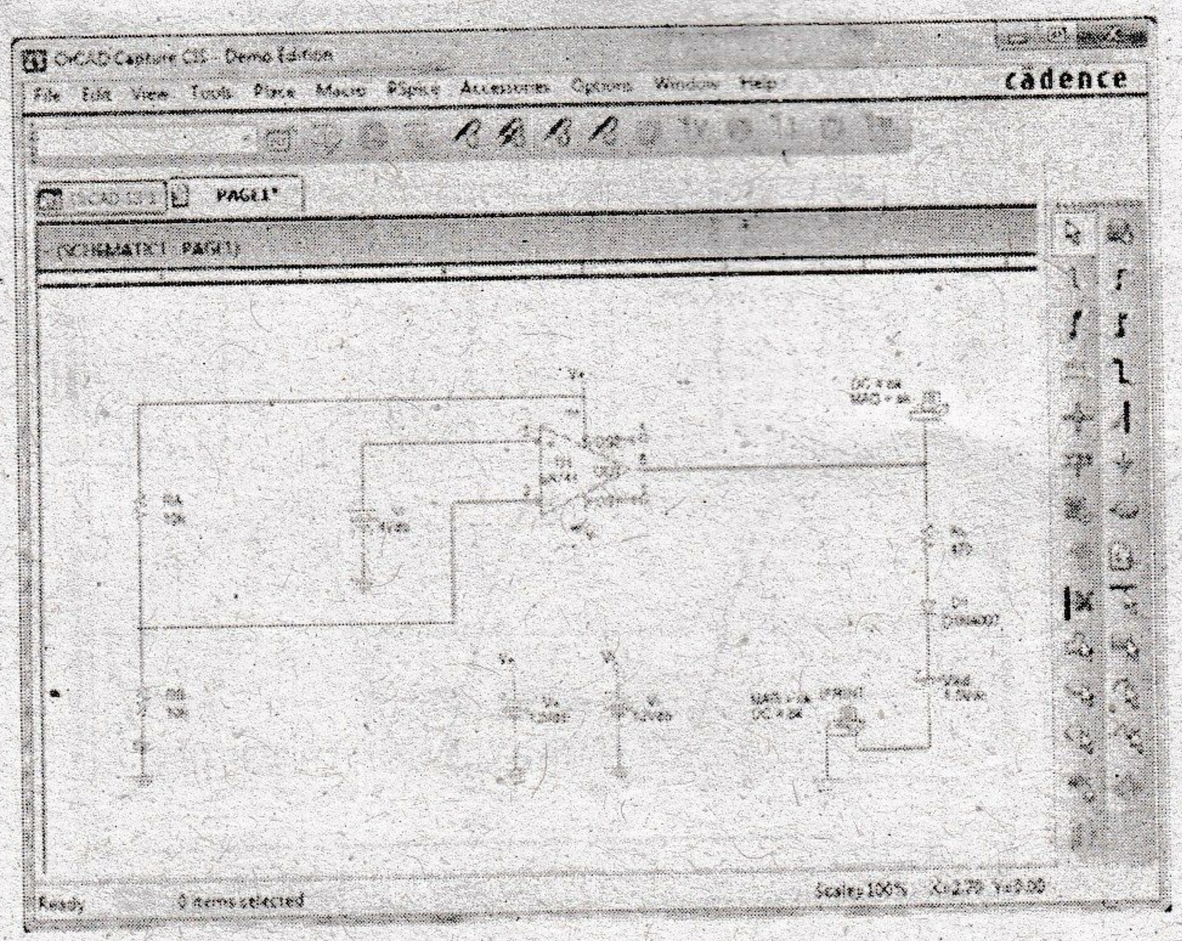


FIG. 13.32

Cor *ircuit used to drive an LED.*

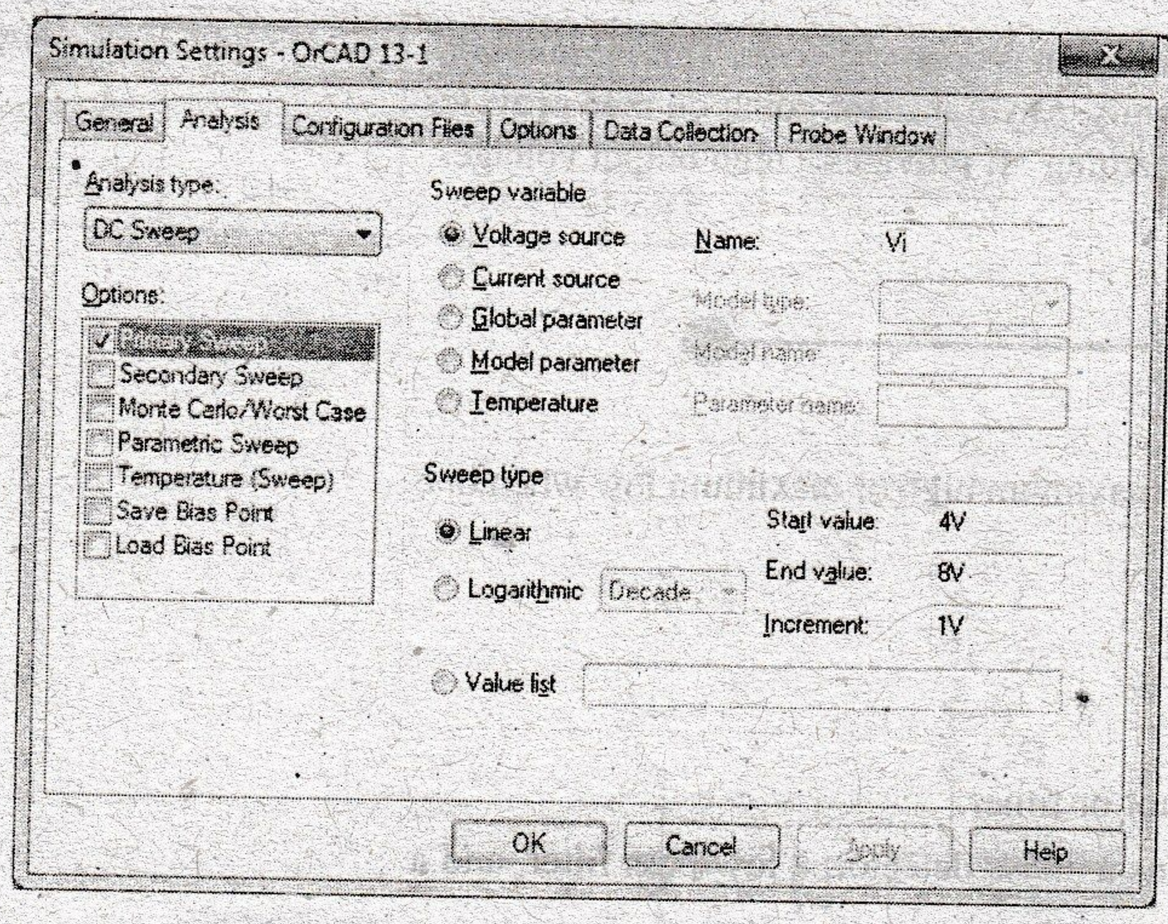


FIG. 13.33

Analysis Setup for a dc sweep of the circuit of Fig. 13.32.

```
****          DC TRANSFER CURVES
*****************************************
V_Vi          V(N00334)

4.000E+00     1.200E+01
5.000E+00     1.200E+01
6.000E+00     1.200E+01
7.000E+00     1.200E+01
8.000E+00     1.200E+01

****          DC TRANSFER CURVES
*****************************************
V_Vi          I(V_PRINT2)

4.000E+00     -2.079E-02
5.000E+00     -2.079E-02
6.000E+00     -2.079E-02
7.000E+00     -2.079E-02
8.000E+00     -2.079E-02
```

FIG. 13.34

Analysis output (edited) for circuit of Fig. 13.32.

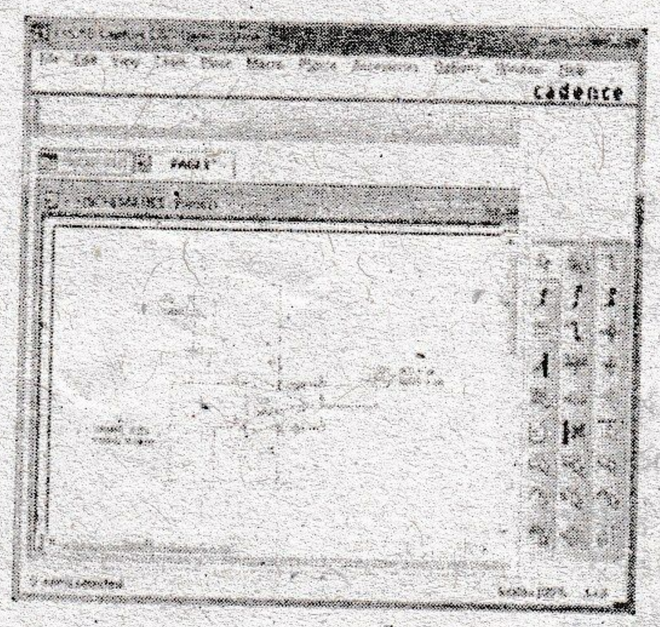


FIG. 13.35

Schematic for a comparator.

The circuit of Fig. 13.32 shows a voltage divider that provides 6 V to the minus input, so that any input V_i below 6 V will result in the output at the minus saturation voltage (near −10 V). Any input above +6 V results in the output going to the positive saturation level (near +10 V). The LED will therefore be driven *on* by any input above the reference level of +6 V and left *off* by any input below +6 V. Figure 13.34 shows a table of the output voltage and a table of the LED current for inputs from 4 V to 8 V. The table shows that the LED current is nearly 0 for inputs up to +6 V, and that a current of about 20 mA lights the LED for inputs at +6 V or above.

Program 13.2—Comparator Operation The operation of a comparator IC can be demonstrated using a 741 op-amp as shown in Fig. 13.35. The input is a 5 V, peak sinusoidal signal. The **Analysis Setup** provides for **Transient** analysis with **Print Step** of **20 ns** and **Run Time** of **3 ms**. Since the input signal is applied to the noninverting input, the output is in phase with the input. When the input goes above 0 V, the output goes to the positive saturation level, near +5 V. When the input goes below 0 V, the output goes to the negative saturation level—this being 0 V since the minus voltage input is set to that value. Figure 13.36 shows input and output voltages.

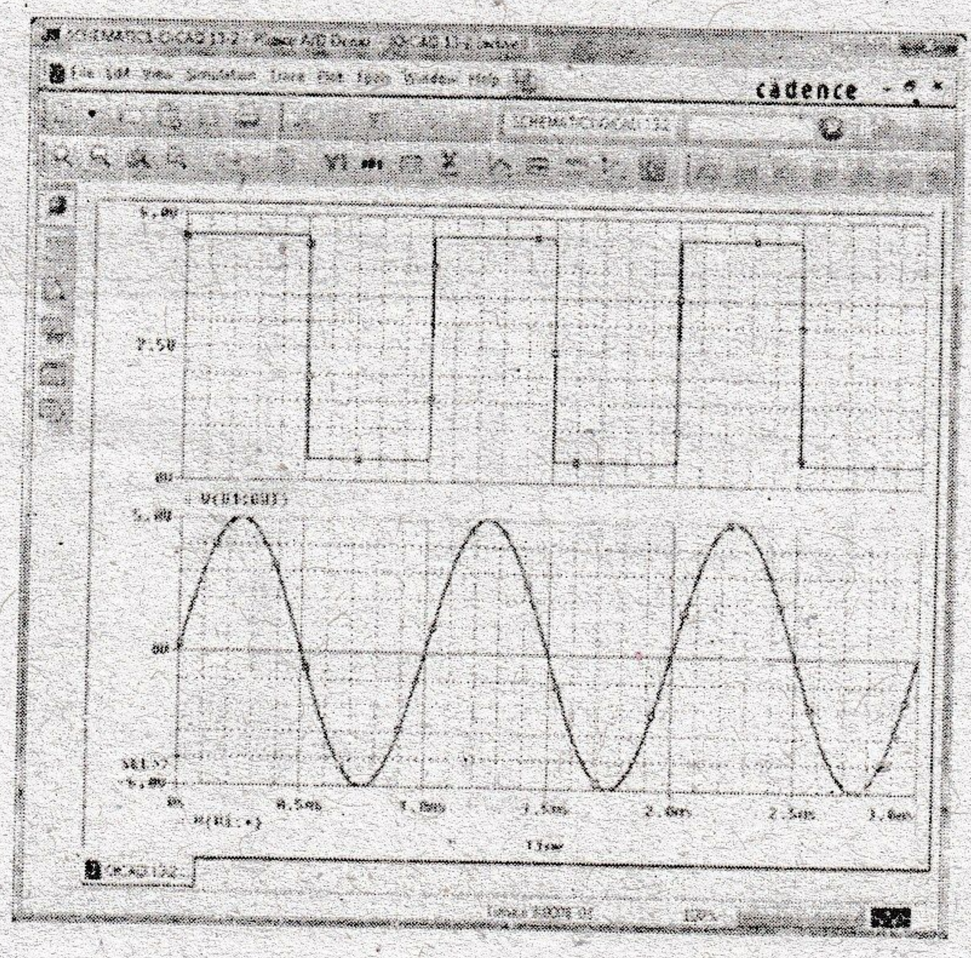


FIG. 13.36

Output for the comparator of Fig. 13.35.

Program 13.3–Operation of 555 Timer as Oscillator Figure 13.37 shows a 555 timer connected as an oscillator. Equations (13.3) and (13.4) can be used to calculate the charge and discharge times as follows:

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5\,\text{k}\Omega + 7.15\,\text{k}\Omega)(0.1\,\mu\text{F}) = 1.05\,\text{ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5\,\text{k}\Omega)(0.1\,\mu\text{F}) = 0.525\,\text{ms}$$

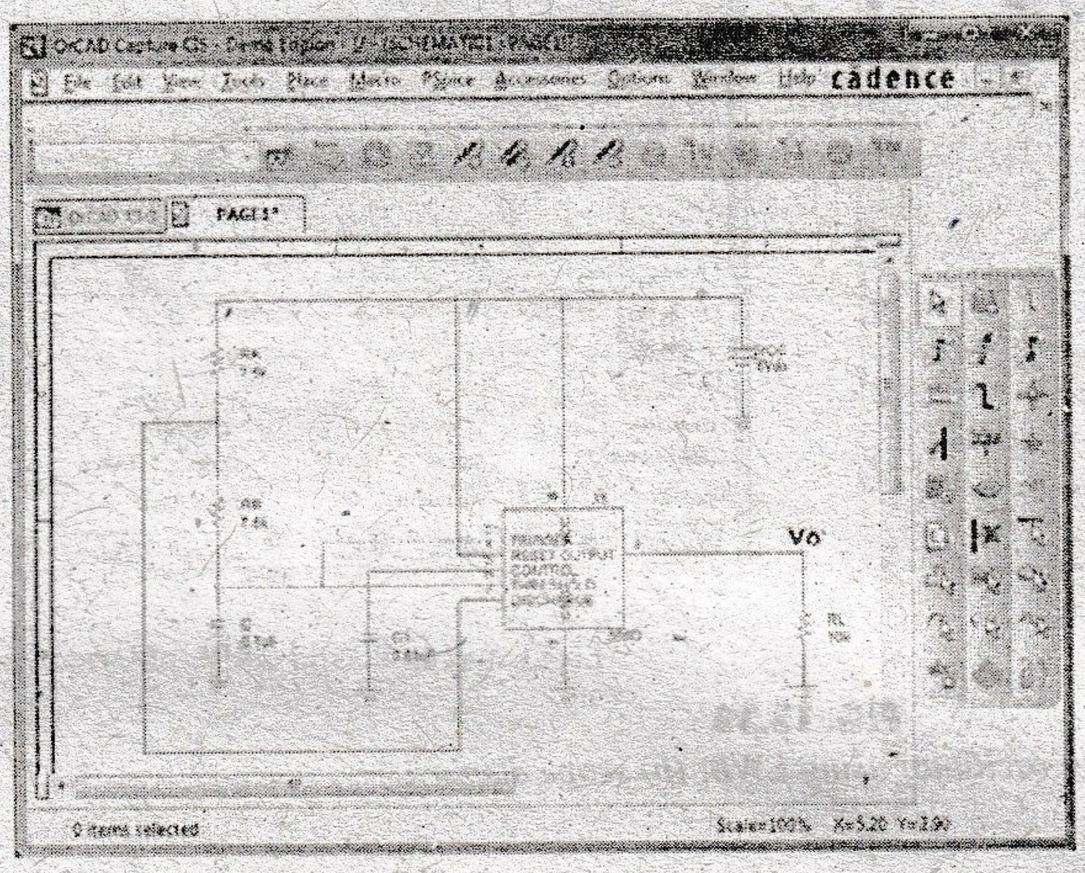


FIG. 13.37
Schematic of a 555 timer oscillator.

The resulting trigger and output waveforms are shown in Fig. 13.38. When the trigger charges to the upper trigger level, the output goes to the low output level of 0 V. The output stays low until the trigger input discharges to the low trigger level, at which time the output goes to the high level of +5 V.

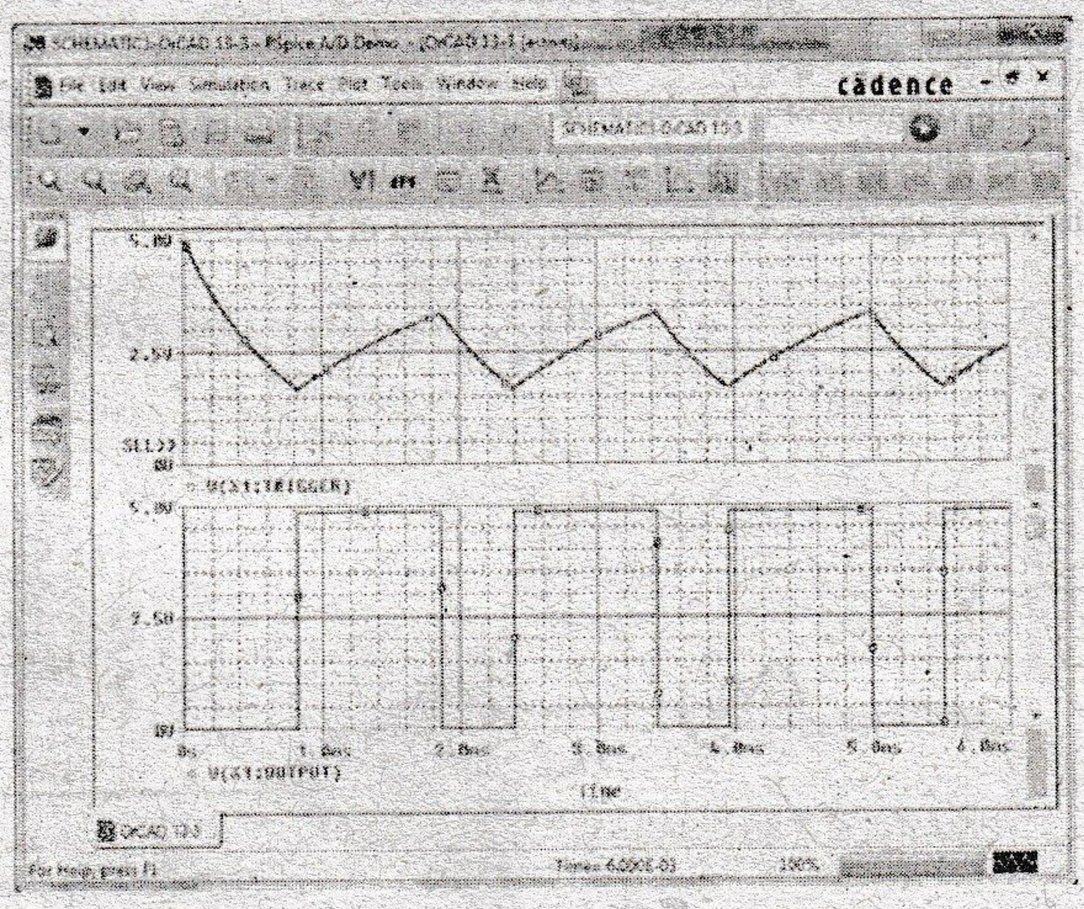
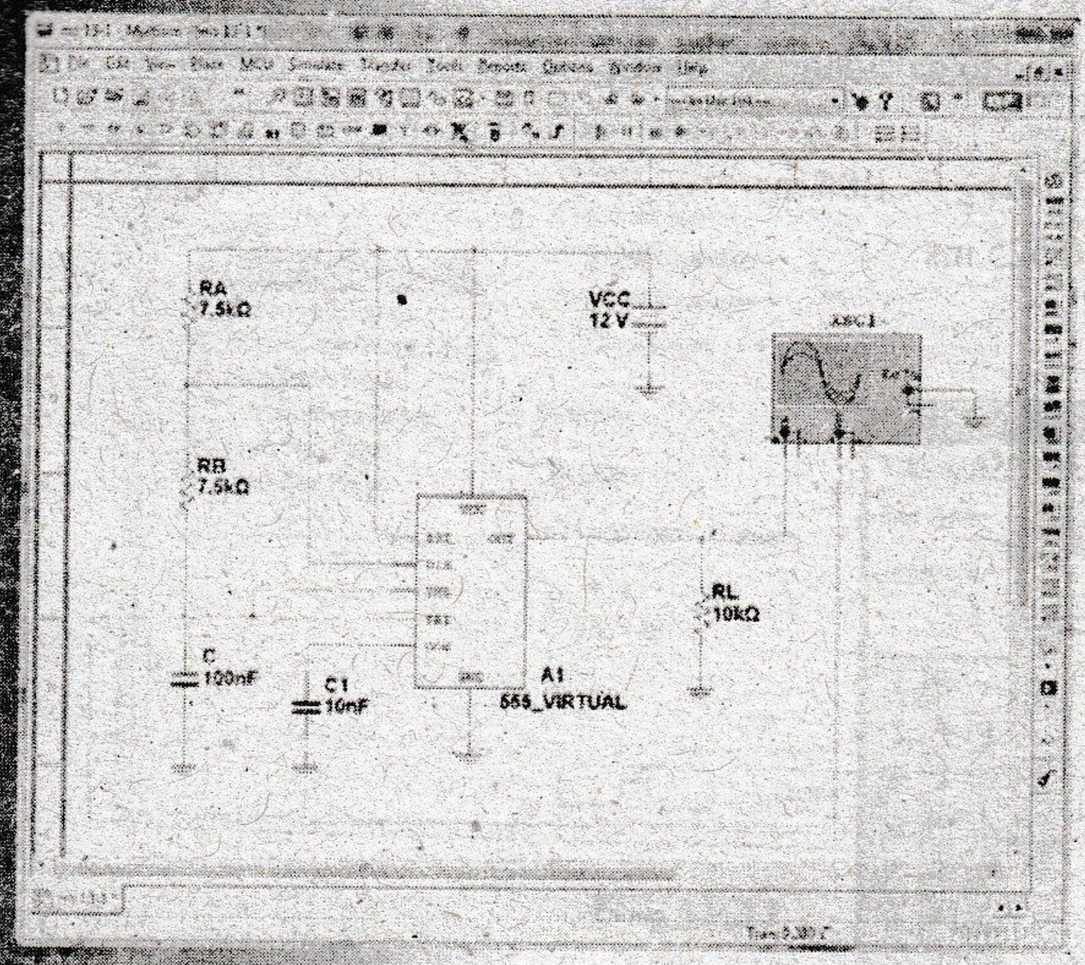


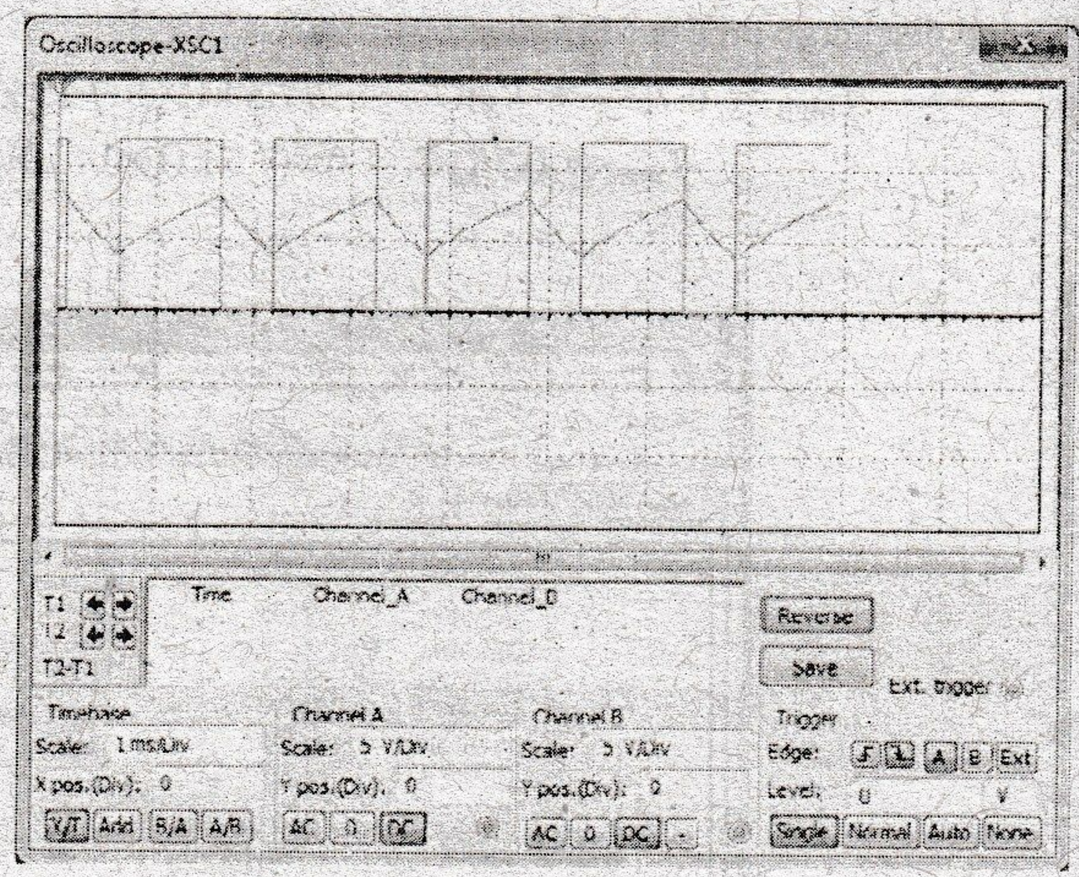
FIG. 13.38
Probe output for the 555 oscillator of Fig. 13.37.

Multisim

Program 13.4–The 555 Timer as an Oscillator Figure 13.39(a) shows the same oscillator circuit as in Program 13.3, this time using Multisim to build the circuit and to show



(a)



(b)

FIG. 13.39
(a) Timer oscillator using EWB; (b) scope display.

resulting waveforms on an oscilloscope. Using the oscilloscope instrument, we find the waveform across the capacitor and that from the output as shown in Fig. 13.39(b).

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

13.2 Comparator Unit Operation

1. Draw the diagram of a 741 op-amp operated from ±15-V supplies with $V_i(-) = 0$ V and $V_i(+) = +5$ V. Include terminal pin connections.
2. Sketch the output waveform for the circuit of Fig. 13.40.
3. Draw a circuit diagram of a 311 op-amp showing an input of 10 V rms applied to the inverting input and the plus input to ground. Identify all pin numbers.
4. Draw the resulting output waveform for the circuit of Fig. 13.41.

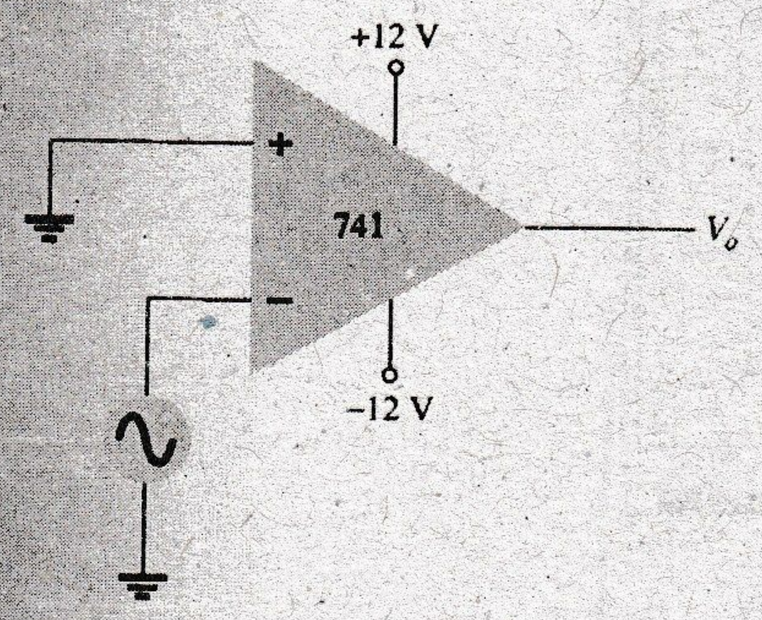


FIG. 13.40
Problem 2.

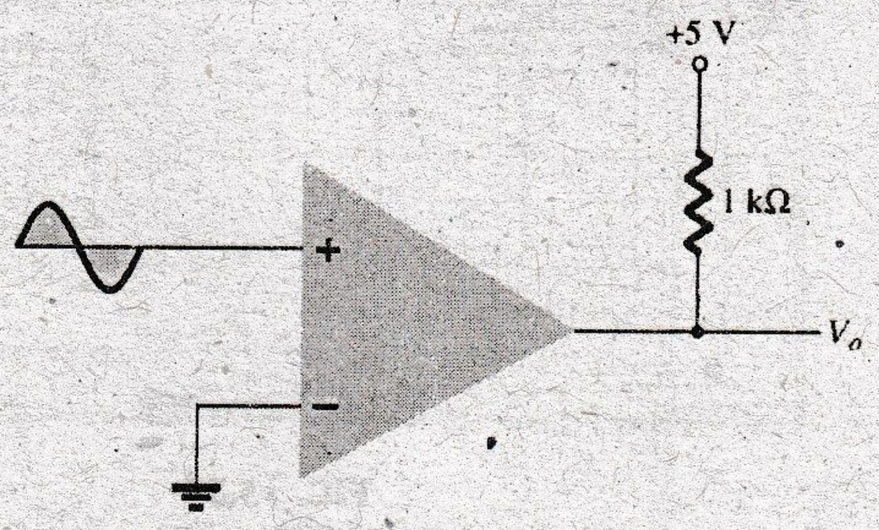


FIG. 13.41
Problem 4.

5. Draw the circuit diagram of a zero-crossing detector using a 339 comparator stage with ±12-V supplies.

6. Sketch the output waveform for the circuit of Fig. 13.42.

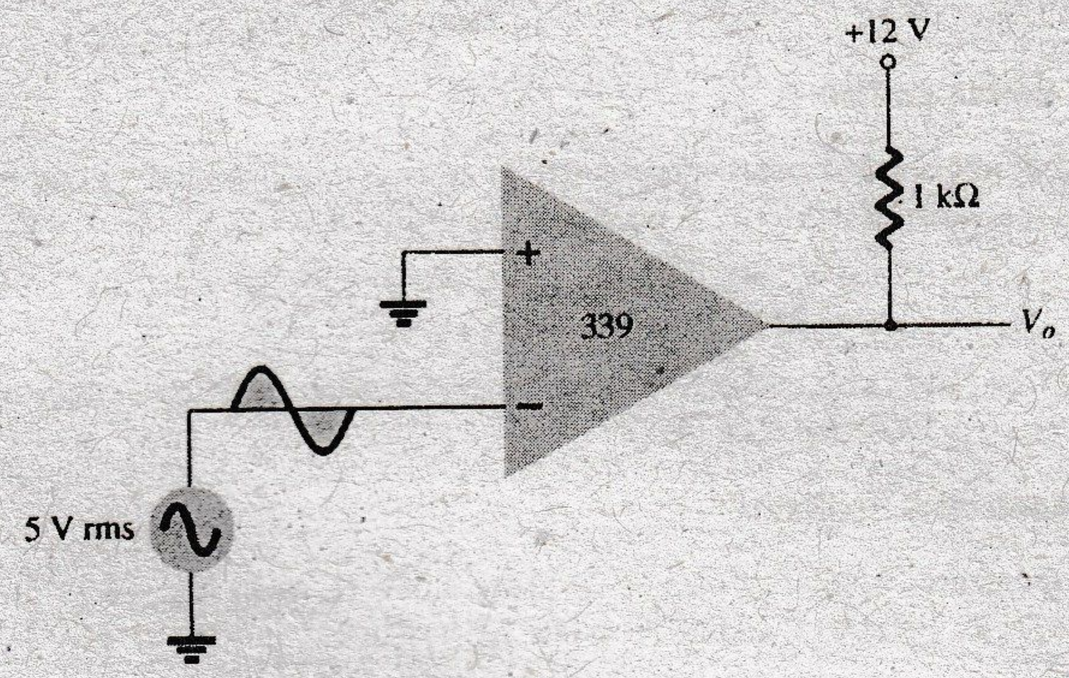


FIG. 13.42
Problem 6.

***7.** Describe the operation of the circuit in Fig. 13.43.

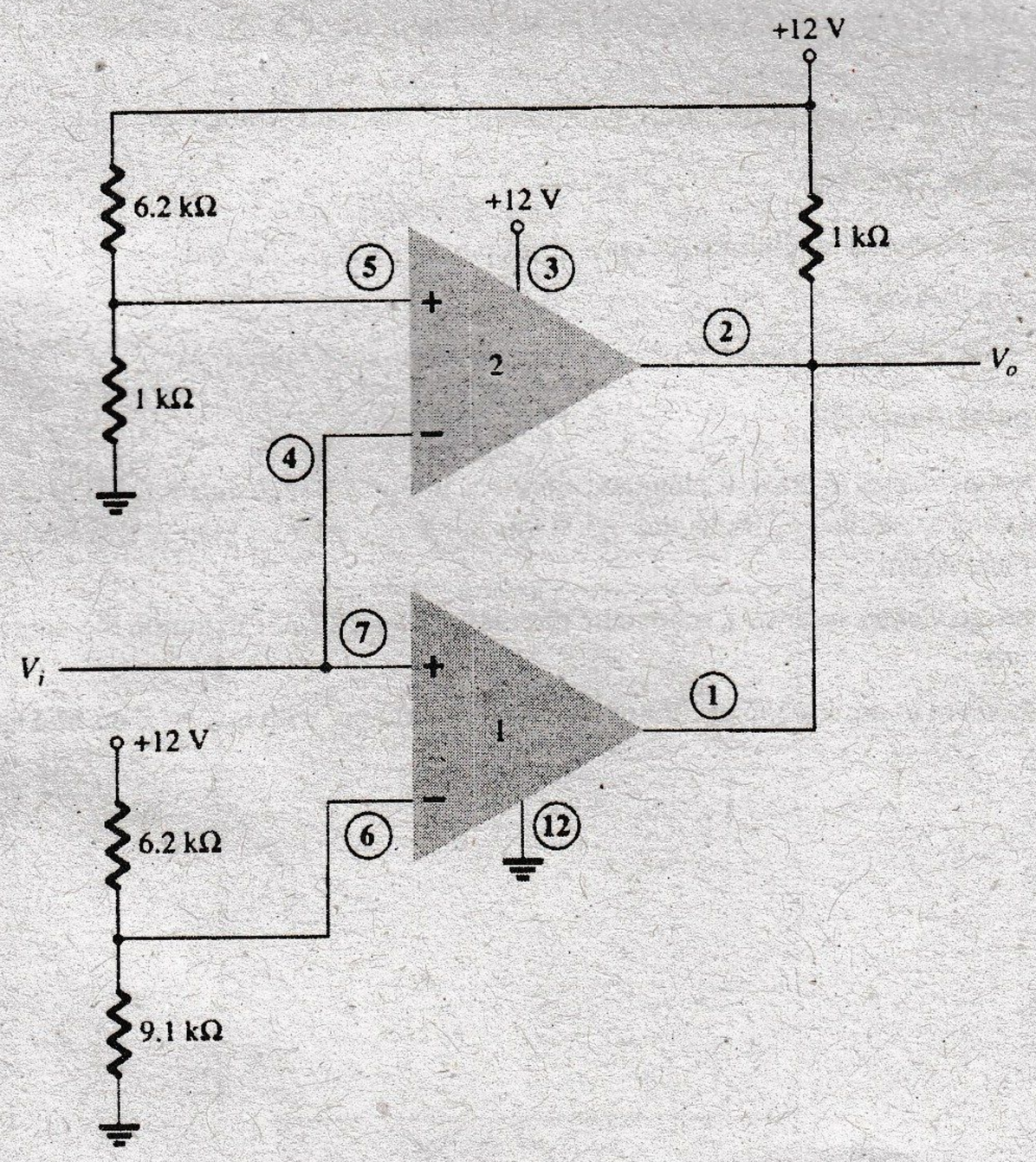


FIG. 13.43
Problem 7.

13.3 Digital–Analog Converters

8. Sketch a five-stage ladder network using 15-kΩ and 30-kΩ resistors.

9. For a reference voltage of 16 V, calculate the output voltage for an input of 11010 to the circuit of Problem 8.

10. What voltage resolution is possible using a 12-stage ladder network with a 10-V reference voltage?

11. For a dual-slope converter, describe what occurs during the fixed time interval and the count interval.

of the peak point, the device cannot turn on. An equation for R_1 that will ensure a turn-on condition can be established if we consider the peak point at which $I_{R_1} = I_P$ and $V_E = V_P$. (The equality $I_{R_1} = I_P$ is valid since the charging current of the capacitor at this instant is zero. That is, at this particular instant the capacitor is changing from a charging to a discharging state.) Then $V - I_{R_1}R_1 = V_E$ and $R_1 = (V - V_E)/I_{R_1} = (V - V_P)/I_P$ at the peak point. To ensure firing, the condition is

$$\boxed{R_1 < \frac{V - V_P}{I_P}} \tag{17.6}$$

At the valley point $I_E = I_V$ and $V_E = V_V$, so that

$$V - I_{R_1}R_1 = V_E$$

becomes

$$V - I_V R_1 = V_V$$

and

$$R_1 = \frac{V - V_V}{I_V}$$

or, to ensure turning off,

$$\boxed{R_1 > \frac{V - V_V}{I_V}} \tag{17.7}$$

The range of R_1 is therefore limited by

$$\boxed{\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P}} \tag{17.8}$$

The resistance R_2 must be chosen small enough to ensure that the SCR is not turned on by the voltage V_{R_2} of Fig. 17.42 when $I_E \cong 0$ A. The voltage V_{R_2} is then given by

$$\boxed{V_{R_2} \cong \left.\frac{R_2 V}{R_2 + R_{BB}}\right|_{I_E = 0\text{ A}}} \tag{17.9}$$

The capacitor C will determine, as we shall see, the time interval between triggering pulses and the time span of each pulse.

At the instant the dc supply voltage V is applied, the voltage $v_E = v_C$ will charge toward V volts from V_V as shown in Fig. 17.43 with a time constant $\tau = R_1C$.

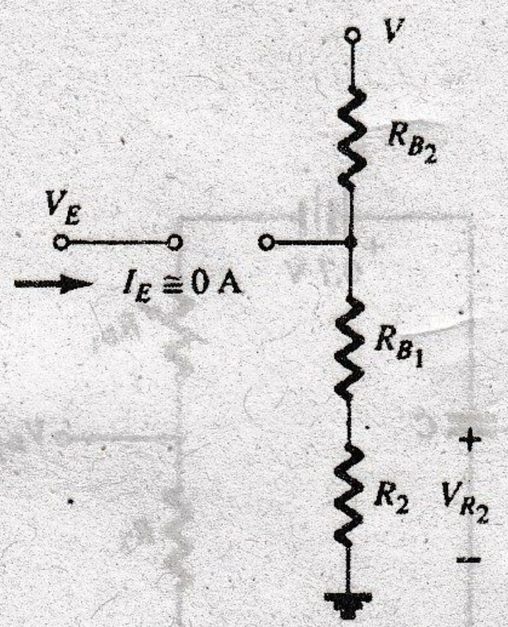


FIG. 17.42
Triggering network when $I_E \cong 0$ A.

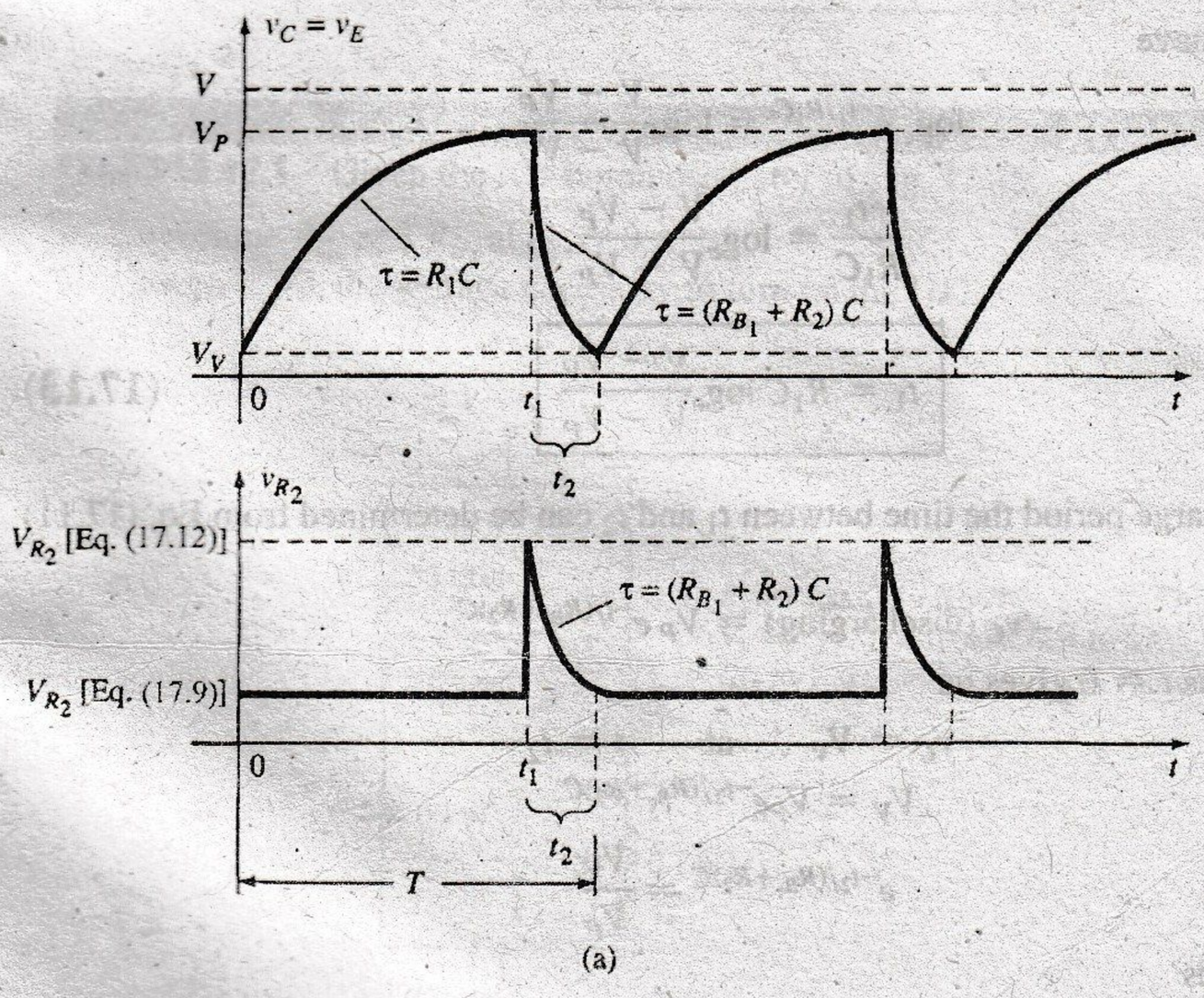


FIG. 17.43
(a) Charging and discharging phases for trigger network of Fig. 17.40; (b) equivalent network when UJT turns on.

The general equation for the charging period is

$$v_C = V_V + (V - V_V)(1 - e^{-t/R_1C}) \tag{17.10}$$

As noted in Fig. 17.43, the voltage across R_2 is determined by Eq. (17.9) during this charging period. When $v_C = v_E = V_P$, the UJT will enter the conduction state and the capacitor will discharge through R_{B_1} and R_2 at a rate determined by the time constant $\tau = (R_{B_1} + R_2)C$.

The discharge equation for the voltage $v_C = v_E$ is

$$v_C \cong V_P e^{-t/(R_{B_1}+R_2)C} \tag{17.11}$$

Equation (17.11) is complicated somewhat by the fact that R_{B_1} will decrease with increasing emitter current and the other elements of the network, such as R_1 and V, will affect the discharge rate and final level. However, the equivalent network appears as shown in Fig. 17.43 and the magnitudes of R_1 and R_{B_2} are typically such that a Thévenin network for the network surrounding the capacitor C will be only slightly affected by these two resistors. Even though V is a reasonably high voltage, the voltage-divider contribution to the Thévenin voltage can be ignored on an approximate basis.

Using the reduced equivalent of Fig. 17.44 for the discharge phase results in the following approximation for the peak value of V_{R_2}:

$$V_{R_2} \cong \frac{R_2(V_P - 0.7)}{R_2 + R_{B_1}} \tag{17.12}$$

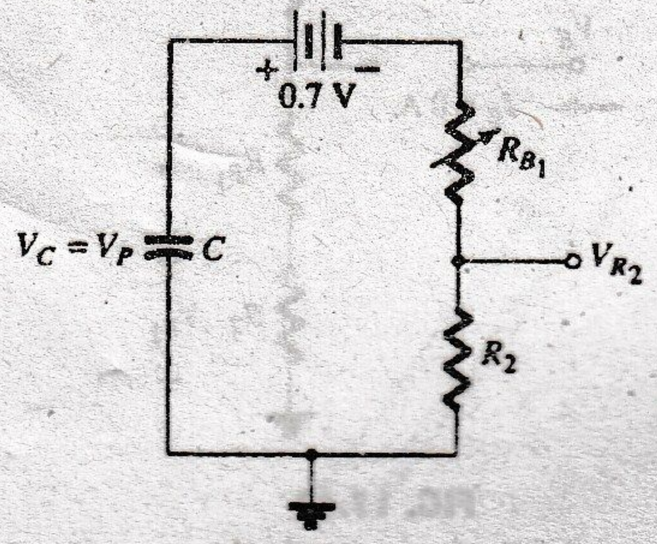


FIG. 17.44
Reduced equivalent network when UJT turns on.

The period t_1 of Fig. 17.43 can be determined in the following manner:

$$\begin{aligned} v_C\,(\text{charging}) &= V_V + (V - V_V)(1 - e^{-t/R_1C}) \\ &= V_V + V - V_V - (V - V_V)e^{-t/R_1C} \\ &= V - (V - V_V)e^{-t/R_1C} \end{aligned}$$

when $v_C = V_P$, $t = t_1$, and $V_P = V - (V - V_V)e^{-t_1/R_1C}$, or

$$\frac{V_P - V}{V - V_V} = -e^{-t_1/R_1C}$$

and

$$e^{-t_1/R_1C} = \frac{V - V_P}{V - V_V}$$

Using logs, we have

$$\log_e e^{-t_1/R_1C} = \log_e \frac{V - V_P}{V - V_V}$$

and

$$\frac{-t_1}{R_1C} = \log_e \frac{V - V_P}{V - V_P}$$

with

$$t_1 = R_1C \log_e \frac{V - V_V}{V - V_P} \tag{17.13}$$

For the discharge period the time between t_1 and t_2 can be determined from Eq. (17.11) as follows:

$$v_C\,(\text{discharging}) = V_P\, e^{-t/(R_{B_1}+R_2)C}$$

Establishing t_1 as $t = 0$ gives us

$$v_C = V_V \quad \text{at} \quad t = t_2$$

and

$$V_V = V_P e^{-t_2/(R_{B_1}+R_2)C}$$

or

$$e^{-t_2/(R_{B_1}+R_2)C} = \frac{V_V}{V_P}$$

Using logs yields

$$\frac{-t_2}{(R_{B_1} + R_2)C} = \log_e \frac{V_V}{V_P}$$

and
$$t_2 = (R_{B_1} + R_2)C \log_e \frac{V_P}{V_V} \tag{17.14}$$

The period of time to complete one cycle is defined by T in Fig. 17.43. That is,

$$T = t_1 + t_2 \tag{17.15}$$

Relaxation Oscillator

If the SCR were dropped from the configuration, the network would behave as a *relaxation oscillator*, generating the waveform of Fig. 17.43. The frequency of oscillation is determined by

$$f_{\text{osc}} = \frac{1}{T} \tag{17.16}$$

In many systems, $t_1 \gg t_2$, and

$$T \cong t_1 = R_1 C \log_e \frac{V - V_V}{V - V_P}$$

Since $V \gg V_V$ in many instances,

$$T \cong t_1 = R_1 C \log_e \frac{V}{V - V_P}$$

$$= R_1 C \log_e \frac{1}{1 - V_P/V}$$

but $\eta = V_P/V$ if we ignore the effects of V_D in Eq. (17.5), and

$$T \cong R_1 C \log_e \frac{1}{1 - \eta}$$

or
$$f \cong \frac{1}{R_1 C \log_e [1/(1 - \eta)]} \tag{17.17}$$

EXAMPLE 17.1 Given the relaxation oscillator of Fig. 17.45:

a. Determine R_{B_1} and R_{B_2} at $I_E = 0$ A.
b. Calculate V_P, the voltage necessary to turn on the UJT.

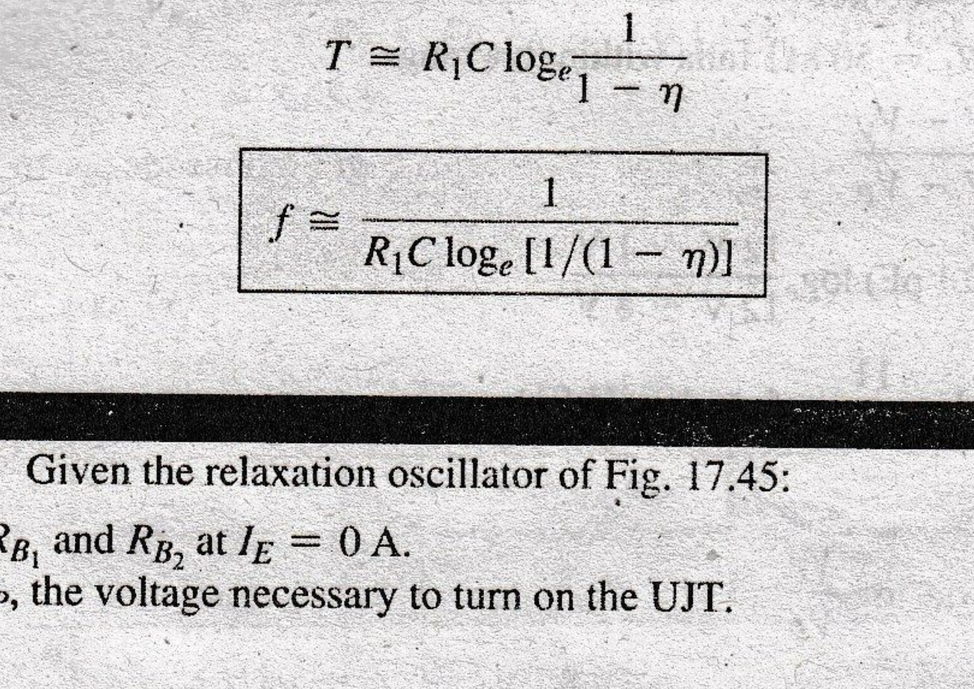


FIG. 17.45
Example 17.1.

c. Determine whether R_1 is within the permissible range of values as determined by Eq. (17.8) to ensure firing of the UJT.
d. Determine the frequency of oscillation if $R_{B_1} = 100\ \Omega$ during the discharge phase.
e. Sketch the waveform of v_C for a full cycle.
f. Sketch the waveform of v_{R_2} for a full cycle.

Solution:

a. $$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

$$0.6 = \frac{R_{B_1}}{R_{BB}}$$

$$R_{B_1} = 0.6R_{BB} = 0.6(5\ \text{k}\Omega) = \mathbf{3\ k\Omega}$$

$$R_{B_2} = R_{BB} - R_{B_1} = 5\ \text{k}\Omega - 3\ \text{k}\Omega = \mathbf{2\ k\Omega}$$

b. At the point where $v_C = V_P$, if we continue with $I_E = 0$ A, the network of Fig. 17.46 results, where

$$V_P = 0.7\ \text{V} + \frac{(R_{B_1} + R_2)12\ \text{V}}{\underbrace{R_{B_1} + R_{B_2}}_{R_{BB}} + R_2}$$

$$= 0.7\ \text{V} + \frac{(3\ \text{k}\Omega + 0.1\ \text{k}\Omega)12\ \text{V}}{5\ \text{k}\Omega + 0.1\ \text{k}\Omega} = 0.7\ \text{V} + 7.294\ \text{V}$$

$$\cong \mathbf{8\ V}$$

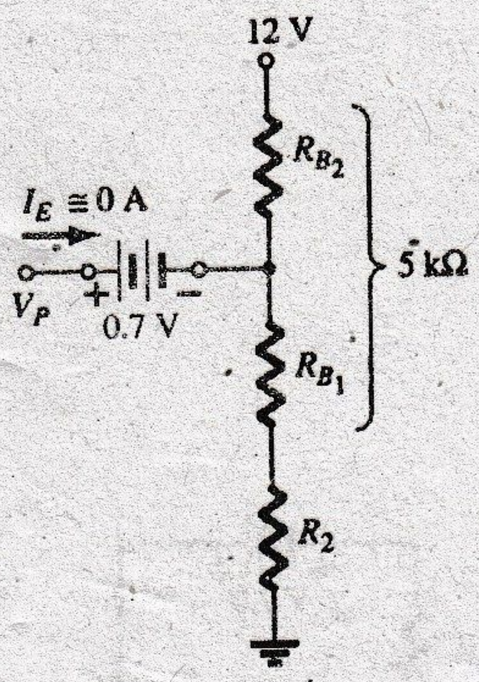


FIG. 17.46
Network for determining V_P, the voltage required to turn on the UJT.

c. $$\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P}$$

$$\frac{12\ \text{V} - 1\ \text{V}}{10\ m\text{A}} < R_1 < \frac{12\ \text{V} - 8\ \text{V}}{10\ \mu\text{A}}$$

$$1.1\ \text{k}\Omega < R_1 < 400\ \text{k}\Omega$$

The resistance $R_1 = 50\ \text{k}\Omega$ falls within this range.

d. $$t_1 = R_1 C \log_e \frac{V - V_V}{V - V_P}$$

$$= (50\ \text{k}\Omega)(0.1\ \text{pF}) \log_e \frac{12\ \text{V} - 1\ \text{V}}{12\ \text{V} - 8\ \text{V}}$$

$$= 5 \times 10^{-3} \log_e \frac{11}{4} = 5 \times 10^{-3}(1.01)$$

$$= 5.05\ \text{ms}$$

$$t_2 = (R_{B_1} + R_2) C \log_e \frac{V_P}{V_V}$$

$$= (0.1\ \text{k}\Omega + 0.1\ \text{k}\Omega)(0.1\ \text{pF}) \log_e \frac{8}{1}$$

$$= (0.02 \times 10^{-6})(2.08)$$

$$= 41.6\ \mu\text{s}$$

and $$T = t_1 + t_2 = 5.05\ \text{ms} + 0.0416\ \text{ms}$$

$$= 5.092\ \text{ms}$$

with $$f_{\text{osc}} = \frac{1}{T} = \frac{1}{5.092\ \text{ms}} \cong \mathbf{196\ Hz}$$

Using Eq. (17.17) gives

$$f \cong \frac{1}{R_1 C \log_e [1/(1 - \eta)]}$$

$$= \frac{1}{5 \times 10^{-3} \log_e 2.5}$$

$$= \mathbf{218\ Hz}$$

e. See Fig. 17.47.

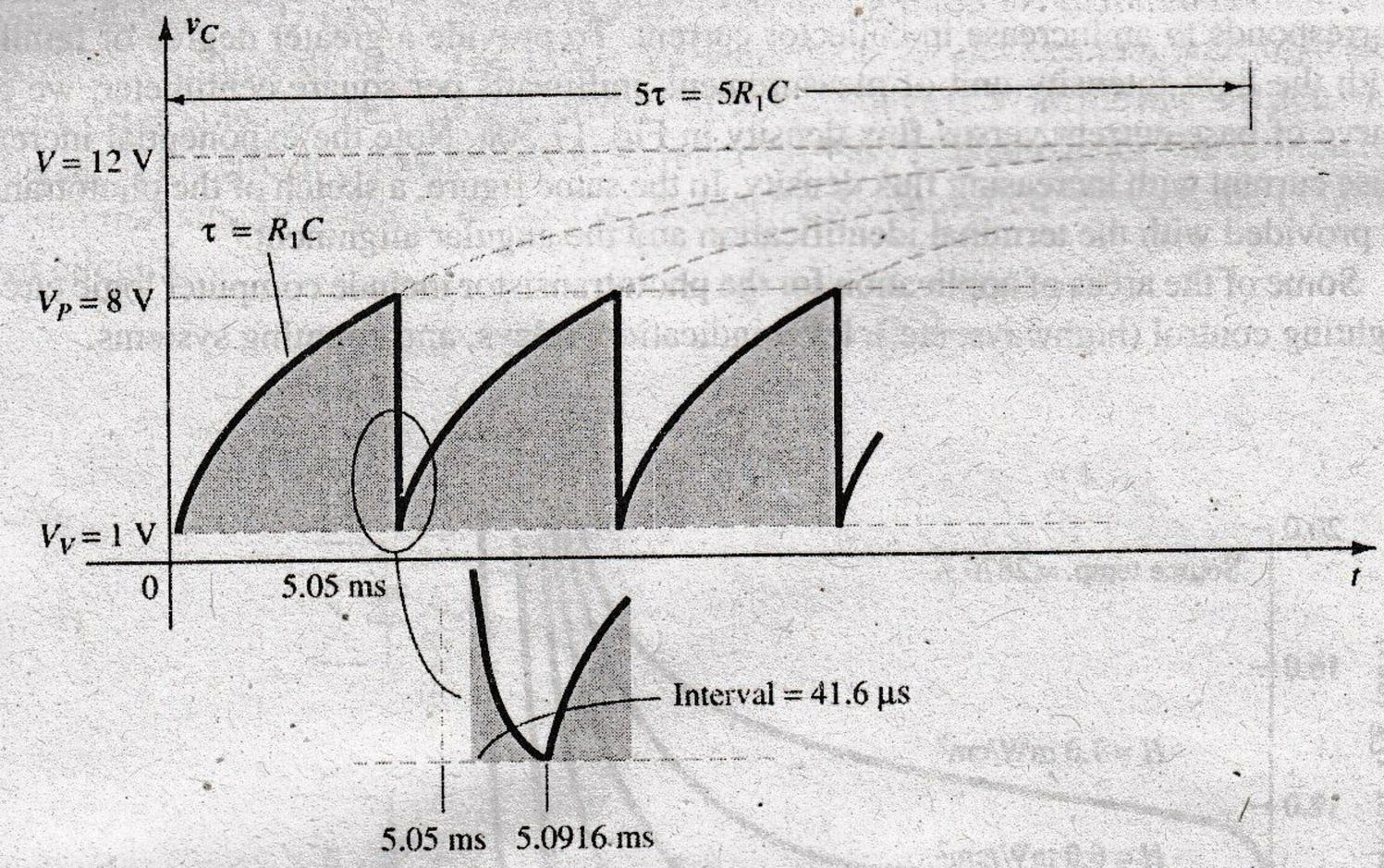


FIG. 17.47

The voltage v_C for the relaxation oscillator of Fig. 17.45.

f. During the charging phase, from (Eq. 17.9), we have

$$V_{R_2} = \frac{R_2 V}{R_2 + R_{BB}} = \frac{0.1\,\text{k}\Omega(12\,V)}{0.1\,\text{k}\Omega + 5\,\text{k}\Omega} = \mathbf{0.235\ V}$$

When $v_C = V_P$, from (Eq. 17.12), we have

$$V_{R_2} \cong \frac{R_2(V_P - 0.7\ \text{V})}{R_2 + R_{B_1}} = \frac{0.1\,\text{k}\Omega(8\ \text{V} - 0.7\ \text{V})}{0.1\,\text{k}\Omega + 0.1\,\text{k}\Omega}$$
$$= \mathbf{3.65\ V}$$

The plot of v_{R_2} appears in Fig. 17.48.

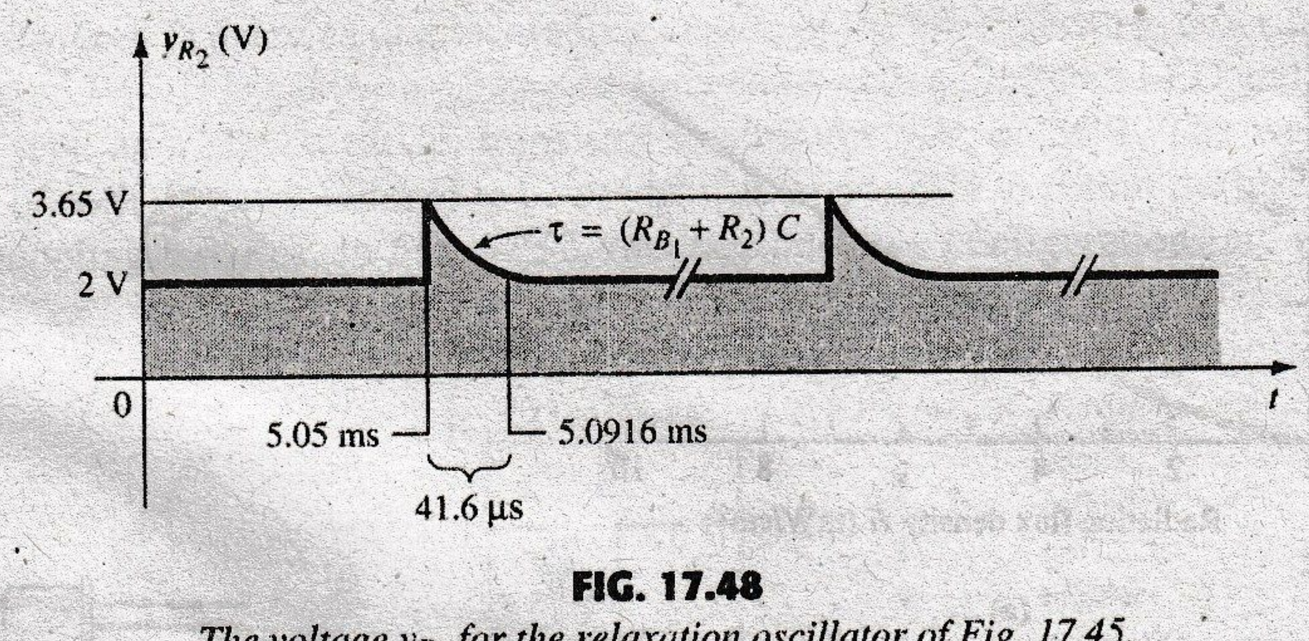


FIG. 17.48

The voltage v_{R_2} for the relaxation oscillator of Fig. 17.45.

17.13 PHOTOTRANSISTORS

The fundamental behavior of photoelectric devices was introduced earlier with the description of the photodiode. This discussion will now be extended to include the phototransistor, which has a photosensitive collector--base p–n junction. The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I_λ for the photoinduced base current, the resulting collector current, on an approximate basis, is

$$\boxed{I_C \cong h_{fe} I_\lambda} \qquad \textbf{(17.18)}$$