4 DC Biasing—BJTs

CHAPTER OBJECTIVES

- Be able to determine the dc levels for the variety of important BJT configurations.
- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.
- Be able to perform a load-line analysis of the most common BJT configurations.
- Become acquainted with the design process for BJT amplifiers.
- Understand the basic operation of transistor switching networks.
- Begin to understand the troubleshooting process as applied to BJT configurations.
- Develop a sense for the stability factors of a BJT configuration and how they affect its operation due to changes in specific characteristics and environmental changes.

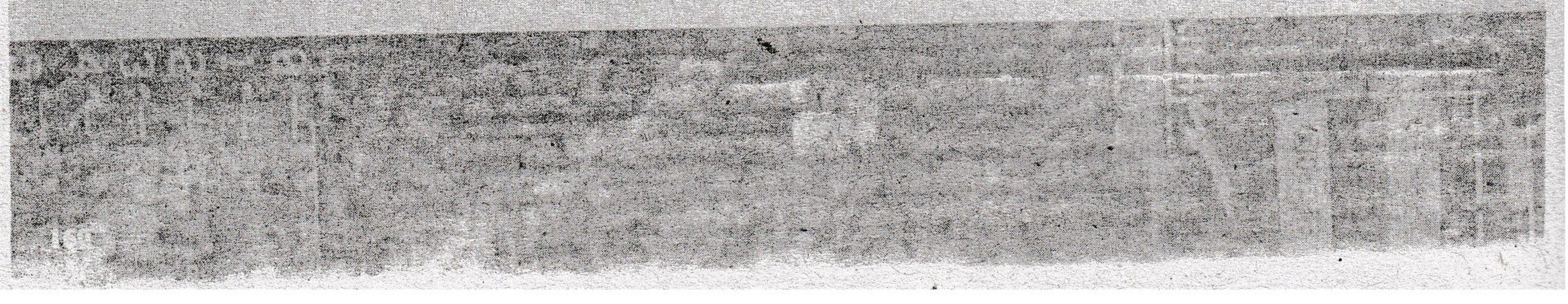
4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion. Fortunately, the superposition theorem is applicable, and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the bipolar junction transistor (BJT) amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.



Although a number of networks are analyzed in this chapter, there is an underlying similarity in the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$\boxed{V_{BE} \cong 0.7\ \text{V}} \tag{4.1}$$

$$\boxed{I_E = (\beta + 1)I_B \cong I_C} \tag{4.2}$$

$$\boxed{I_C = \beta I_B} \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated Q-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The

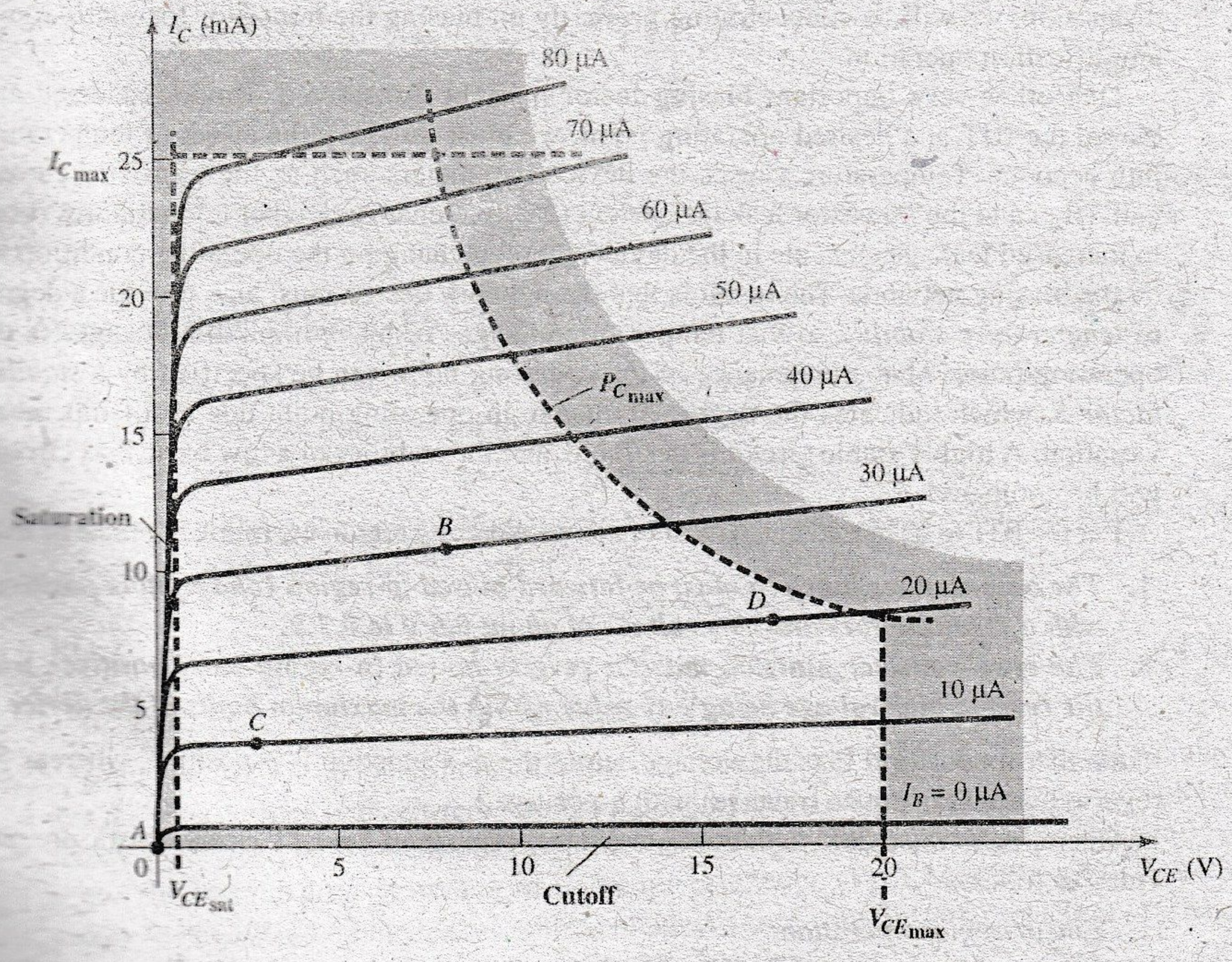


FIG. 4.1

Various operating points within the limits of operation of a transistor.

biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\ \mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{sat}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, we can select many different operating areas or points. The chosen Q-point often depends on the intended use of the circuit. Still, we can consider some differences among the various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a Q-point at A—namely, zero current through the device (and zero voltage across it). Because it is necessary to bias a device so that it can respond to the entire range of an input signal, point A would not be suitable. For point B, if a signal is applied to the circuit, the device will vary in current and voltage from the operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary, but not enough to drive the device into *cutoff* or *saturation.* Point C would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0$ V and $I_C = 0$ mA. Operating at point C also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point B is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point D sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point B therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 5) but not the case necessarily for power amplifiers, which will be considered in Chapter 12. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, we must also take the effect of temperature into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor S,* which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. ***The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.***
2. ***The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.***

[Note that for forward bias the voltage across the p–n junction is p-positive, whereas for reverse bias it is opposite (reverse) with n-positive.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction reverse-biased

2. *Cutoff-region operation:*
   Base–emitter junction reverse-biased
   Base–collector junction reverse-biased
3. *Saturation-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the *actual* current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency. For dc, $f = 0$ Hz, and $X_C = \frac{1}{2}\pi fC = \frac{1}{2}\pi(0)C = \infty\,\Omega$. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

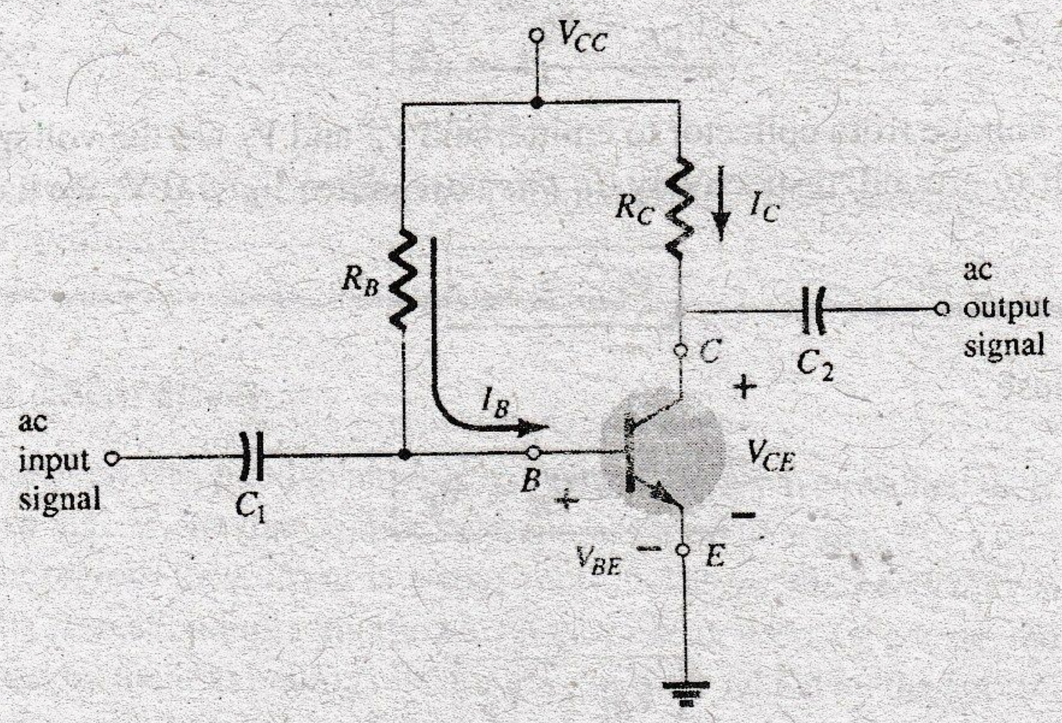


FIG. 4.2
Fixed-bias circuit.

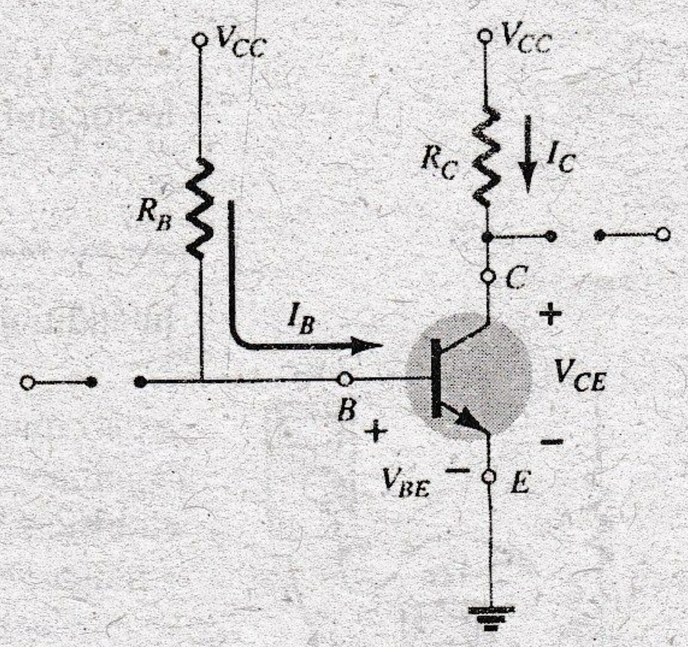


FIG. 4.3
DC equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B results in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}). In addition, because the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

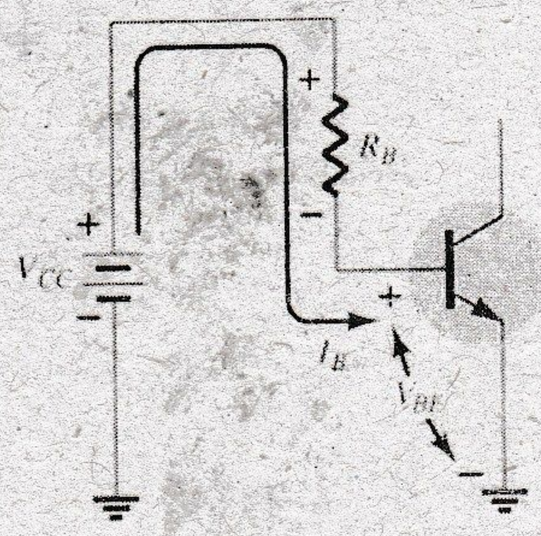


FIG. 4.4
Base–emitter loop.

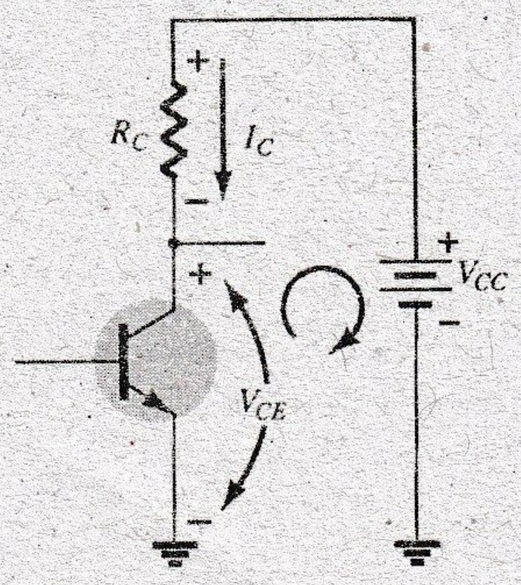


FIG. 4.5
Collector–emitter loop.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$\boxed{I_C = \beta I_B} \tag{4.5}$$

It is interesting to note that because the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{4.6}$$

which states that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$\boxed{V_{CE} = V_C - V_E} \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case,* since $V_E = 0$ V, we have

$$\boxed{V_{CE} = V_C} \tag{4.8}$$

In addition, because

$$\boxed{V_{BE} = V_B - V_E} \tag{4.9}$$

and $V_E = 0$ V, then

$$\boxed{V_{BE} = V_B} \tag{4.10}$$

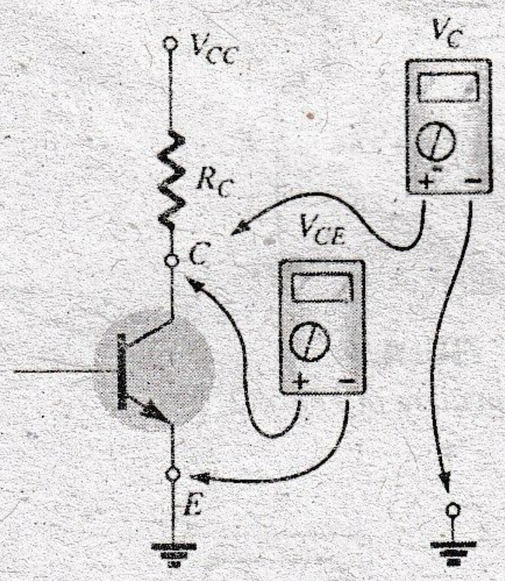


FIG. 4.6
Measuring V_{CE} and V_C.

Keep in mind that voltage levels such as V_{CE} are determined by placing the positive lead (normally red) of the voltmeter at the collector terminal with the negative lead (normally black) at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

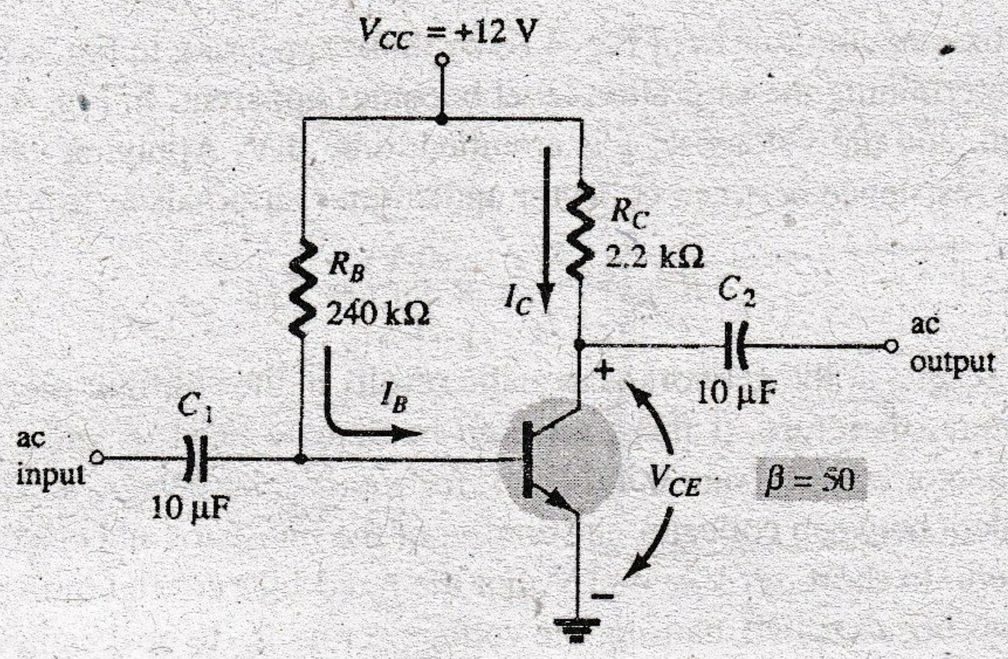


FIG. 4.7
DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6): $V_{CE_Q} = V_{CC} - I_C R_C$
$= 12\,\text{V} - (2.35\,\text{mA})(2.2\,\text{k}\Omega)$
$= \mathbf{6.83\,V}$

c. $V_B = V_{BE} = \mathbf{0.7\,V}$
$V_C = V_{CE} = \mathbf{6.83\,V}$

d. Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\,\text{V} - 6.83\,\text{V}$$
$$= \mathbf{-6.13\,V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of water. For a transistor operating in the saturation region, the current is a maximum value *for the particular design*. Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

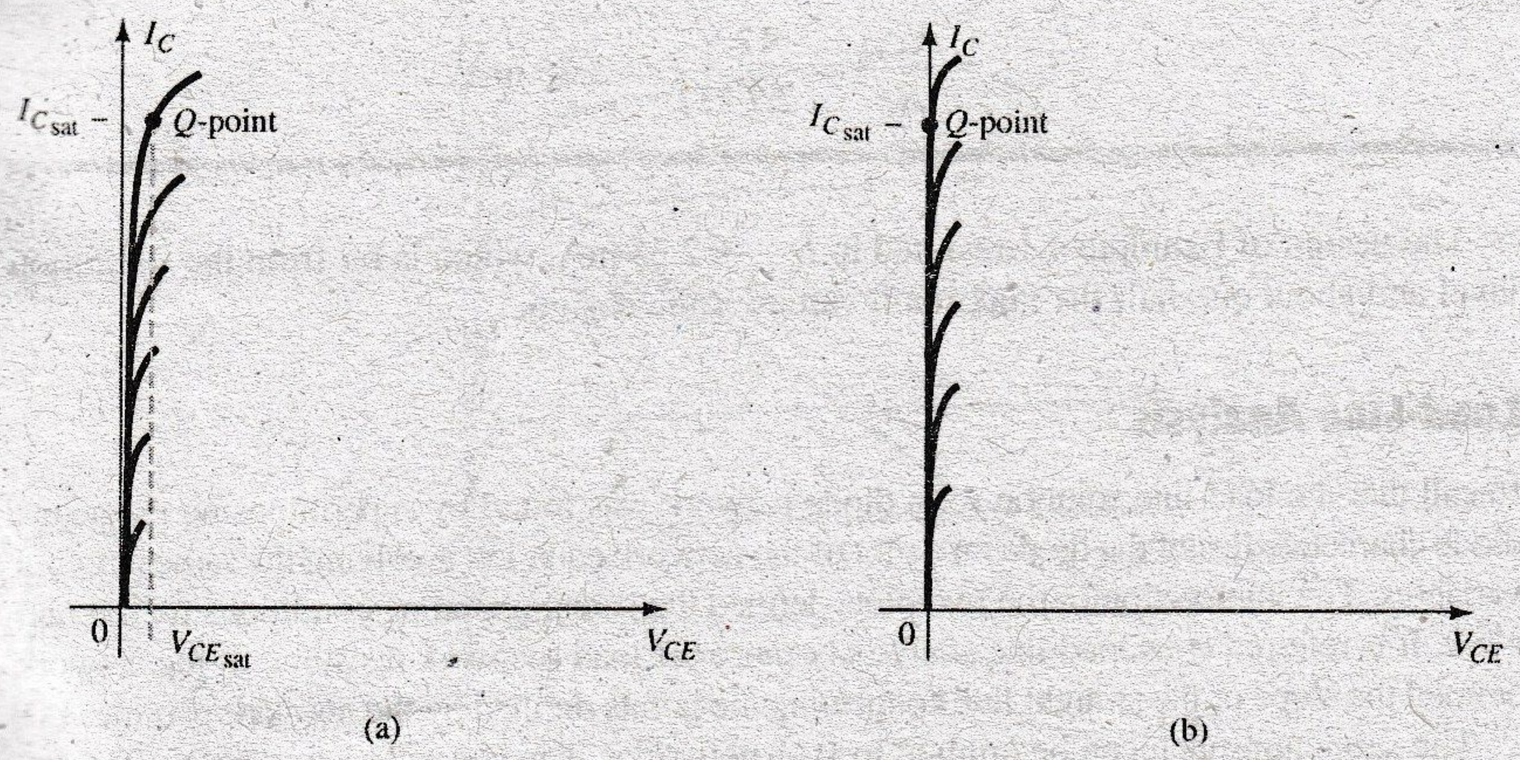


FIG. 4.8
Saturation regions: (a) actual; (b) approximate.

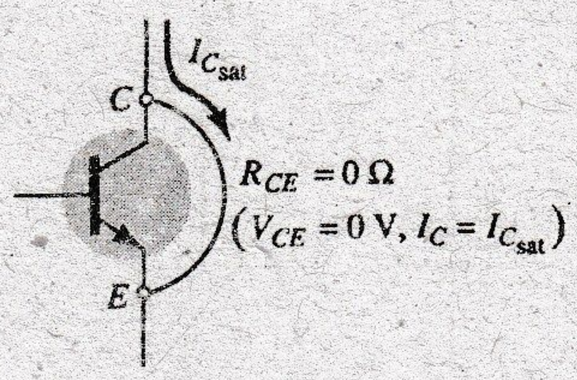


FIG. 4.9
Determining $I_{C_{sat}}$.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high, and the voltage V_{CE} is assumed to be 0 V. Applying Ohm's law, we can determine the resistance between collector and emitter terminals as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\,V}{I_{C_{sat}}} = 0\,\Omega$$

Applying the results to the network schematic results in the configuration of Fig. 4.9.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}} \qquad (4.11)$$

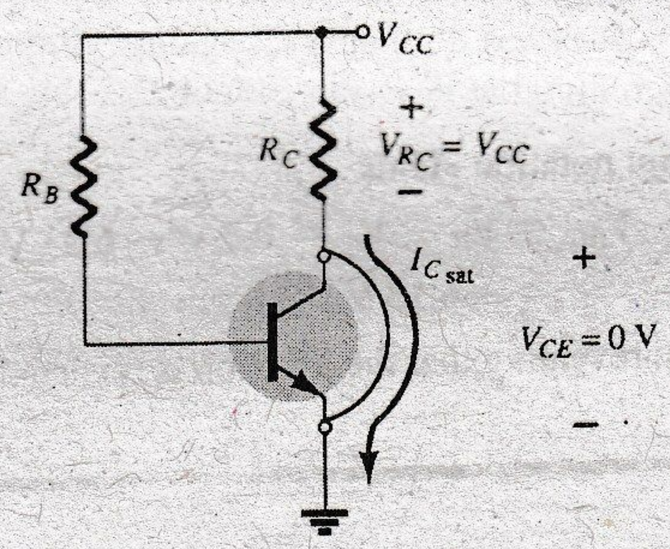


FIG. 4.10
Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once $I_{C_{sat}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\,V}{2.2\,k\Omega} = \mathbf{5.45\ mA}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

Recall that the load-line solution for a diode network was found by superimposing the actual diode characteristics of the diode on a plot of the network equation involving the same network variables. The intersection of the two plots defined the actual operating conditions for the network. It is referred to as load-line analysis because the load (network resistors) of the network defined the slope of the straight line connecting the points defined by the network parameters.

The same approach can be applied to BJT networks. The characteristics of the BJT are superimposed on a plot of the network equation defined by the same axis parameters. The load resistor R_C for the fixed-bias configuration will define the slope of the network equation and the resulting intersection between the two plots. The smaller the load resistance, the

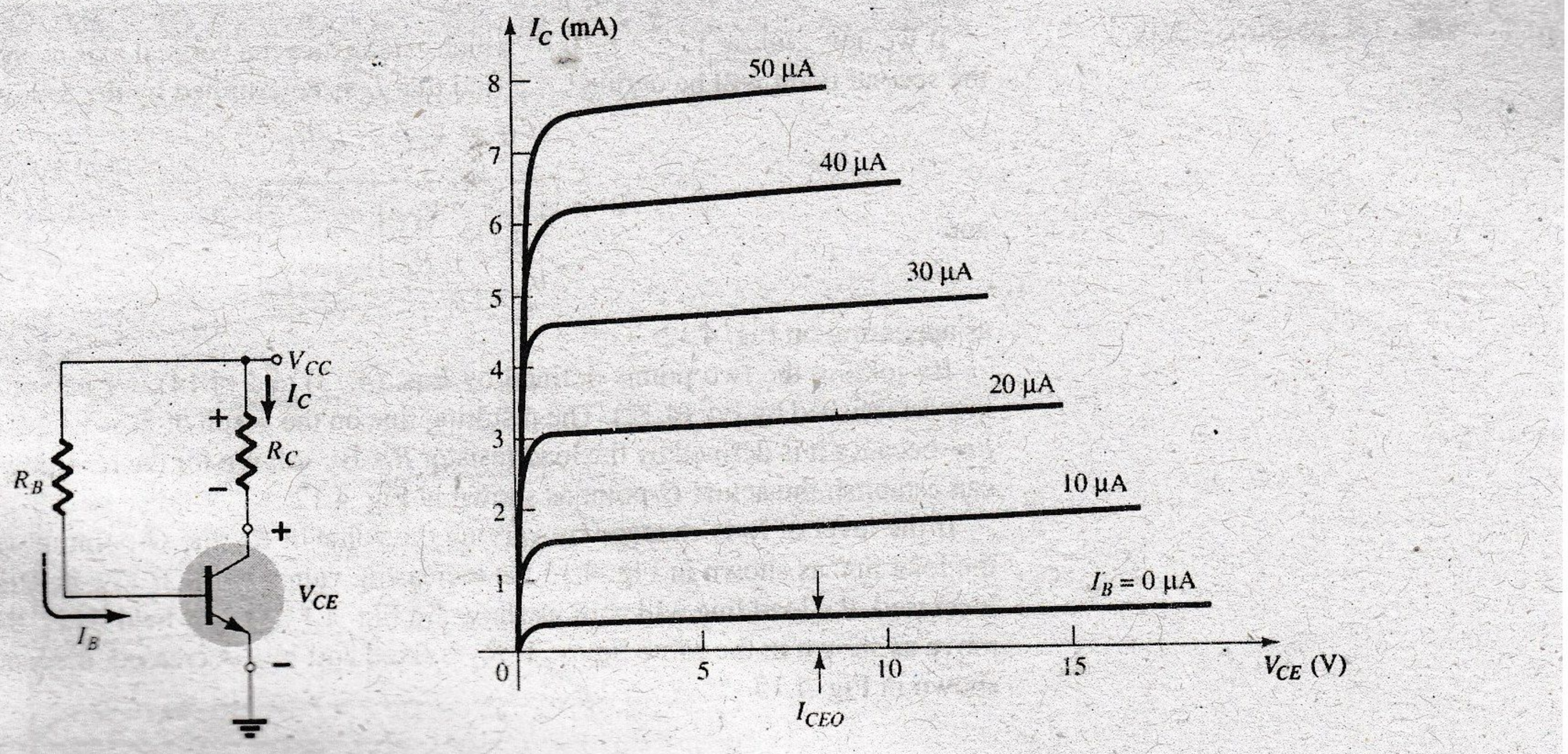


FIG. 4.11

Load-line analysis: (a) the network; (b) the device characteristics.

steeper the slope of the network load line. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$V_{CE} = V_{CC}|_{I_C = 0\,\text{mA}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

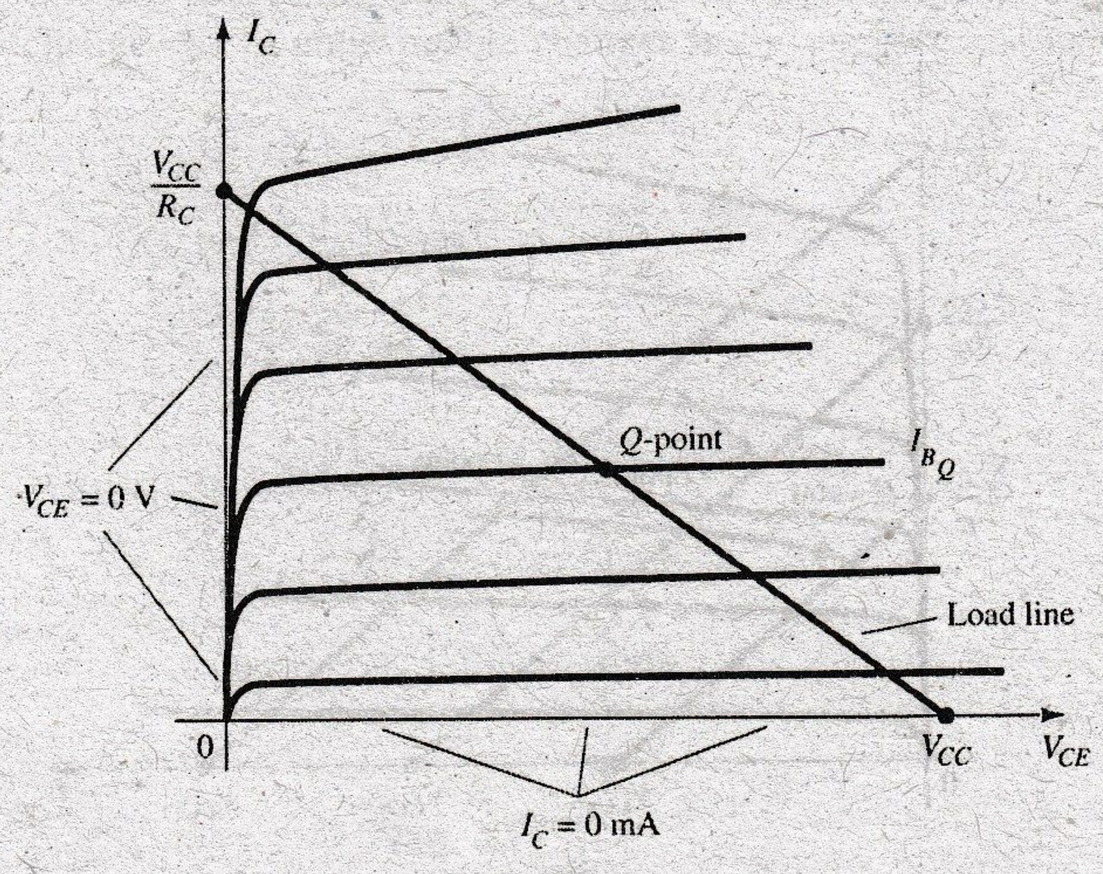


FIG. 4.12

Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$\boxed{I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\text{ V}}} \tag{4.14}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), we can draw the straight line established by Eq. (4.12). The resulting line on the graph of Fig. 4.12 is called the *load line* because it is defined by the load resistor R_C. By solving for the resulting level of I_B, we can establish the actual Q-point as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B, the Q-point moves up or down the load line as shown in Fig. 4.13 for increasing values of I_B. If V_{CC} is held fixed and R_C increased, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} decreased, the load line shifts as shown in Fig. 4.15.

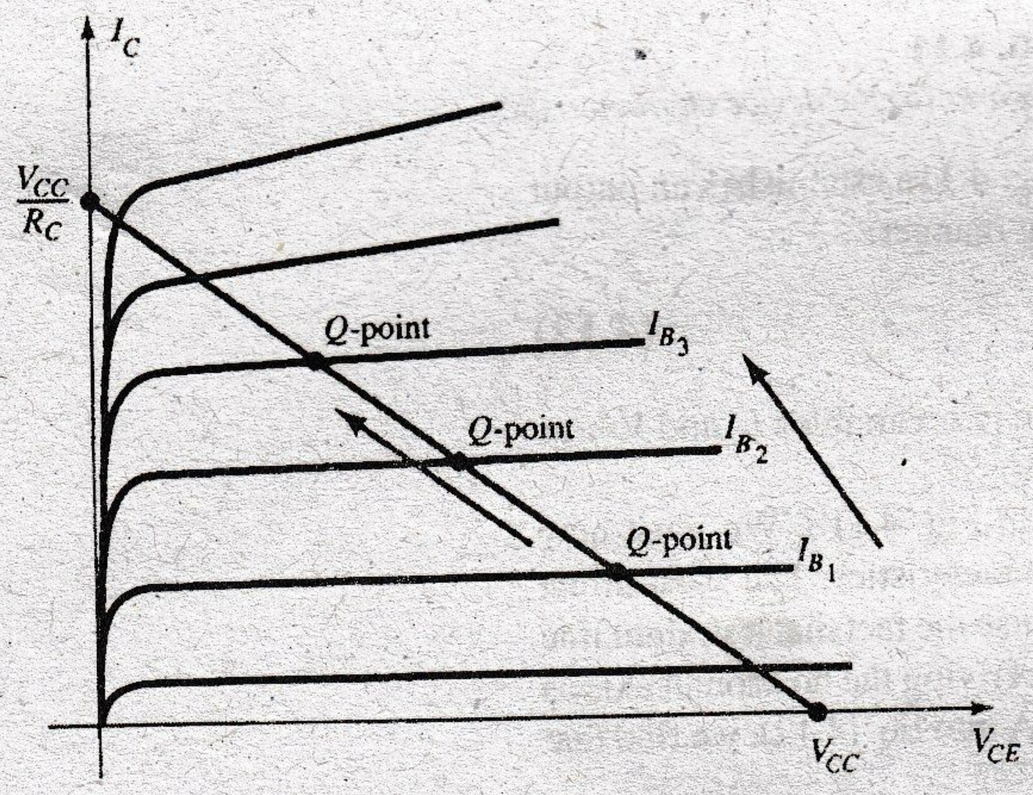


FIG. 4.13
Movement of the Q-point with increasing level of I_B.

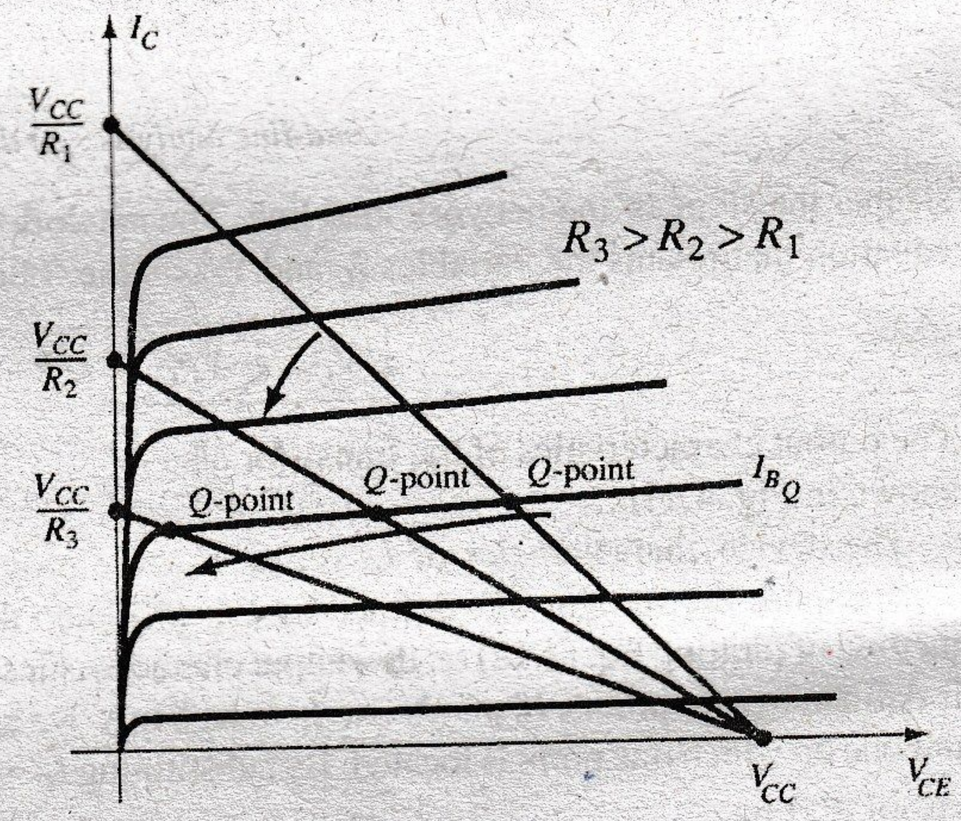


FIG. 4.14
Effect of an increasing level of R_C on the load line and the Q-point.

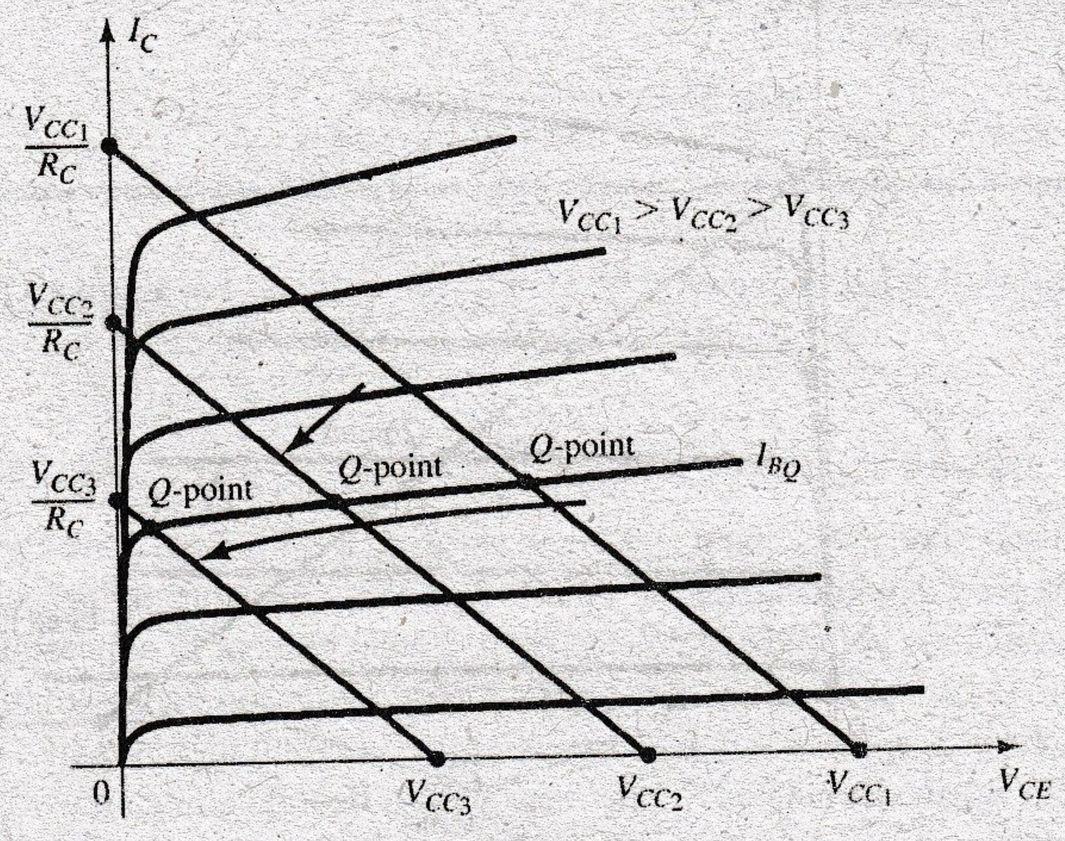


FIG. 4.15
Effect of lower values of V_{CC} on the load line and the Q-point.

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

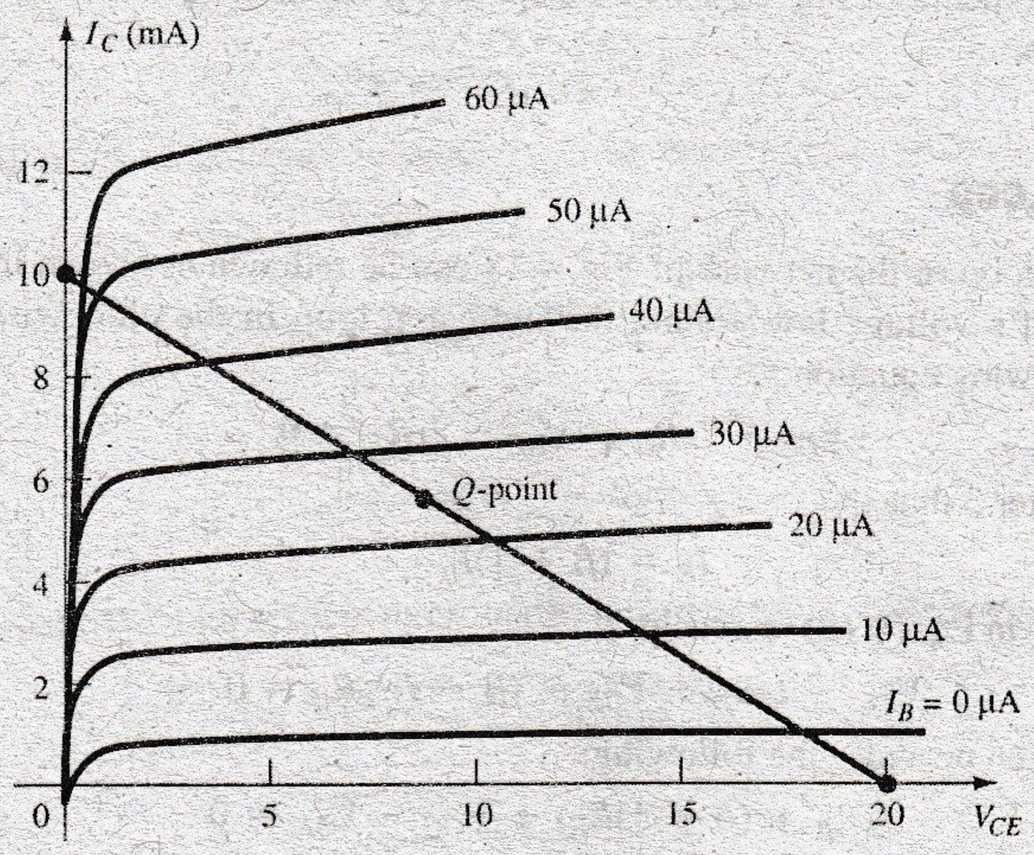


FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-BIAS CONFIGURATION

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The more stable a configuration, the less its response will change due to undesireable changes in temperature and parameter

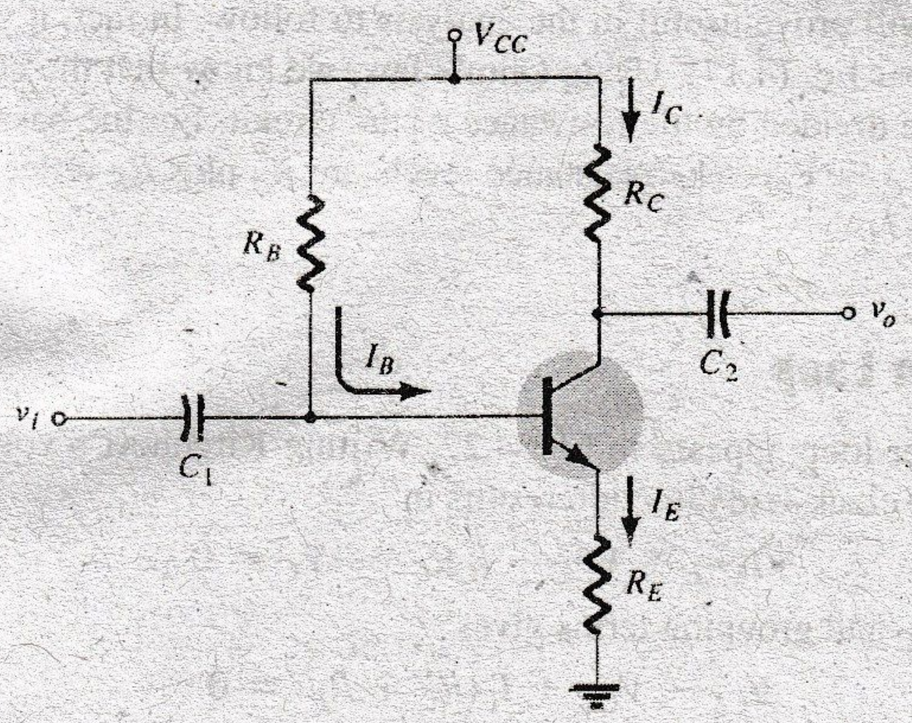


FIG. 4.17
BJT bias circuit with emitter resistor.

variations. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop. The dc equivalent of Fig. 4.17 appears in Fig 4.18 with a separation of the source to create an input and output section.

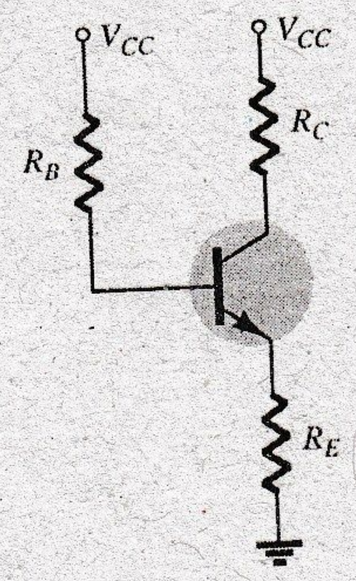


FIG. 4.18
DC equivalent of Fig. 4.17.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.18 can be redrawn as shown in Fig. 4.19. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \tag{4.15}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \tag{4.16}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{4.17}$$

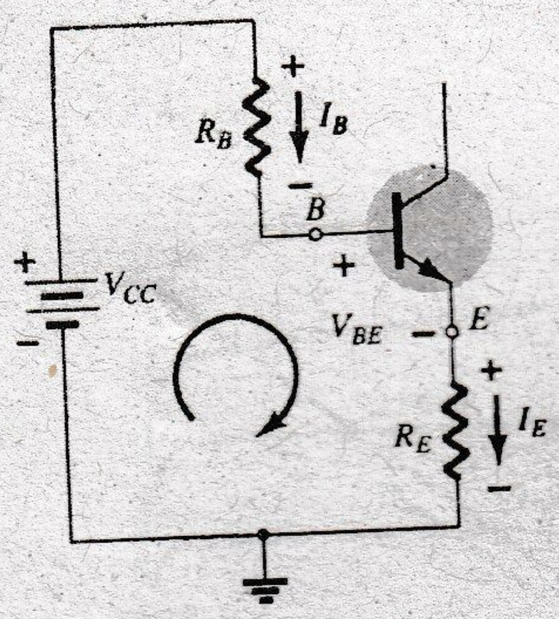


FIG. 4.19
Base–emitter loop.

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of Fig. 4.20. Solving for the current I_B results in the same equation as obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base–emitter loop. Because β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.21,

$$\boxed{R_i = (\beta + 1)R_E} \tag{4.18}$$

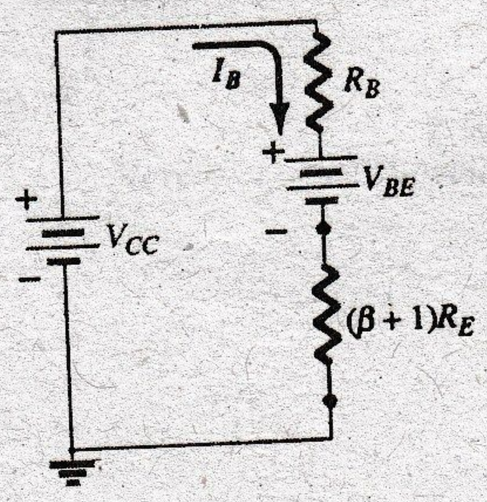


FIG. 4.20
Network derived from Eq. (4.17).

Equation (4.18) will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base–emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

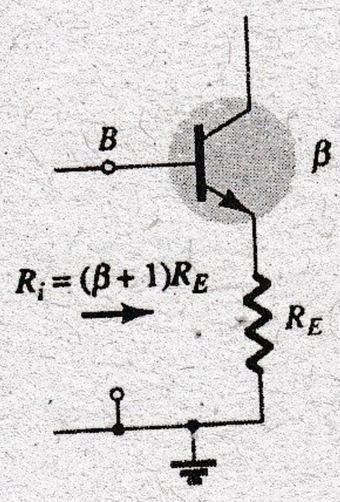


FIG. 4.21
Reflected impedance level of R_E.

Collector–Emitter Loop

The collector–emitter loop appears in Fig. 4.22. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.19}$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \tag{4.20}$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \tag{4.21}$$

or

$$V_C = V_{CC} - I_C R_C \tag{4.22}$$

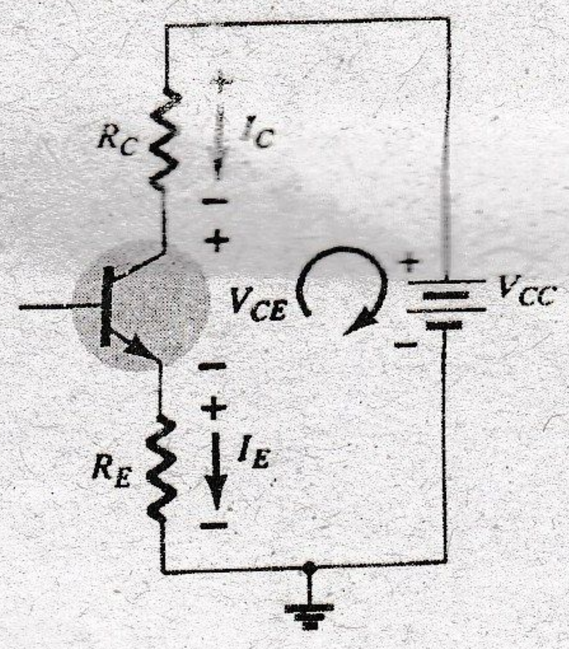


FIG. 4.22
Collector–emitter loop.

The voltage at the base with respect to ground can be determined using Fig. 4.18

$$V_B = V_{CC} - I_B R_B \tag{4.23}$$

or

$$V_B = V_{BE} + V_E \tag{4.24}$$

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

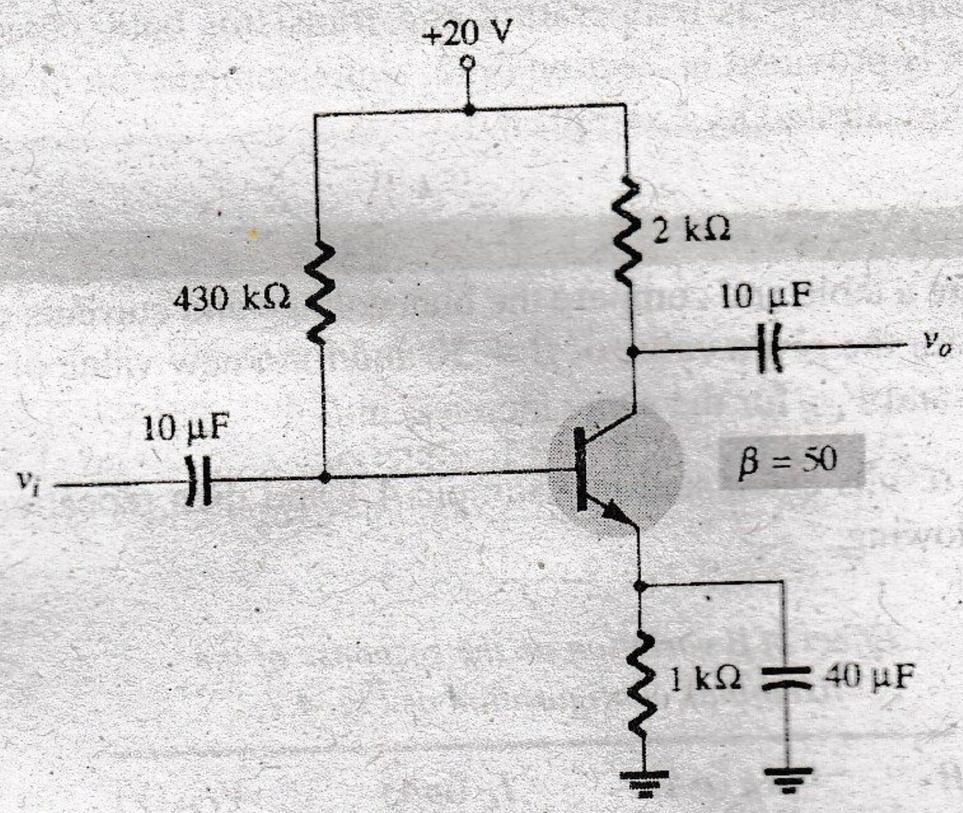


FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17):
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\text{ V}}$

d. $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\text{ V}}$

e. $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\text{ V}}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\text{ V}}$

f. $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\text{ V}}$

g. $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\text{ V}}$ (reverse-biased as required)

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change. Although a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5 Prepare a table and compare the bias voltage and currents of the circuits of Fig. 4.7 and Fig. 4.23 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution: Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

Effect of β variation on the response of the fixed-bias configuration of Fig. 4.7.

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. The value of I_B is the same, and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

Effect of β variation on the response of the emitter-bias configuration of Fig. 4.23.

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C—or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.23 is therefore more stable than that of Fig. 4.7 for the same change in β.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.24 and calculate the resulting collector current. For Fig. 4.24

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \tag{4.25}$$

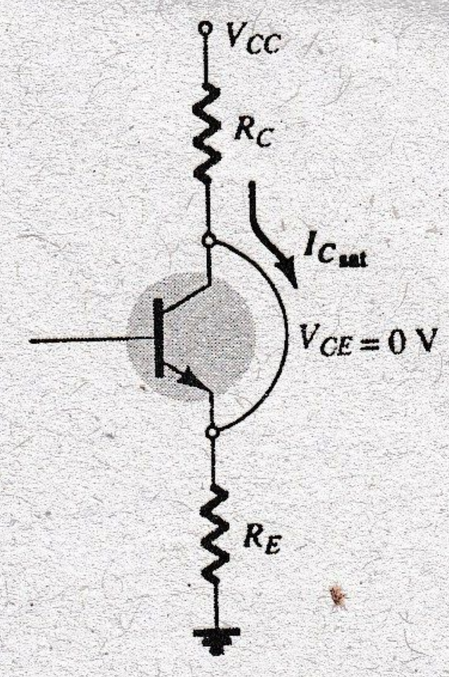


FIG. 4.24
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

EXAMPLE 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$

$$= \mathbf{6.67\text{ mA}}$$

which is about three times the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.25 (denoted I_{B_Q}).

The collector–emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

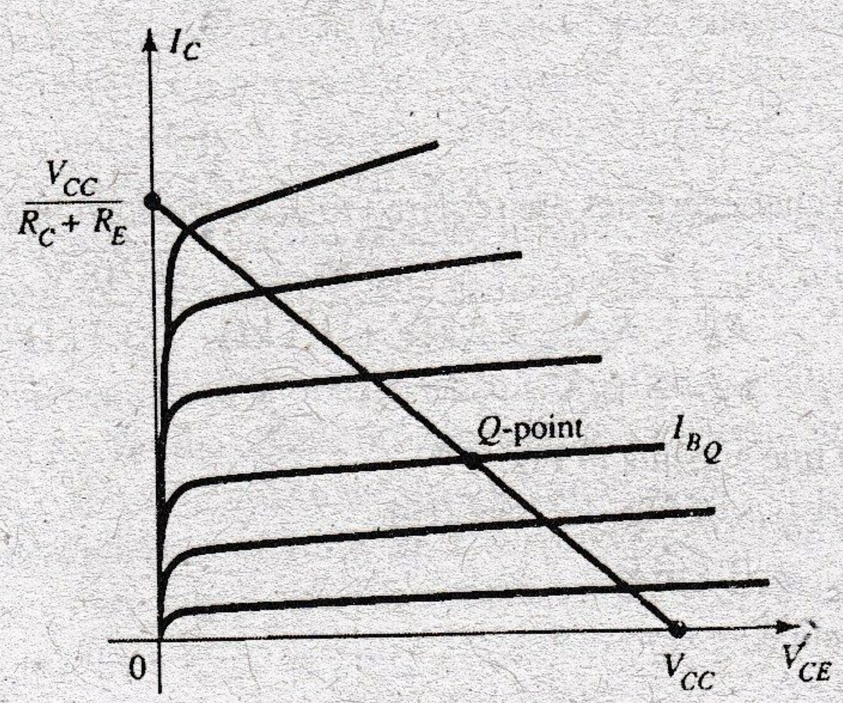


FIG. 4.25
Load line for the emitter-bias configuration.

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}|_{I_C=0\text{ mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\text{ V}}} \tag{4.27}$$

as shown in Fig. 4.25. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.

EXAMPLE 4.7

a. Draw the load line for the network of Fig. 4.26a on the characteristics for the transistor appearing in Fig. 4.26b.
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

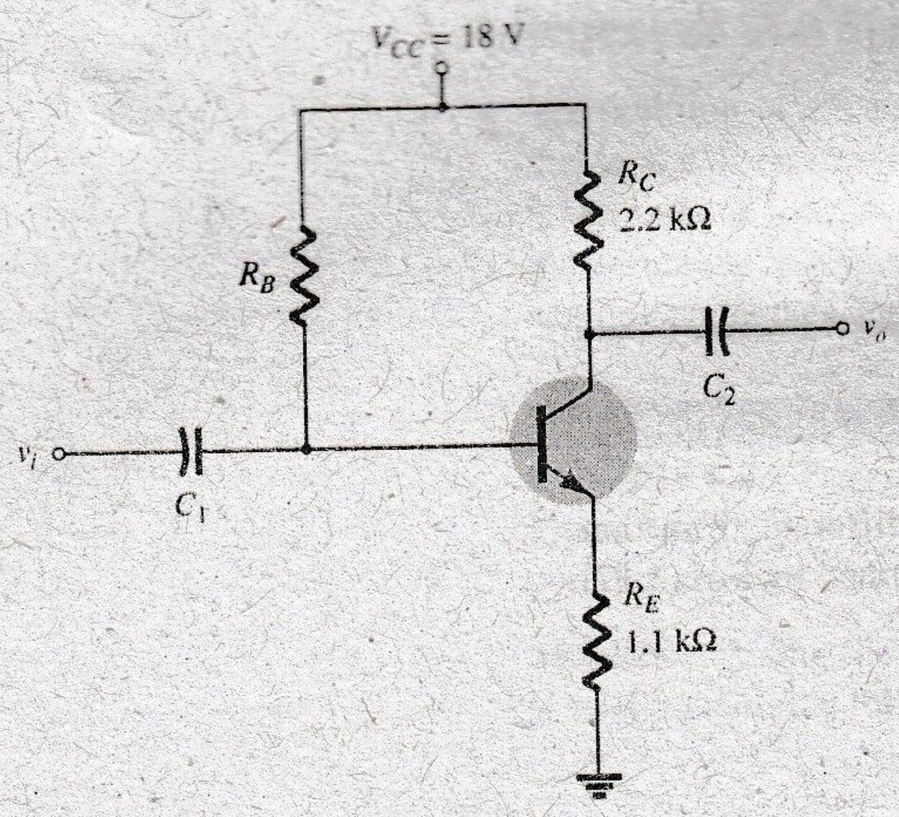


FIG. 4.26a
Network for Example 4.7.

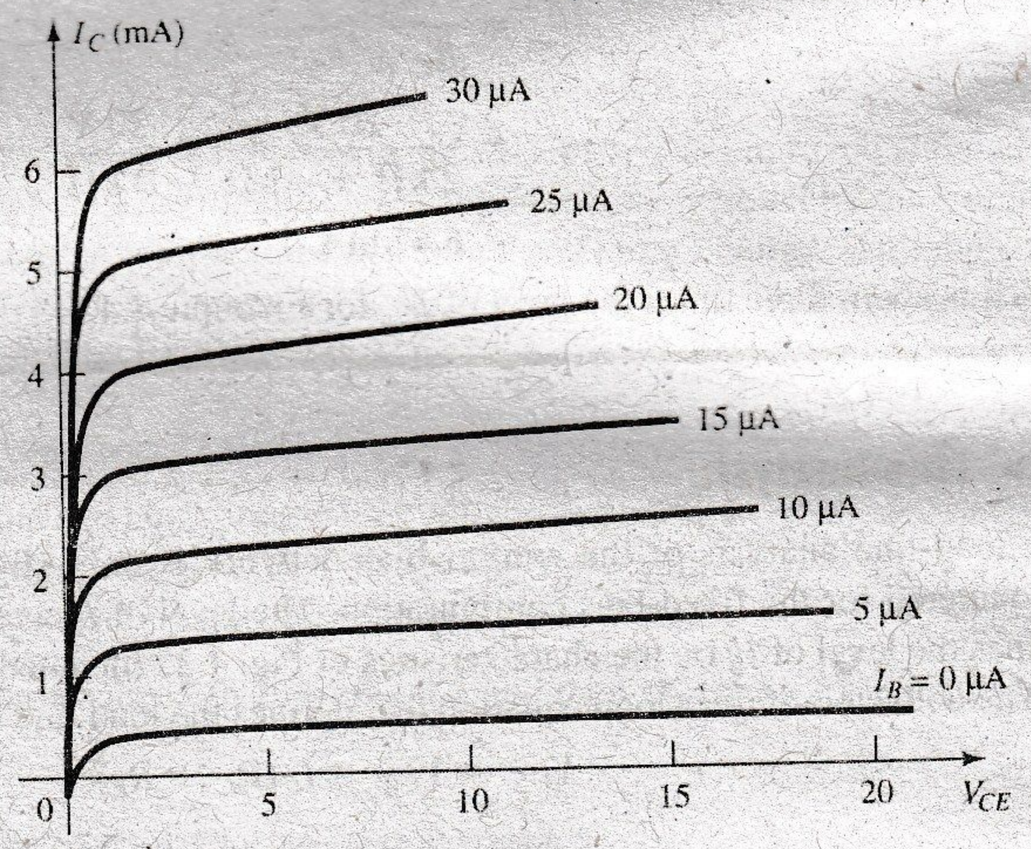


FIG. 4.26b
Example 4.7.

Solution:

a. Two points on the characteristics are required to draw the load line.

$$\text{At } V_{CE} = 0\text{ V}: \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{18\text{ V}}{2.2\text{ k}\Omega + 1.1\text{ k}\Omega} = \frac{18\text{ V}}{3.3\text{ k}\Omega} = 5.45\text{ mA}$$

$$\text{At } I_C = 0\text{ mA}: V_{CE} = V_{CC} = 18\text{ V}$$

The resulting load line appears in Fig. 4.27.

b. From the characteristics of Fig. 4.27 we find

$$V_{CE_Q} \cong \mathbf{7.5\text{ V}}, I_{C_Q} \cong \mathbf{3.3\text{ mA}}$$

c. The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3\text{ mA}}{15\ \mu\text{A}} = \mathbf{220}$$

-13(B)

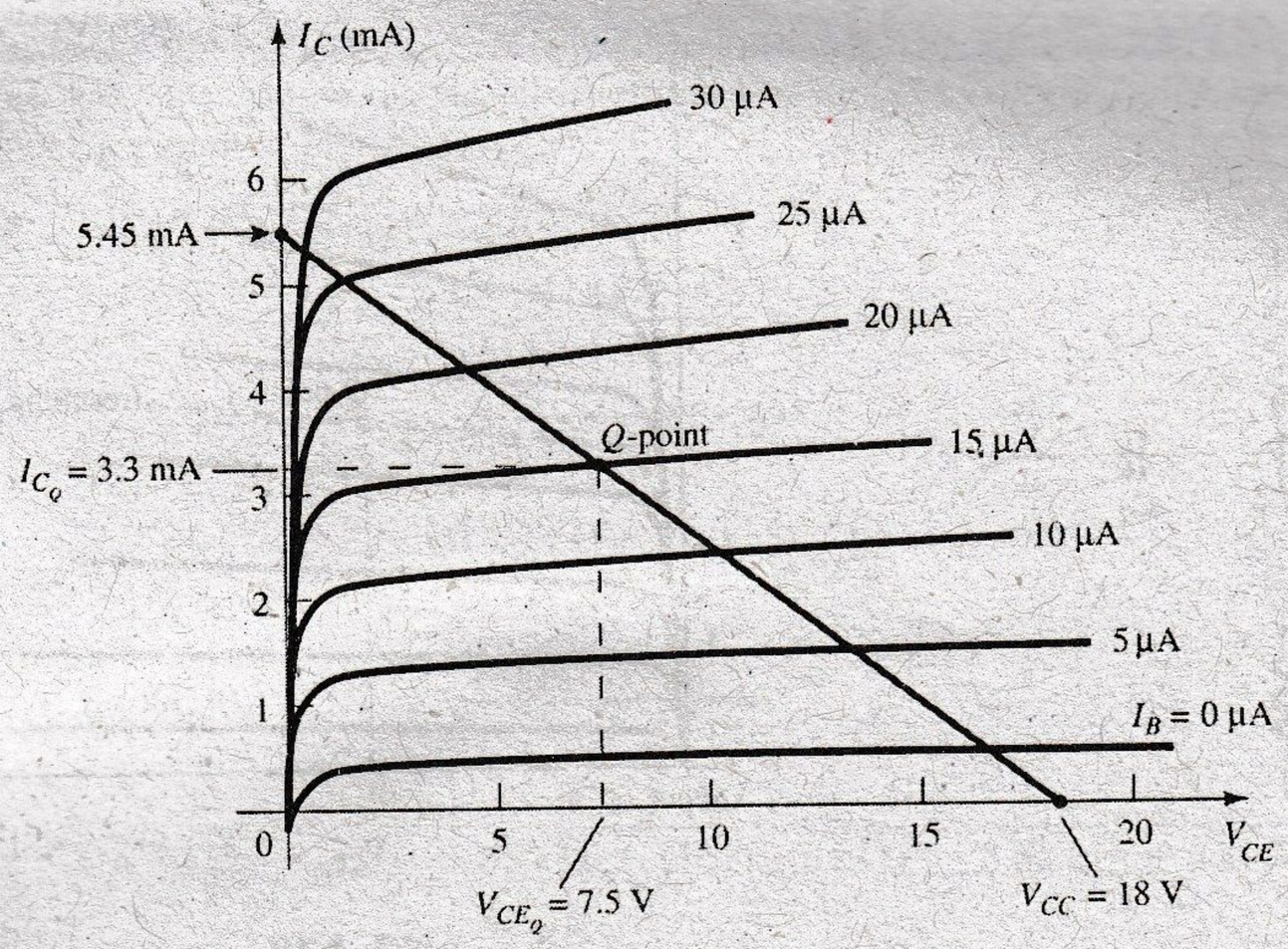


FIG. 4.27
Example 4.7.

d. Applying Eq. 4.17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18\text{ V} - 0.7\text{ V}}{R_B + (220 + 1)(1.1\text{ k}\Omega)}$$

$$\text{and } 15\,\mu\text{A} = \frac{17.3\text{ V}}{R_B + (221)(1.1\text{ k}\Omega)} = \frac{17.3\text{ V}}{R_B + 243.1\text{ k}\Omega}$$

$$\text{so that } (15\,\mu\text{A})(R_B) + (15\,\mu\text{A})(243.1\text{ k}\Omega) = 17.3\text{ V}$$

$$\text{and } (15\,\mu\text{A})(R_B) = 17.3\text{ V} - 3.65\text{ V} = 13.65\text{ V}$$

$$\text{resulting in } R_B = \frac{13.65\text{ V}}{15\,\mu\text{A}} = \mathbf{910\,k\Omega}$$

4.5 VOLTAGE-DIVIDER BIAS CONFIGURATION

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.28 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.29. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted earlier, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

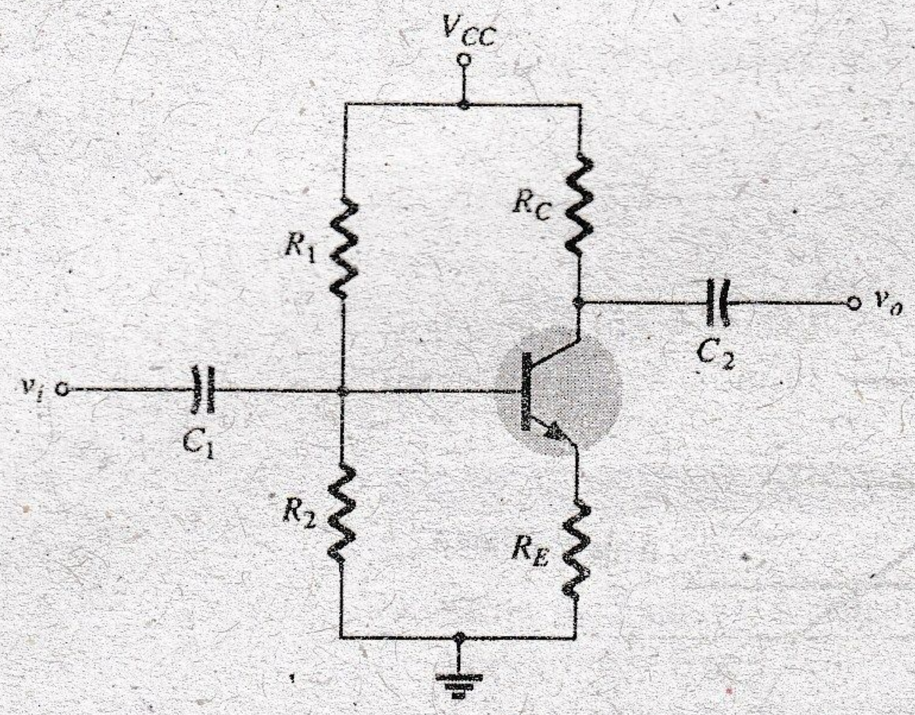


FIG. 4.28
Voltage-divider bias configuration.

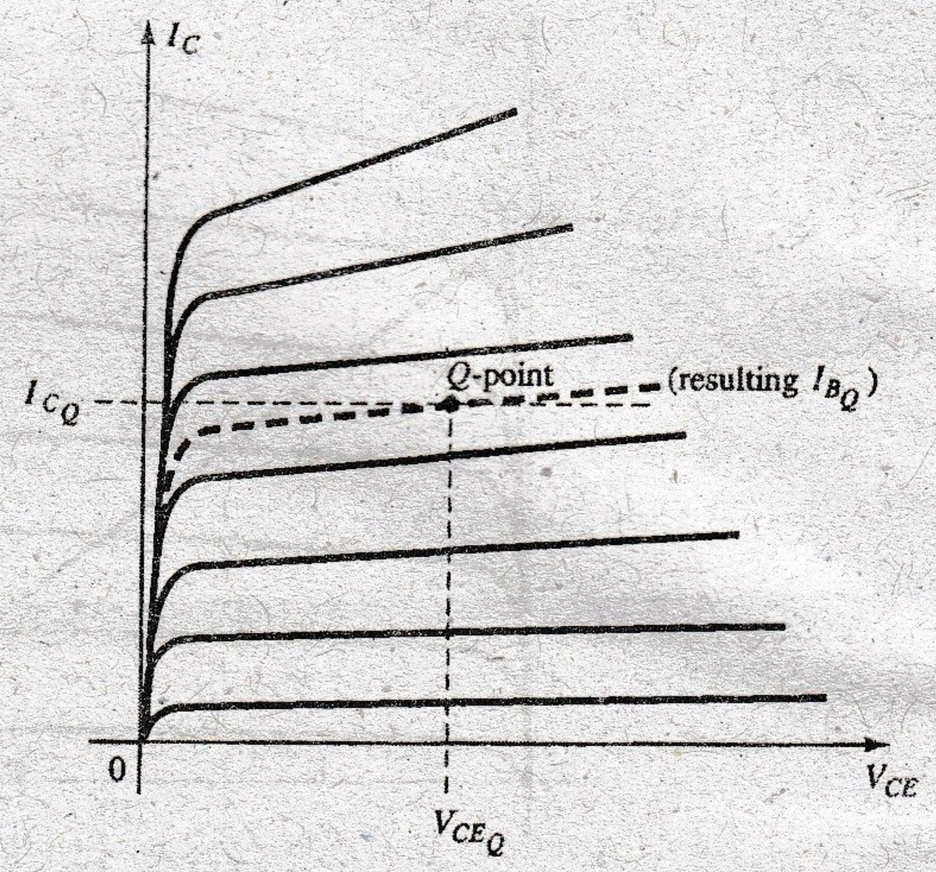


FIG. 4.29
Defining the Q-point for the voltage-divider bias configuration.

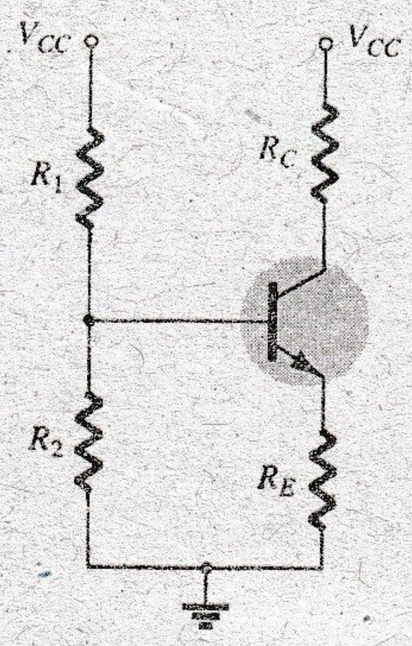


FIG. 4.30
DC components of the voltage-divider configuration.

Exact Analysis

For the dc analysis the network of Fig. 4.28 can be redrawn as shown in Fig. 4.30. The input side of the network can then be redrawn as shown in Fig. 4.31 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

R_{Th} The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.32:

$$R_{Th} = R_1 \| R_2 \tag{4.28}$$

E_{Th} The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.33 determined as follows:

Applying the voltage-divider rule gives

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$

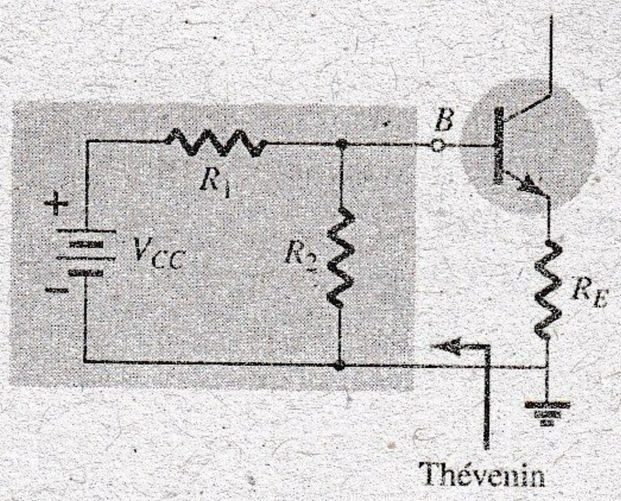


FIG. 4.31
Redrawing the input side of the network of Fig. 4.28.

The Thévenin network is then redrawn as shown in Fig. 4.34, and I_{B_Q} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \tag{4.30}$$

Although Eq. (4.30) initially appears to be different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.31}$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

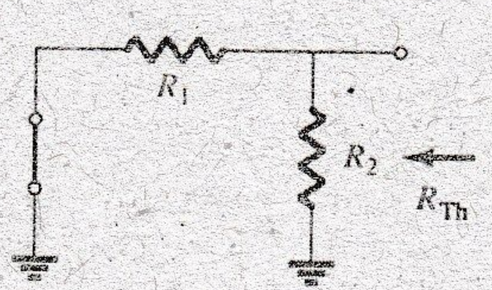


FIG. 4.32
Determining R_{Th}.

EXAMPLE 4.8 Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.35.

Solution: Eq. (4.28): $R_{Th} = R_1 \| R_2$

$$= \frac{(39\,\text{k}\Omega)(3.9\,\text{k}\Omega)}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 3.55\,\text{k}\Omega$$

Eq. (4.29): $E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$

$$= \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Eq. (4.30): $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$

$$= \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (101)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 151.5\,\text{k}\Omega}$$

$$= 8.38\,\mu\text{A}$$

$$I_C = \beta I_B$$

$$= (100)(8.38\,\mu\text{A})$$

$$= \mathbf{0.84\,mA}$$

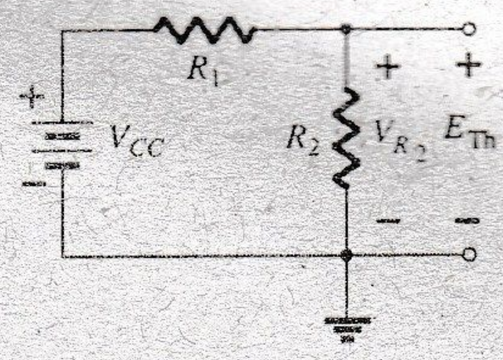


FIG. 4.33
Determining E_{Th}.

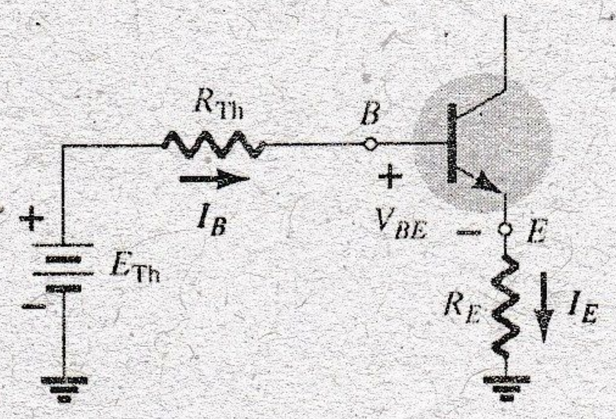


FIG. 4.34
Inserting the Thévenin equivalent circuit.

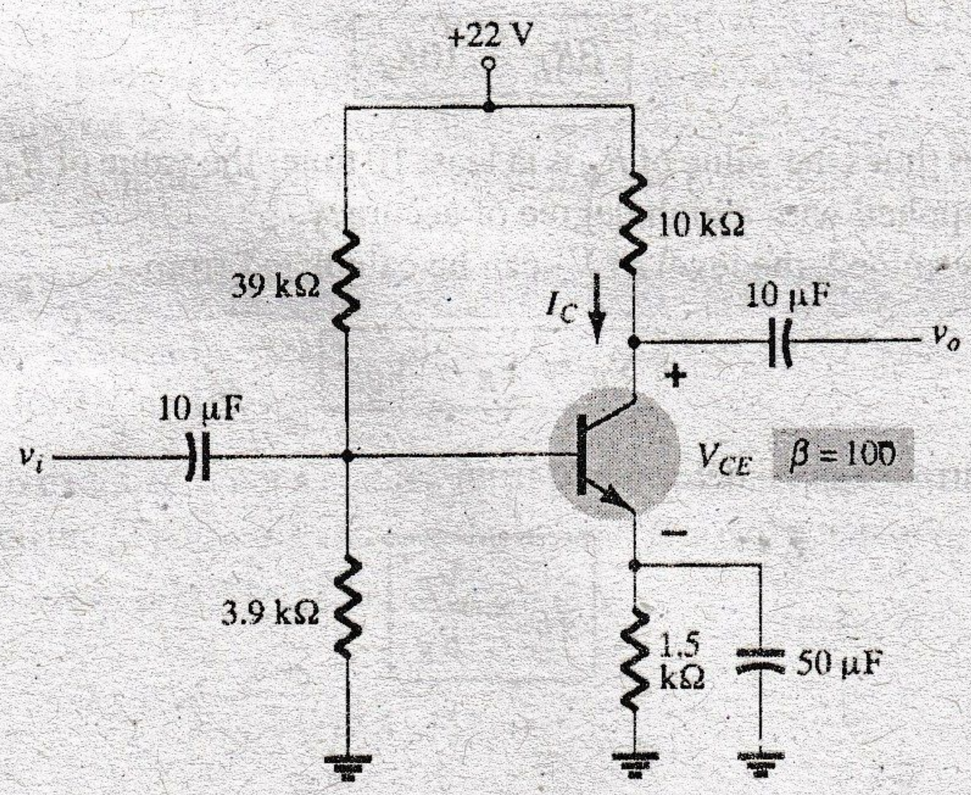


FIG. 4.35
Beta-stabilized circuit for Example 4.8.

Eq. (4.31): $V_{CE} = V_{CC} - I_C(R_C + R_E)$

$$= 22\,\text{V} - (0.84\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega)$$

$$= 22\,\text{V} - 9.66\,\text{V}$$

$$= \mathbf{12.34\,V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.36. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially 0 A compared to I_1 or I_2, then $I_1 = I_2$, and R_1 and R_2 can be considered series elements. The voltage across R_2, which is actually the base voltage, can be

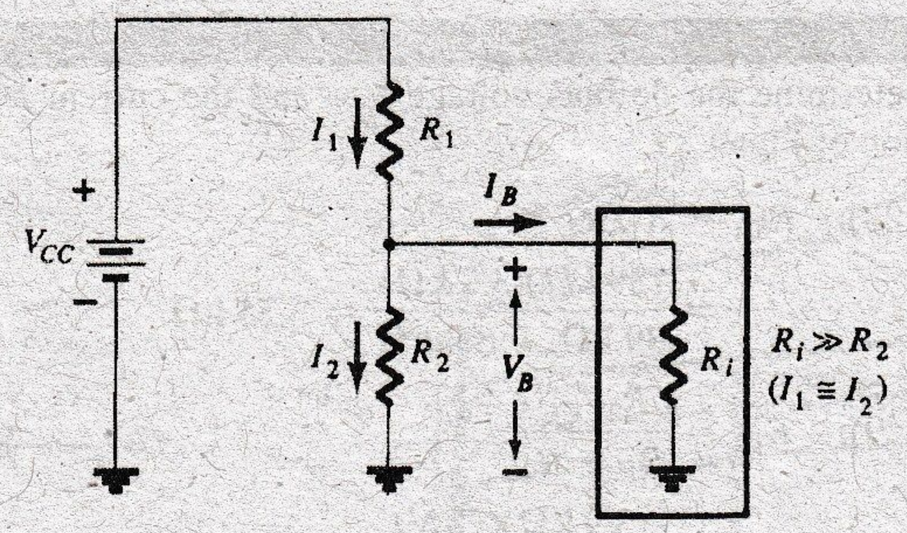


FIG. 4.36
Partial-bias circuit for calculating the approximate base voltage V_B.

determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.32}$$

Because $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied is

$$\beta R_E \geq 10R_2 \tag{4.33}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE} \tag{4.34}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \tag{4.35}$$

and

$$I_{C_Q} \cong I_E \tag{4.36}$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) \tag{4.37}$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{C_Q} and V_{CE_Q}) is therefore independent of the value of β.

EXAMPLE 4.9 Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: Testing:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\ \text{k}\Omega) \geq 10(3.9\ \text{k}\Omega)$$
$$150\ \text{k}\Omega \geq 39\ \text{k}\Omega\ (\textit{satisfied})$$

$$\text{Eq. (4.32):} \quad V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\text{Eq. (4.34):} \quad V_E = V_B - V_{BE} = 2\,\text{V} - 0.7\,\text{V} = 1.3\,\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\,\text{V}}{1.5\,\text{k}\Omega} = \mathbf{0.867\,mA}$$

compared to 0.84 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.867\,\text{mA})(10\,\text{kV} + 1.5\,\text{k}\Omega) = 22\,\text{V} - 9.97\,\text{V} = \mathbf{12.03\,V}$$

versus 12.34 V obtained in Example 4.8.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer is the approximate to the exact solution. Example 4.11 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.10 Repeat the exact analysis of Example 4.8 if β is reduced to 50, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: This example is not a comparison of exact versus approximate methods, but a testing of how much the Q-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{\text{Th}} = 3.55\,\text{k}\Omega, \qquad E_{\text{Th}} = 2\,\text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (51)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 76.5\,\text{k}\Omega}$$

$$= 16.24\,\mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(16.24\,\mu\text{A}) = \mathbf{0.81\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.81\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega) = \mathbf{12.69\,V}$$

Tabulating the results, we have:

Effect of β variation on the response of the voltage-divider configuration of Fig. 4.35.

β	I_{C_Q} (mA)	V_{CE_Q} (V)
100	0.84 mA	12.34 V
50	0.81 mA	12.69 V

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 100 to 50, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.

Important Note: Looking back on the results for the fixed-bias configuration, we find the current decreased from 4.71 mA to 2.35 mA when beta dropped from 100 to 50. For the voltage-divider configuration, the same change in beta only resulted in a change in current from 0.84 mA to 0.81 mA. Even more noticeable is the change in V_{CE_Q} for the fixed-bias configuration. Dropping beta from 100 to 50 resulted in an increase in voltage from 1.64 to 6.83 V (a change of over 300%). For the voltage-divider configuration, the increase in voltage was only from 12.34 V to 12.69 V, which is a change of less than 3%. In summary, therefore, changing beta by 50% resulted in a change in an important network parameter of over 300% for the fixed-bias configuration and less than 3% for the voltage-divider configuration—a significant difference.

EXAMPLE 4.11 Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) *will not be satisfied* and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

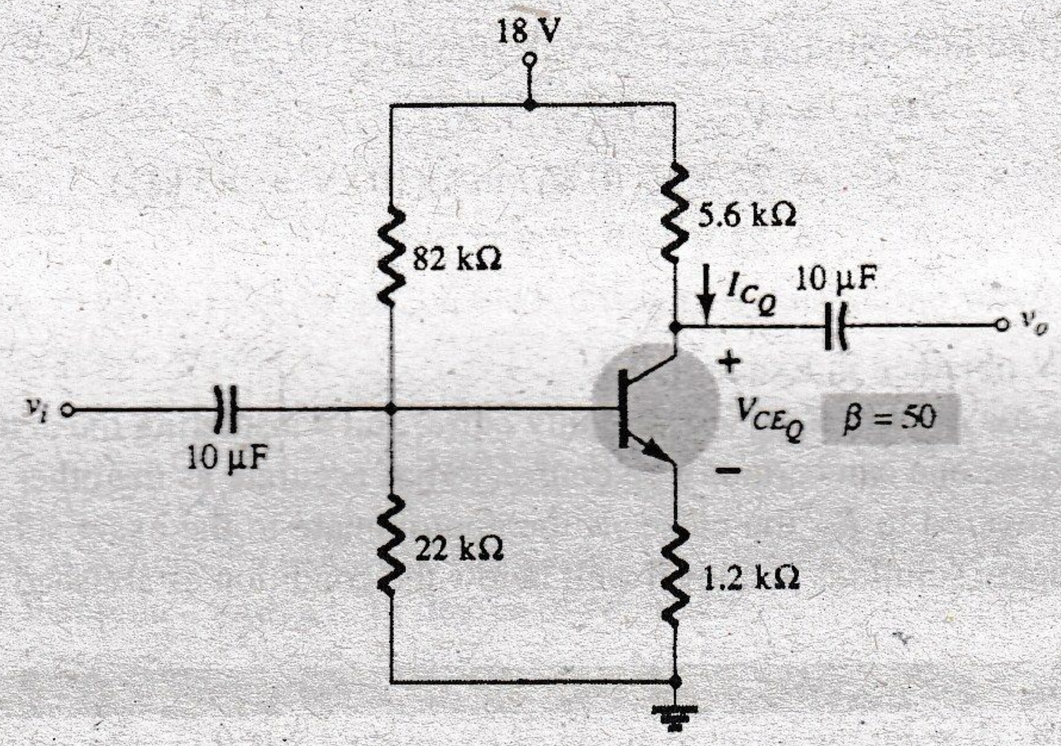


FIG. 4.37
Voltage-divider configuration for Example 4.11.

Solution: Exact analysis:

Eq. (4.33):

$$\beta R_E \geq 10R_2$$

$$(50)(1.2\,\text{k}\Omega) \geq 10(22\,\text{k}\Omega)$$

$$60\,\text{k}\Omega \not\geq 220\,\text{k}\Omega \text{ (not satisfied)}$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\,\text{k}\Omega \| 22\,\text{k}\Omega = 17.35\,\text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,\text{k}\Omega(18\,\text{V})}{82\,\text{k}\Omega + 22\,\text{k}\Omega} = 3.81\,\text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\,\text{V} - 0.7\,\text{V}}{17.35\,\text{k}\Omega + (51)(1.2\,\text{k}\Omega)} = \frac{3.11\,\text{V}}{78.55\,\text{k}\Omega} = 39.6\,\mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu\text{A}) = \mathbf{1.98\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\,\text{V} - (1.98\,\text{mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$

$$= \mathbf{4.54\,V}$$

Approximate analysis:

$$V_B = E_{\text{Th}} = 3.81\,\text{V}$$

$$V_E = V_B - V_{BE} = 3.81\,\text{V} - 0.7\,\text{V} = 3.11\,\text{V}$$

$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\,\text{V}}{1.2\,\text{k}\Omega} = \mathbf{2.59\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\,\text{V} - (2.59\,\text{mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$

$$= \mathbf{3.88\,V}$$

Tabulating the results, we have:

Comparing the exact and approximate approaches.

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, whereas V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.25, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\,V} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0\,mA} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 COLLECTOR FEEDBACK CONFIGURATION

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.38. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop, with the results then applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.39 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

It is important to note that the current through R_C is not I_C, but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B, and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

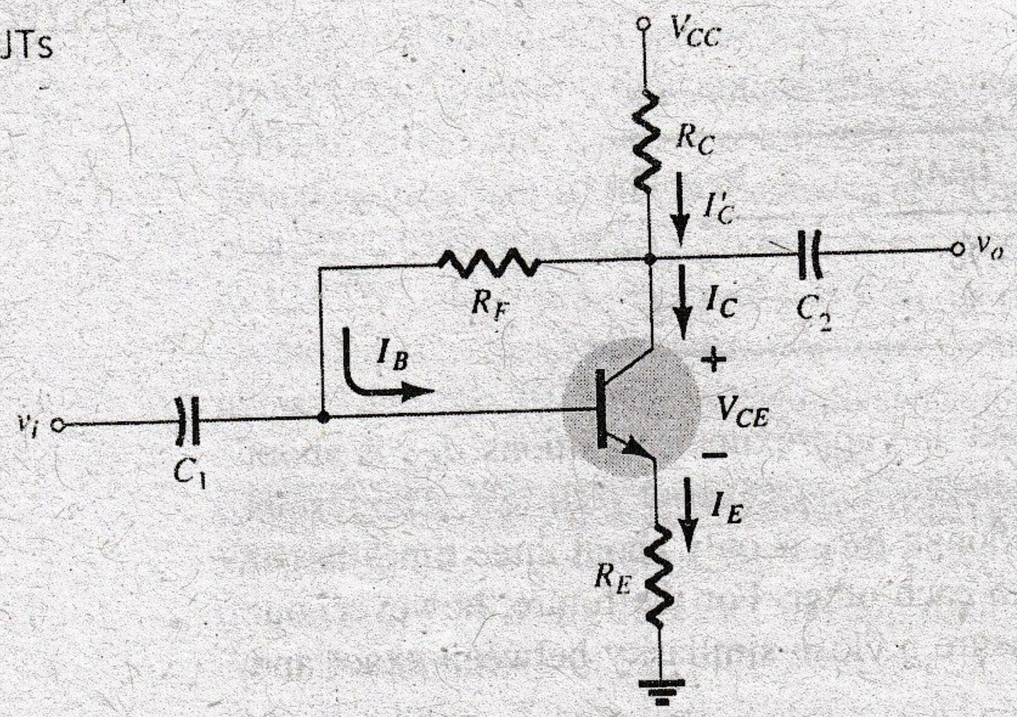


FIG. 4.38
DC bias circuit with voltage feedback.

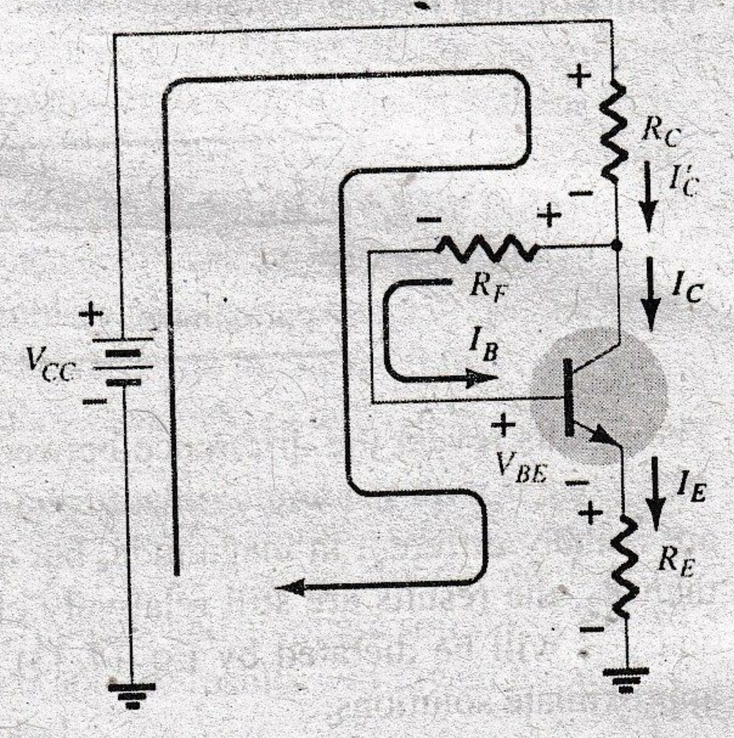


FIG. 4.39
Base–emitter loop for the network of Fig. 4.38.

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} \tag{4.41}$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, whereas the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has the following format, which can be compared with the result for the fixed-bias and emitter-bias configurations.

$$I_B = \frac{V'}{R_F + \beta R'}$$

For the fixed-bias configuration $\beta R'$ does not exist. For the emitter-bias setup (with $\beta + 1 \cong \beta$), $R' = R_E$.

Because $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'}$$

In general, the larger R' is compared with $\frac{R_F}{\beta}$, the more accurate the approximation that

$$I_{C_Q} \cong \frac{V'}{R'}$$

The result is an equation absent of β, which would be very stable for variations in β. Because R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is 0 Ω for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

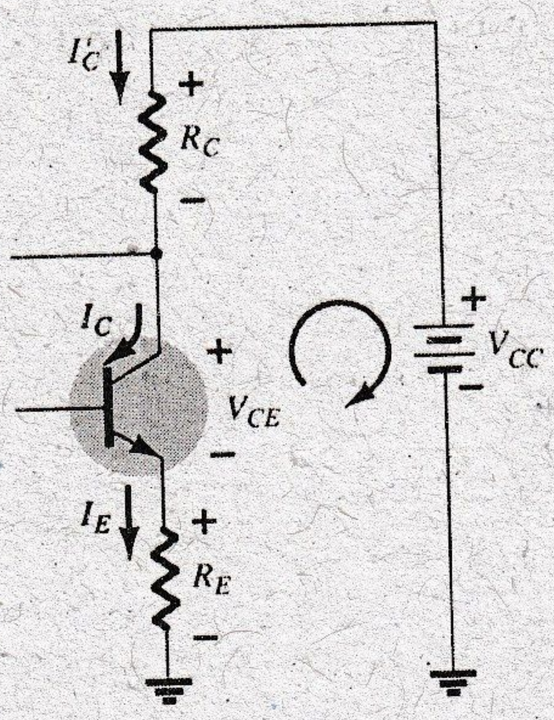


FIG. 4.40
Collector–emitter loop for the network of Fig. 4.38.

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 4.38 is provided in Fig. 4.40. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in

$$I_E R_E + V_{CE} + I_C' R_C - V_{CC} = 0$$

Because $I_C' \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.42}$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

EXAMPLE 4.12 Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.41.

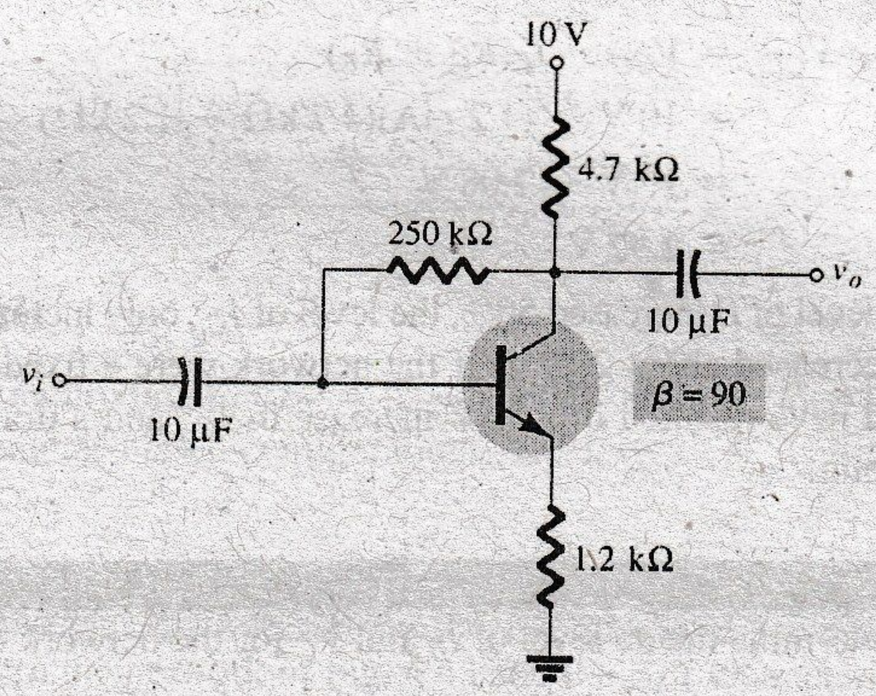


FIG. 4.41
Network for Example 4.12.

Solution: Eq. (4.41):

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\text{ V}}$$

EXAMPLE 4.13 Repeat Example 4.12 using a beta of 135 (50% greater than in Example 4.12).

Solution: It is important to note in the solution for I_B in Example 4.12 that the second term in the denominator of the equation is much larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less is the sensitivity to changes in beta. In this example, the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

1.15 ZENER DIODES

The Zener region of Fig. 1.45 was discussed in some detail in Section 1.6. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive-V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode. The slight slope to the curve in the Zener region reveals that there is a level of resistance to be associated with the Zener diode in the conduction mode.

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in Fig. 1.46a. The semiconductor diode and the Zener diode are presented side by side in Fig. 1.46 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol, as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element as shown in Fig. 1.46c.

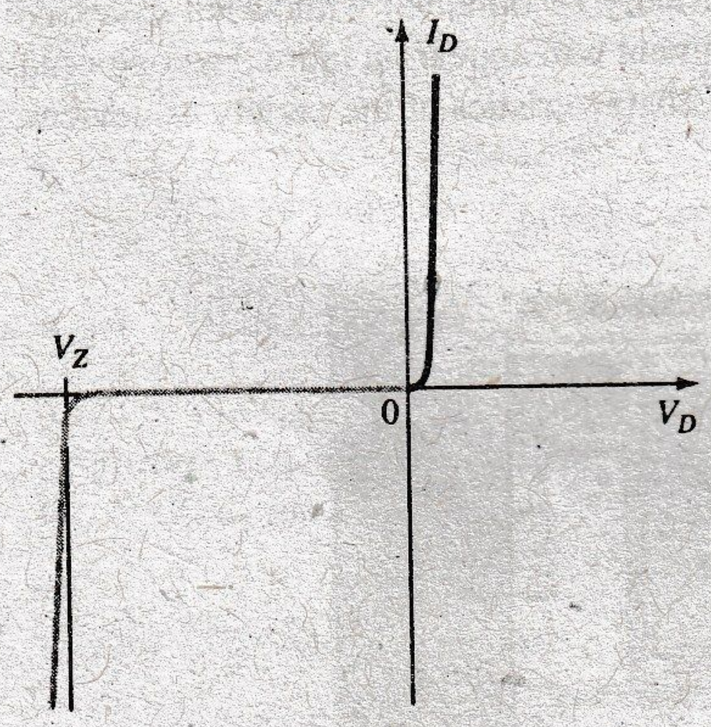


FIG. 1.45
Reviewing the Zener region.

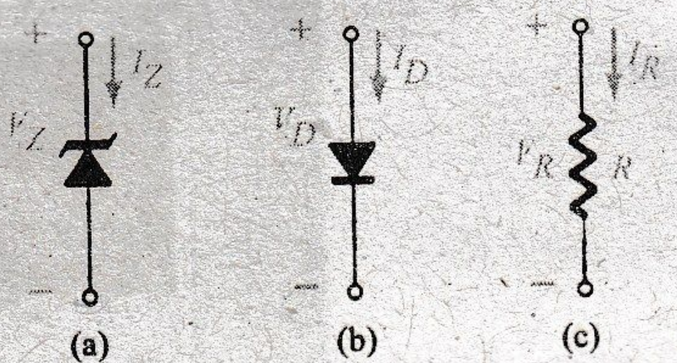


FIG. 1.46
Conduction direction: (a) Zener diode; (b) semiconductor diode; (c) resistive element.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping that produces an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 V to 200 V with power ratings from ¼ W to 50 W. Because of its excellent temperature and current capabilities, silicon is the preferred material in the manufacture of Zener diodes.

It would be nice to assume the Zener diode is ideal with a straight vertical line at the Zener potential. However, there is a slight slope to the characteristics requiring the piecewise equivalent model appearing in Fig. 1.47 for that region. For most of the applications appearing in this text the series resistive element can be ignored and the reduced equivalent model of just a dc battery of V_Z volts employed. Since some applications of Zener diodes swing between the Zener region and the forward-bias region, it is important to understand the operation of the Zener diode in all regions. As shown in Fig. 1.47, the equivalent model for a Zener diode in the reverse-bias region below V_Z is a very large resistor (as for the standard diode). For most applications this resistance is so large it can be ignored and the open-circuit equivalent employed. For the forward-bias region the piecewise equivalent is the same as described in earlier sections.

The specification sheet for a 10-V, 500-mW, 20% Zener diode is provided as Table 1.8, and a plot of the important parameters is given in Fig. 1.48. The term *nominal* used in the specification of the Zener voltage simply indicates that it is a typical average value. Since this is a 20% diode, the Zener potential of the unit one picks out of a *lot* (a term used to describe a package of diodes) can be expected to vary as 10 V + 20%, or from 8 V to 12 V. Both 10% and 50% diodes are also readily available. The test current I_{ZT} is the current defined by the

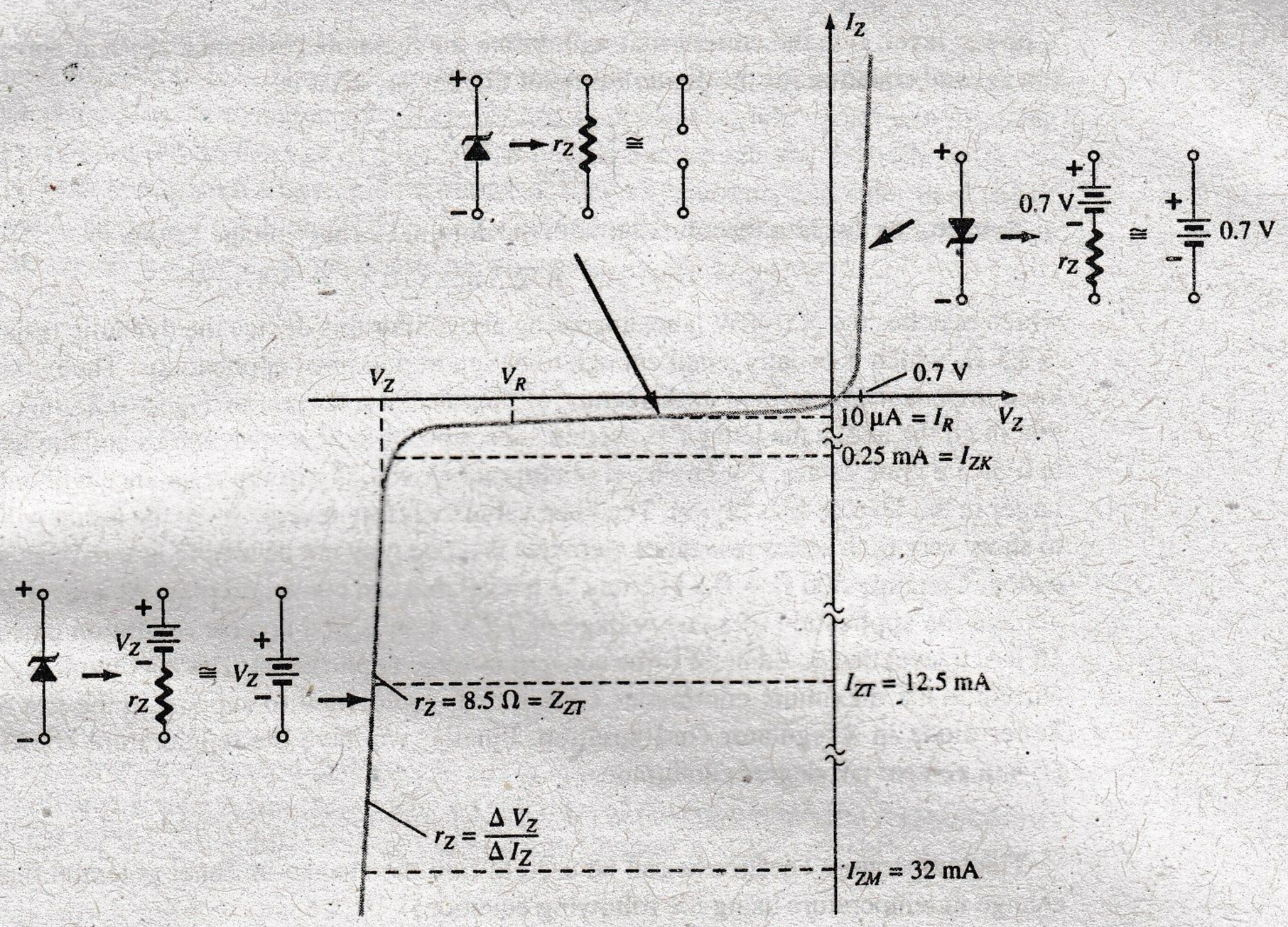
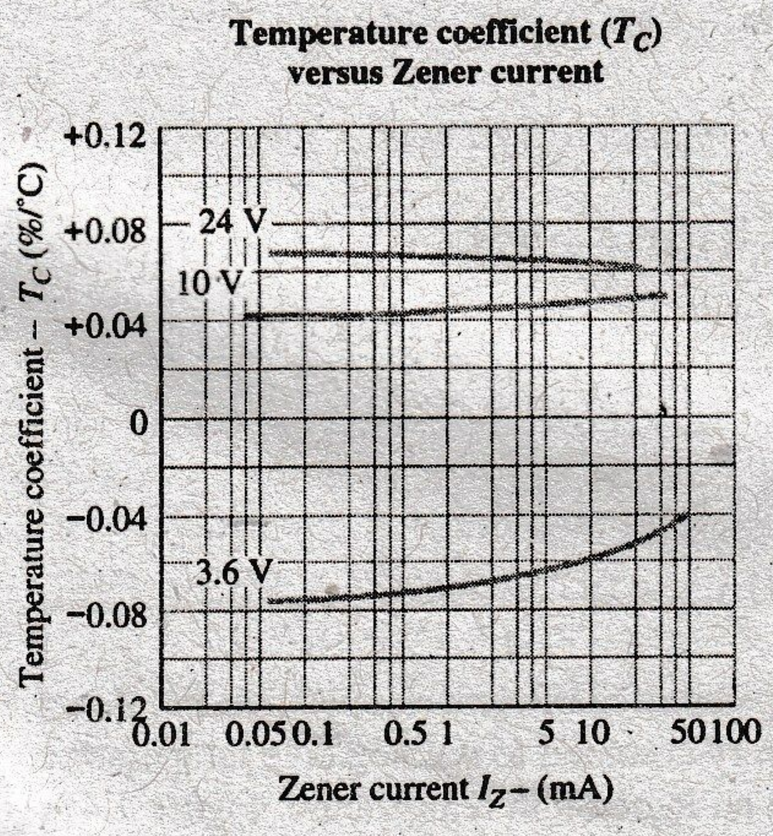


FIG. 1.47
Zener diode characteristics with the equivalent model for each region.

TABLE 1.8
Electrical Characteristics (25°C Ambient Temperature)

Zener Voltage Nominal V_Z (V)	Test Current I_{ZT} (mA)	Maximum Dynamic Impedance Z_{ZT} at I_{ZT} (Ω)	Maximum Knee Impedance Z_{ZK} at I_{ZK} (Ω)	(mA)	Maximum Reverse Current I_R at V_R (μA)	Test Voltage V_R (V)	Maximum Regulator Current I_{ZM} (mA)	Typical Temperature Coefficient (%/°C)
10	12.5	8.5	700	0.25	10	7.2	32	+0.072



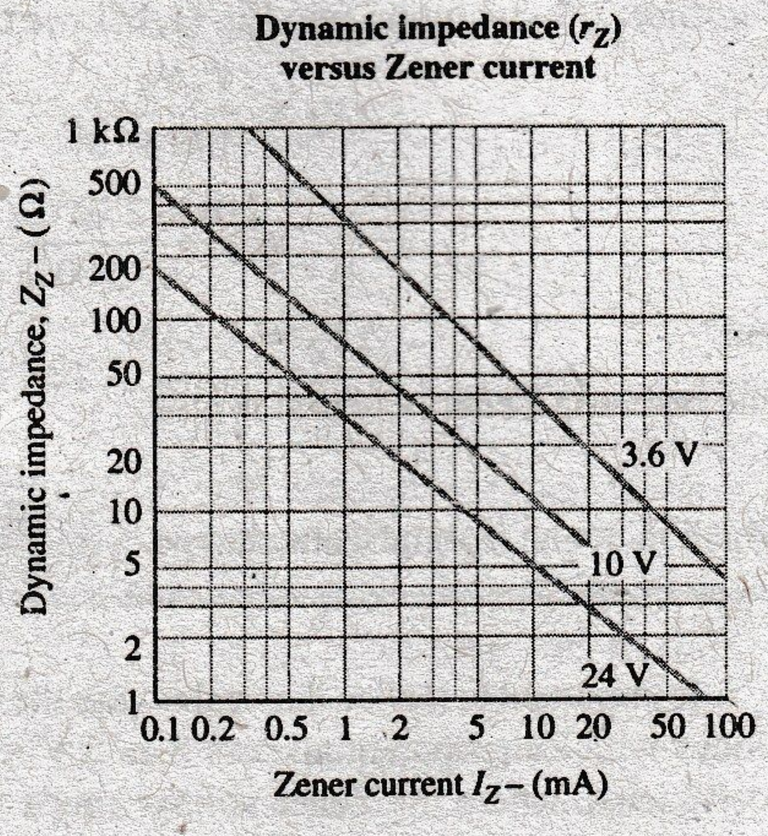


FIG. 1.48
Electrical characteristics for a 10-V, 500-mW Zener diode.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (135)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 796.5\text{ k}\Omega} = \frac{9.3\text{ V}}{1046.5\text{ k}\Omega}$$
$$= 8.89\ \mu\text{A}$$

and
$$I_{C_Q} = \beta I_B$$
$$= (135)(8.89\ \mu\text{A})$$
$$= \mathbf{1.2\text{ mA}}$$

and
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.2\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 10\text{ V} - 7.08\text{ V}$$
$$= \mathbf{2.92\text{ V}}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1%, whereas the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q-point.

EXAMPLE 4.14 Determine the dc level of I_B and V_C for the network of Fig. 4.42.

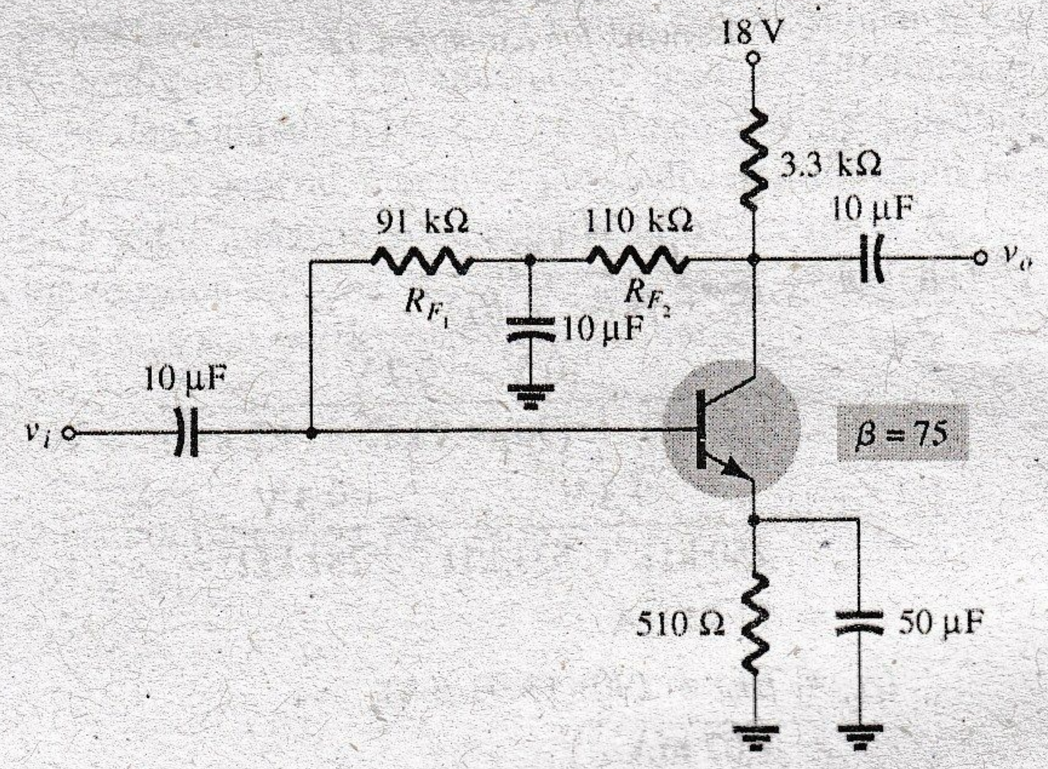


FIG. 4.42
Network for Example 4.14.

Solution: In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and $R_B = R_{F_1} + R_{F_2}$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\text{ k}\Omega + 110\text{ k}\Omega) + (75)(3.3\text{ k}\Omega + 0.51\text{ k}\Omega)}$$
$$= \frac{17.3\text{ V}}{201\text{ k}\Omega + 285.75\text{ k}\Omega} = \frac{17.3\text{ V}}{486.75\text{ k}\Omega}$$
$$= \mathbf{35.5\ \mu\text{A}}$$

$$I_C = \beta I_B$$
$$= (75)(35.5\ \mu A)$$
$$= 2.66\ mA$$
$$V_C = V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C$$
$$= 18\ V - (2.66\ mA)(3.3\ k\Omega)$$
$$= 18\ V - 8.78\ V$$
$$= \mathbf{9.22\ V}$$

Saturation Conditions

Using the approximation $I'_C = I_C$, we find that the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ results in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} is defined by the chosen bias configuration.

EXAMPLE 4.15 Given the network of Fig. 4.43 and the BJT characteristics of Fig. 4.44.

a. Draw the load line for the network on the characteristics.
b. Determine the dc beta in the center region of the characteristics. Define the chosen point as the Q-point.
c. Using the dc beta calculated in part b, find the dc value of I_B.
d. Find I_{C_Q} and I_{CE_Q}.

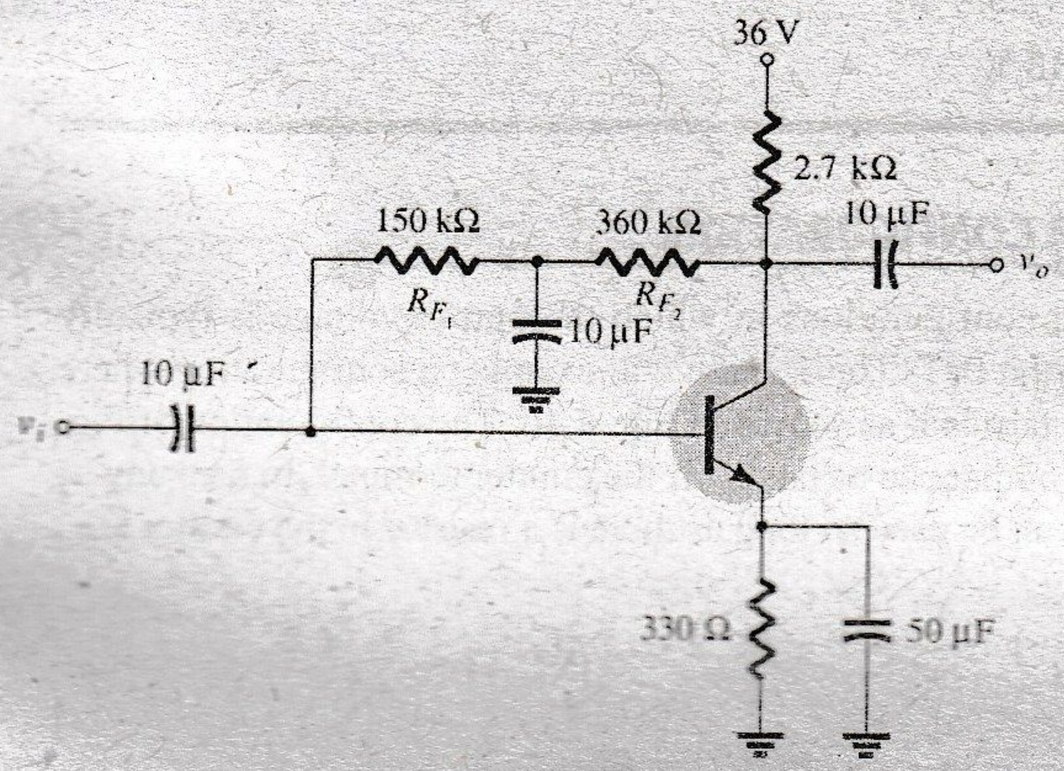


FIG. 4.43
Network for Example 4.15.

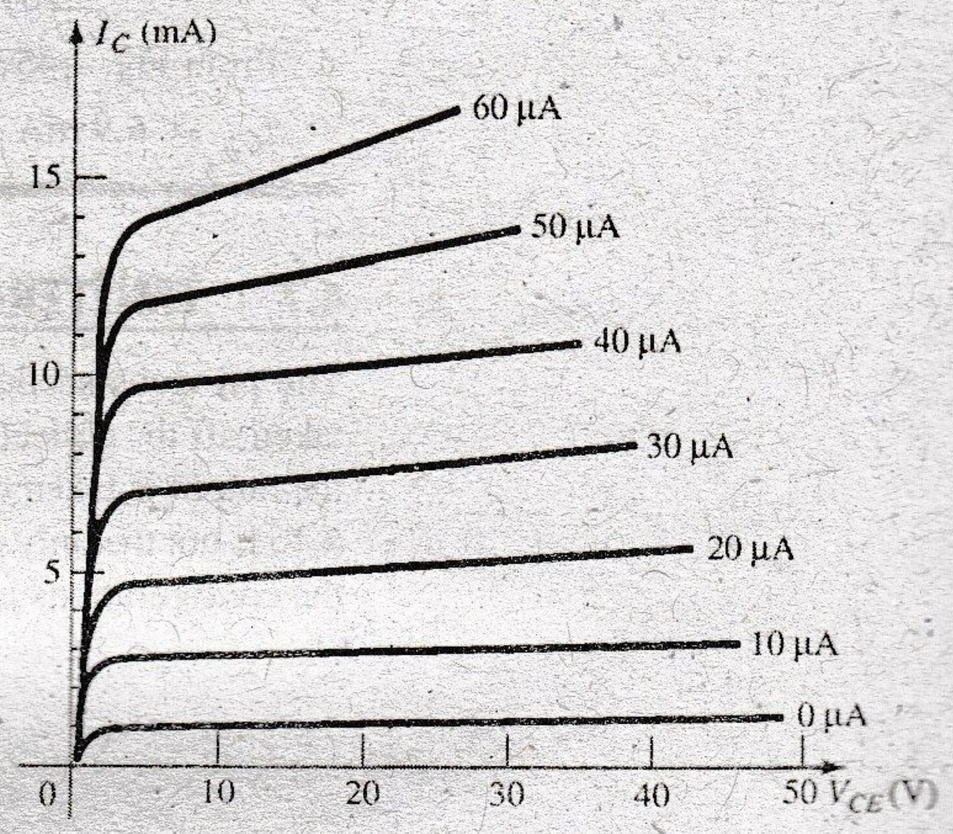


FIG. 4.44
BJT characteristics.

Solution:

a. The load line is drawn on Fig. 4.45 as determined by the following intersections:

$$V_{CE} = 0\ V: I_C = \frac{V_{CC}}{R_C + R_E} = \frac{36\ V}{2.7\ k\Omega + 330\ \Omega} = \mathbf{11.88\ mA}$$

$$I_C = 0\ mA: V_{CE} = V_{CC} = \mathbf{36\ V}$$

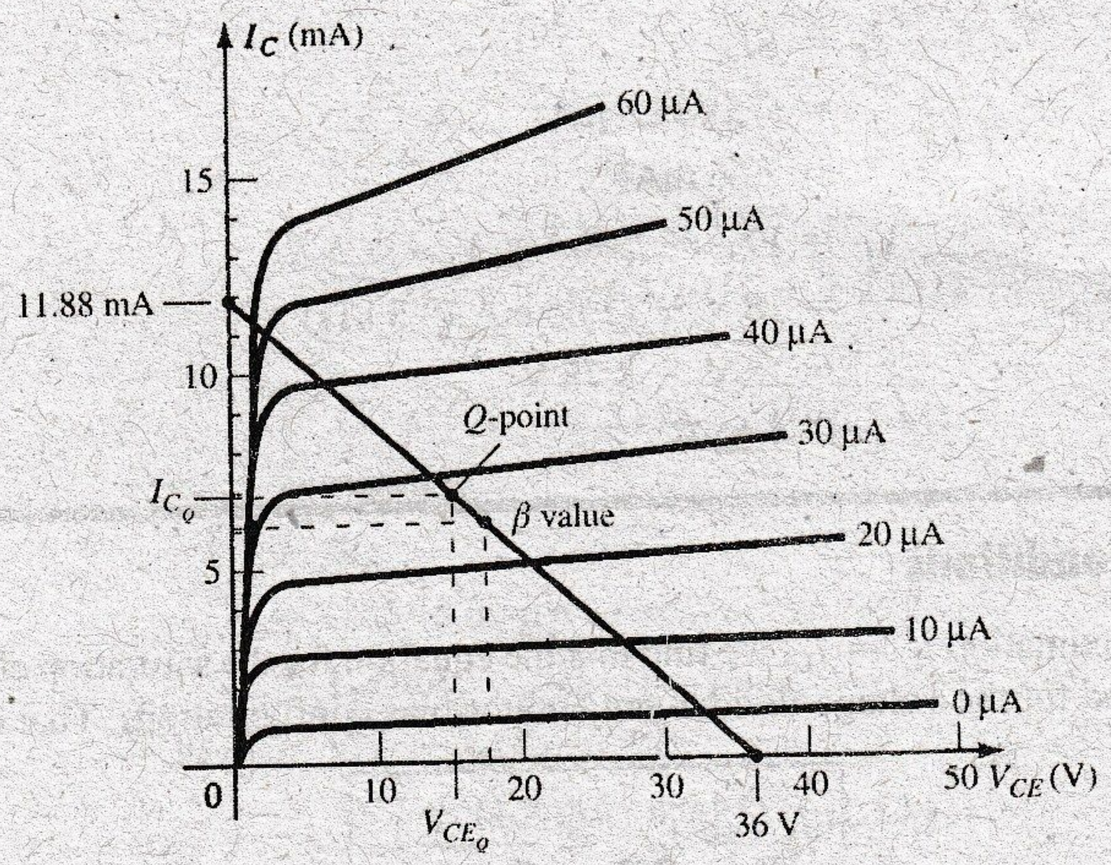


FIG. 4.45
Defining the Q-point for the voltage-divider bias configuration of Fig. 4.43.

b. The dc beta was determined using $I_B = 25\ \mu A$ and V_{CE} about 17 V.

$$\beta \cong \frac{I_{C_Q}}{I_{B_Q}} = \frac{6.2\ \text{mA}}{25\ \mu\text{A}} = \mathbf{248}$$

c. Using Eq. 4.41:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{36\ \text{V} - 0.7\ \text{V}}{510\ \text{k}\Omega + 248(2.7\ \text{k}\Omega + 330\ \Omega)}$$

$$= \frac{35.3\ \text{V}}{510\ \text{k}\Omega + 751.44\ \text{k}\Omega}$$

$$\text{and } I_B = \frac{35.3\ \text{V}}{1.261\ \text{M}\Omega} = \mathbf{28\ \mu A}$$

d. From Fig. 4.45 the quiescent values are

$$I_{C_Q} \cong \mathbf{6.9\ mA} \text{ and } V_{CE_Q} \cong \mathbf{15\ V}$$

4.7 EMITTER-FOLLOWER CONFIGURATION

The previous sections introduced configurations in which the output voltage is typically taken off the collector terminal of the BJT. This section will examine a configuration where the output is taken off the emitter terminal as shown in Fig. 4.46. The configuration of Fig. 4.46 is not the only one where the output can be taken off the emitter terminal. In fact, any of the configurations just described can be used so long as there is a resistor in the emitter leg.

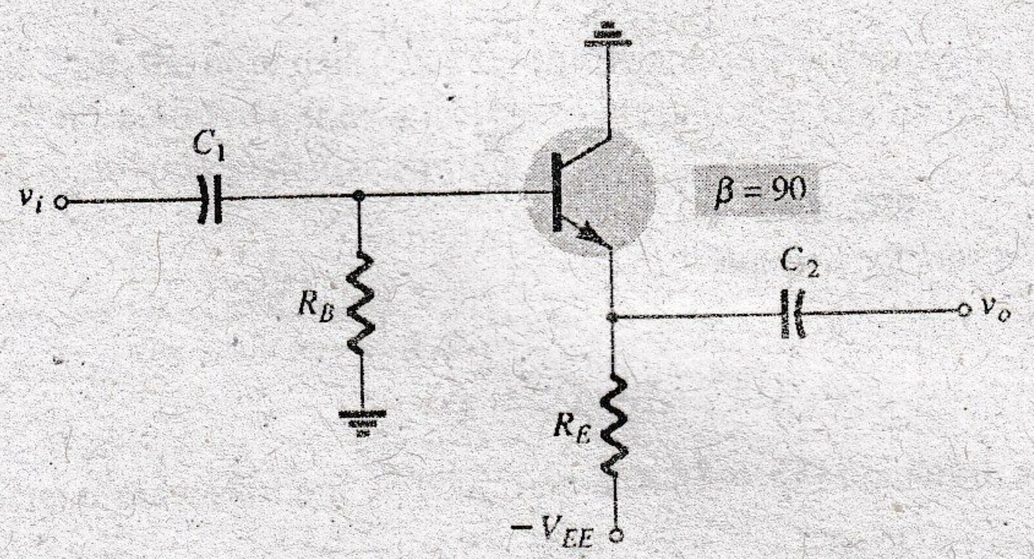


FIG. 4.46
Common-collecter (emitter-follower) configuration.

The dc equivalent of the network of Fig. 4.46 appears in Fig. 4.47

Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

and using $I_E = (\beta + 1)I_B$

$$I_B R_B + (\beta + 1)I_B R_E = V_{EE} - V_{BE}$$

so that

$$\boxed{I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{4.44}$$

For the output network, an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

and

$$\boxed{V_{CE} = V_{EE} - I_E R_E} \tag{4.45}$$

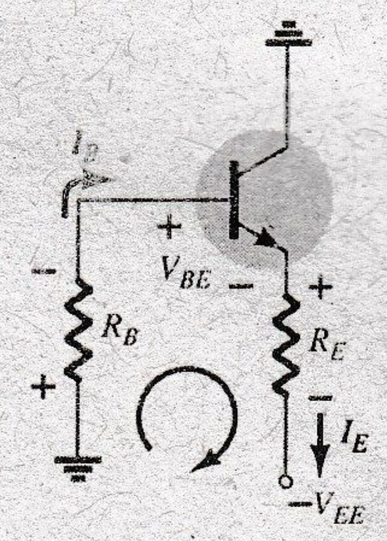


FIG. 4.47
dc equivalent of Fig. 4.46.

EXAMPLE 4.16 Determine V_{CE_Q} and I_{E_Q} for the network of Fig. 4.48.

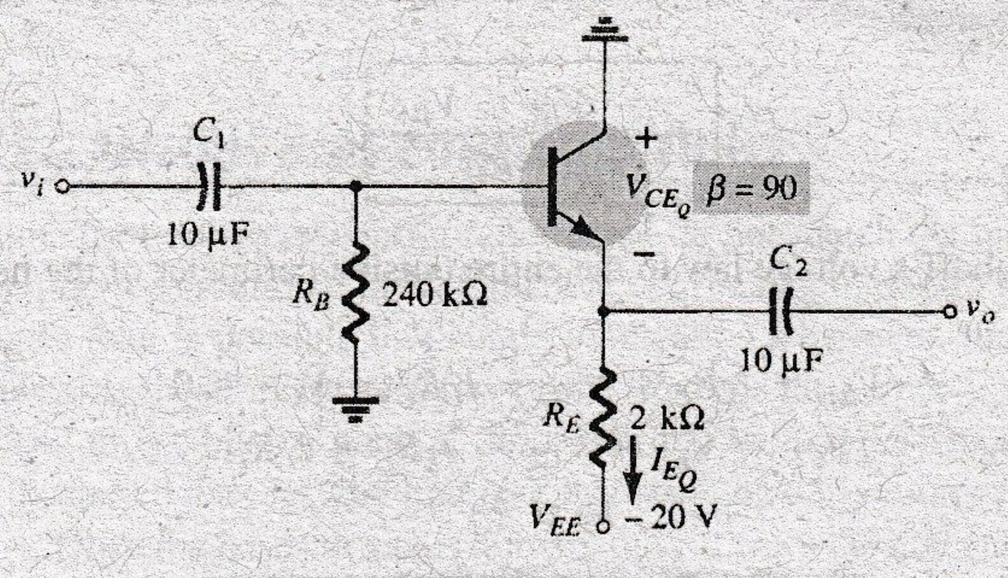


FIG. 4.48
Example 4.16.

Solution:

Eq. 4.44:

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega + (90 + 1)2\text{ k}\Omega} = \frac{19.3\text{ V}}{240\text{ k}\Omega + 182\text{ k}\Omega}$$

$$= \frac{19.3\text{ V}}{422\text{ k}\Omega} = 45.73\ \mu\text{A}$$

and Eq. 4.45:

$$V_{CE_Q} = V_{EE} - I_E R_E$$

$$= V_{EE} - (\beta + 1)I_B R_E$$

$$= 20\text{ V} - (90 + 1)(45.73\ \mu\text{A})(2\text{ k}\Omega)$$

$$= 20\text{ V} - 8.32\text{ V}$$

$$= \mathbf{11.68\text{ V}}$$

$$I_{E_Q} = (\beta + 1)I_B = (91)(45.73\ \mu\text{A})$$

$$= 4.16\text{ mA}$$

4.8 COMMON-BASE CONFIGURATION

The common-base configuration is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential. It is a fairly popular configuration because in the ac domain it has a very low input impedance, high output impedance, and good gain.

A typical common-base configuration appears in Fig. 4.49. Note that two supplies are used in this configuration and the base is the common terminal between the input emitter terminal and output collector terminal.

The dc equivalent of the input side of Fig. 4.49 appears in Fig. 4.50.

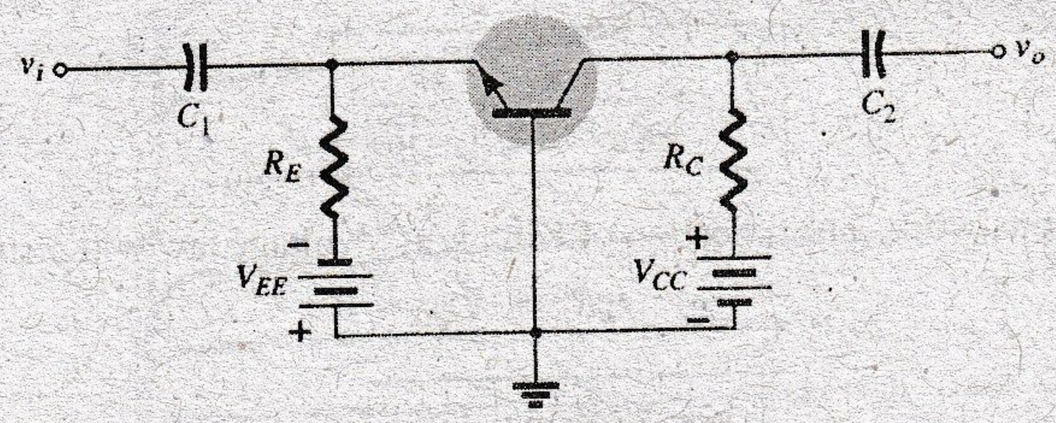


FIG. 4.49
Common-base configuration.

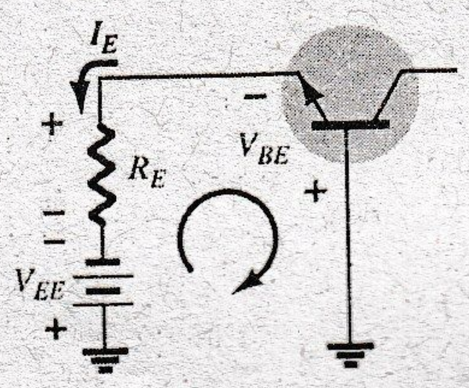


FIG. 4.50
Input dc equivalent of Fig. 4.49.

Applying Kirchhoff's voltage law will result in

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \tag{4.46}$$

Applying Kirchhoff's voltage law to the entire outside perimeter of the network of Fig. 4.51 will result in

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

and solving for V_{CE}:

$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

Because

$$I_E \cong I_C$$

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E) \tag{4.47}$$

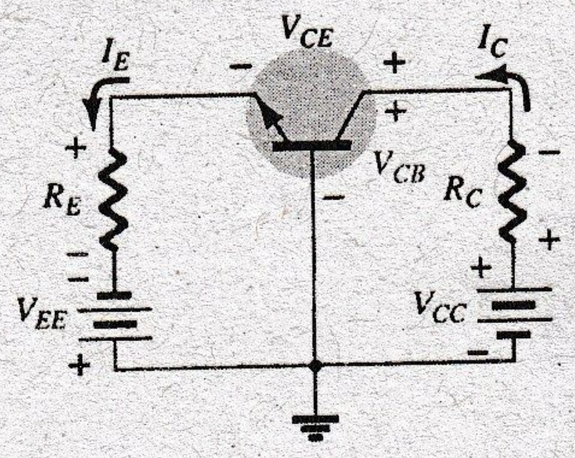


FIG. 4.51
Determining V_{CE} and V_{CB}.

The voltage V_{CB} of Fig. 4.51 can be found by applying Kirchhoff's voltage law to the output loop of Fig 4.51 to obtain:

$$V_{CB} + I_C R_C - V_{CC} = 0$$

or

$$V_{CB} = V_{CC} - I_C R_C$$

Using

$$I_C \cong I_E$$

we have

$$V_{CB} = V_{CC} - I_C R_C \tag{4.48}$$

EXAMPLE 4.17 Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of Fig. 4.52.

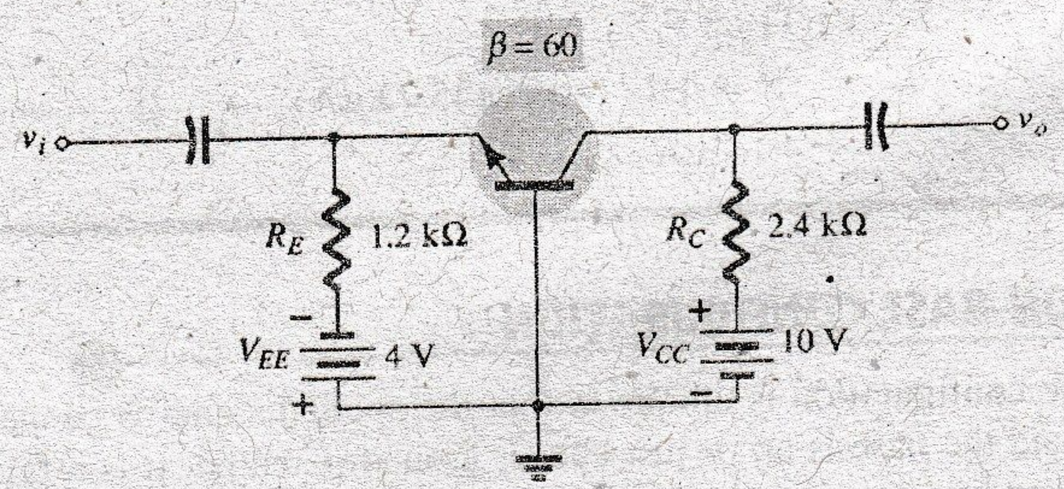


FIG. 4.52
Example 4.17.

Solution: Eq. 4.46:
$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$
$$= \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.75\text{ mA}}$$
$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{ mA}}{60 + 1} = \frac{2.75\text{ mA}}{61}$$
$$= \mathbf{45.08\ \mu A}$$

Eq. 4.47:
$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$
$$= 4\text{ V} + 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 14\text{ V} - (2.75\text{ mA})(3.6\text{ k}\Omega)$$
$$= 14\text{ V} - 9.9\text{ V}$$
$$= \mathbf{4.1\text{ V}}$$

Eq. 4.48:
$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$
$$= 10\text{ V} - (60)(45.08\ \mu\text{A})(24\text{ k}\Omega)$$
$$= 10\text{ V} - 6.49\text{ V}$$
$$= \mathbf{3.51\text{ V}}$$

4.9 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a single publication. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite directly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.38. The analysis is quite similar, but does require dropping R_E from the applied equation.

EXAMPLE 4.18 For the network of Fig. 4.53:

a. Determine I_{C_Q} and V_{CE_Q}.
b. Find V_B, V_C, V_E, and V_{BC}.

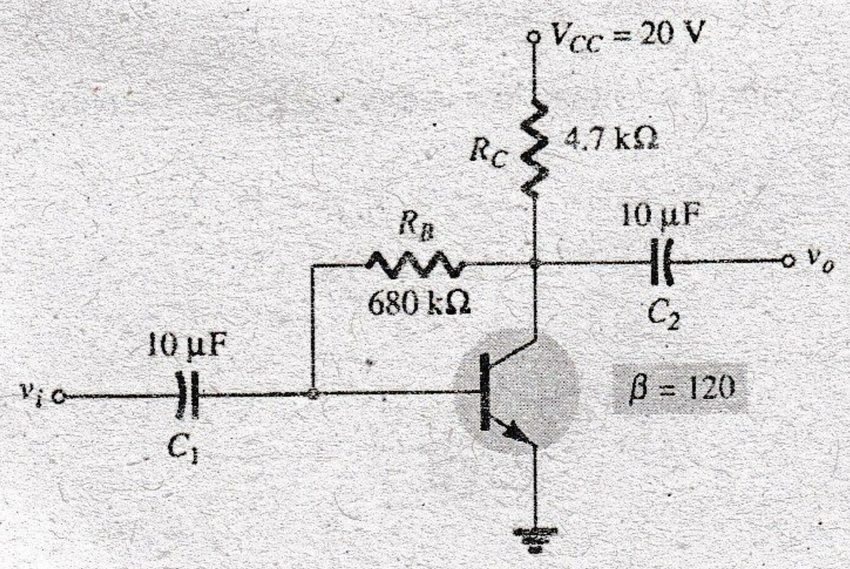


FIG. 4.53
Collector feedback with $R_E = 0\ \Omega$.

Solution:

a. The absence of R_E reduces the reflection of resistive levels to simply that of R_C, and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{680\text{ k}\Omega + (120)(4.7\text{ k}\Omega)} = \frac{19.3\text{ V}}{1.244\text{ M}\Omega}$$

$$= \mathbf{15.51\ \mu A}$$

$$I_{C_Q} = \beta I_B = (120)(15.51\ \mu\text{A})$$

$$= \mathbf{1.86\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (1.86\text{ mA})(4.7\text{ k}\Omega)$$

$$= \mathbf{11.26\text{ V}}$$

b.

$$V_B = V_{BE} = \mathbf{0.7\text{ V}}$$

$$V_C = V_{CE} = \mathbf{11.26\text{ V}}$$

$$V_E = \mathbf{0\text{ V}}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 11.26\text{ V}$$

$$= \mathbf{-10.56\text{ V}}$$

In the next example, the applied voltage is connected to the emitter leg and R_C is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.

EXAMPLE 4.19 Determine V_C and V_B for the network of Fig. 4.54.

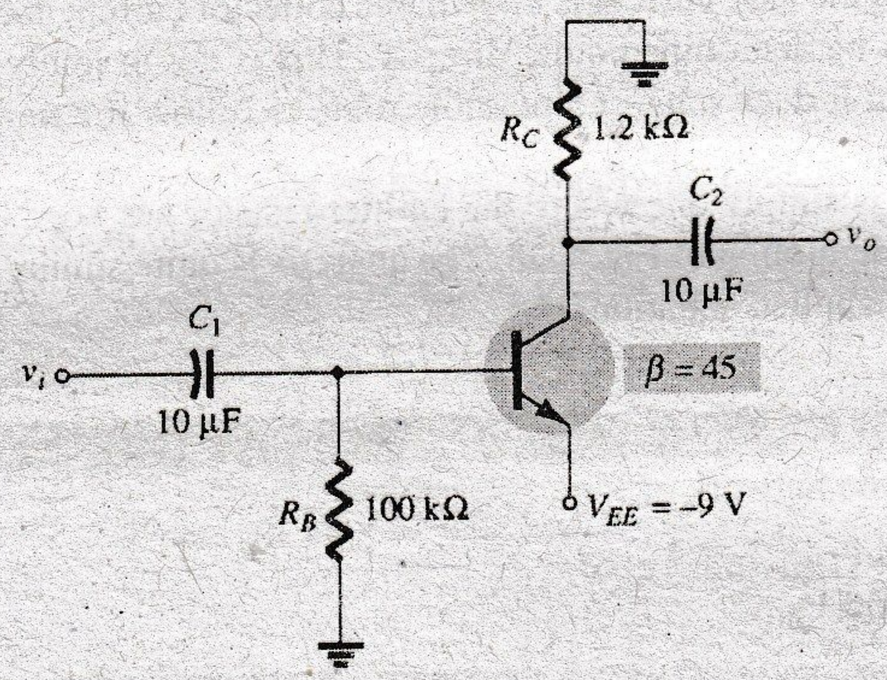


FIG. 4.54
Example 4.19.

Solution: Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}$$

$$= \frac{8.3\text{ V}}{100\text{ k}\Omega}$$

$$= 83\ \mu\text{A}$$

$$I_C = \beta I_B$$
$$= (45)(83\ \mu A)$$
$$= 3.735\ mA$$
$$V_C = -I_C R_C$$
$$= -(3.735\ mA)(1.2\ k\Omega)$$
$$= \mathbf{-4.48\ V}$$
$$V_B = -I_B R_B$$
$$= -(83\ \mu A)(100\ k\Omega)$$
$$= \mathbf{-8.3\ V}$$

Example 4.20 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

EXAMPLE 4.20 Determine V_C and V_B for the network of Fig. 4.55.

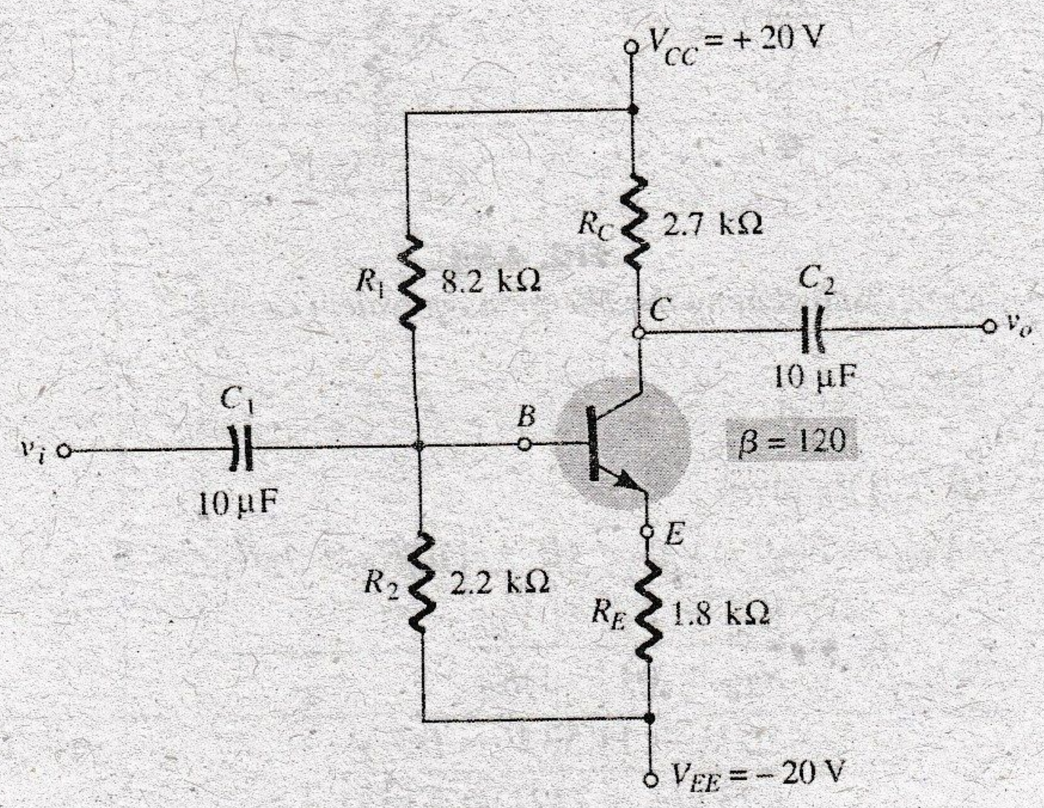


FIG. 4.55
Example 4.20.

Solution: The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.56 and 4.57.

R_{Th}

$$R_{Th} = 8.2\ k\Omega \| 2.2\ k\Omega = 1.73\ k\Omega$$

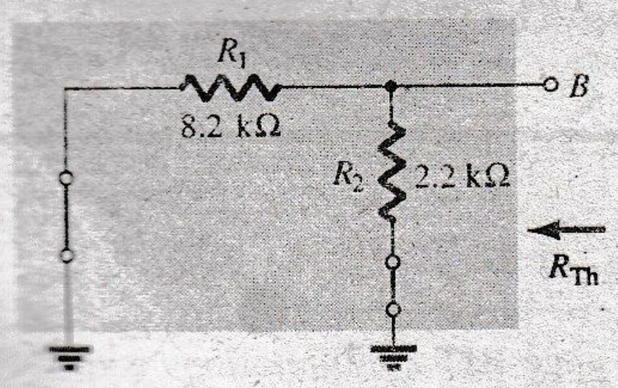


FIG. 4.56
Determining R_{Th}.

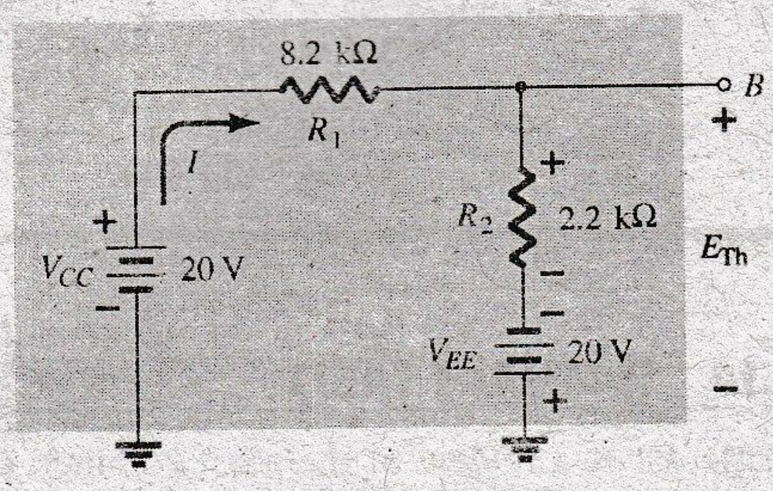


FIG. 4.57
Determining E_{Th}.

E_{Th}

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\text{ V} + 20\text{ V}}{8.2\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{40\text{ V}}{10.4\text{ k}\Omega}$$
$$= 3.85\text{ mA}$$
$$E_{Th} = IR_2 - V_{EE}$$
$$= (3.85\text{ mA})(2.2\text{ k}\Omega) - 20\text{ V}$$
$$= -11.53\text{ V}$$

The network can then be redrawn as shown in Fig. 4.58, where the application of Kirchhoff's voltage law results in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$

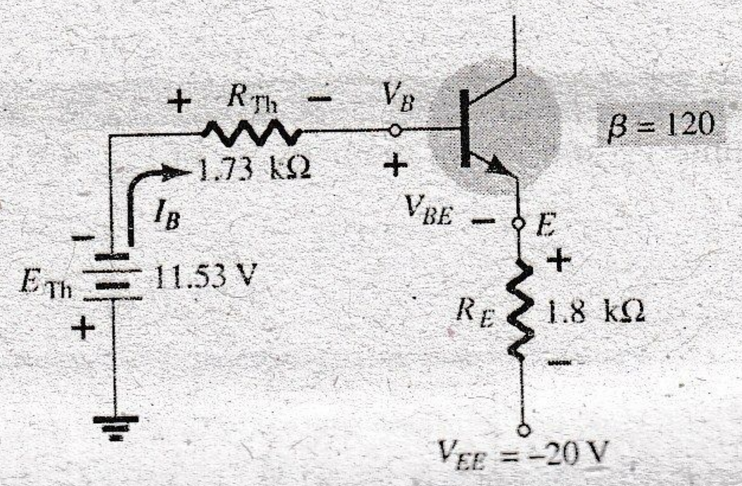


FIG. 4.58
Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

and

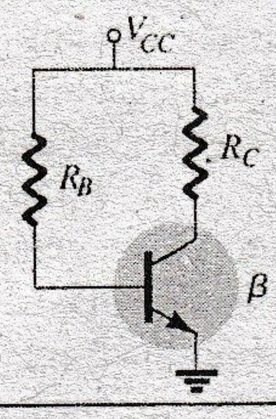
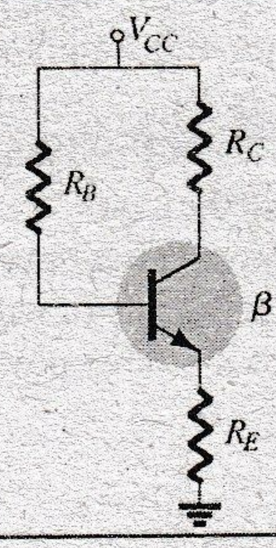
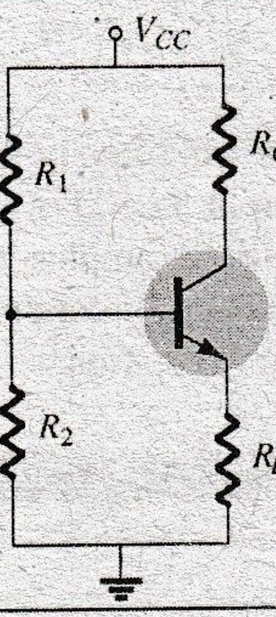
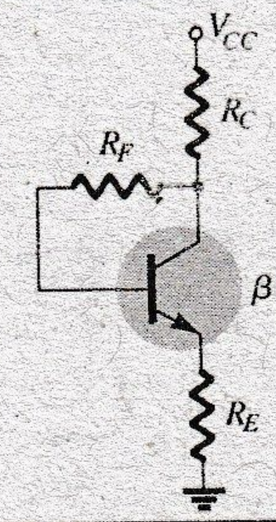
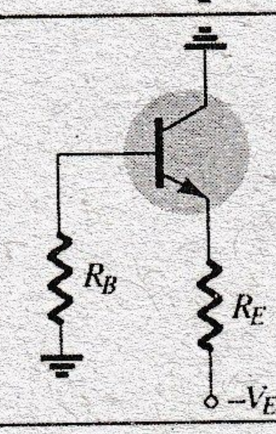
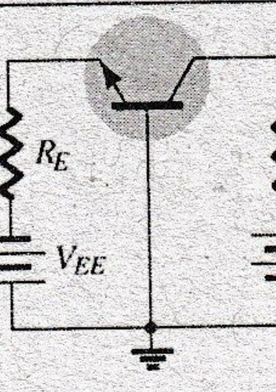
$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{20\text{ V} - 11.53\text{ V} - 0.7\text{ V}}{1.73\text{ k}\Omega + (121)(1.8\text{ k}\Omega)}$$
$$= \frac{7.77\text{ V}}{219.53\text{ k}\Omega}$$
$$= 35.39\ \mu\text{A}$$
$$I_C = \beta I_B$$
$$= (120)(35.39\ \mu\text{A})$$
$$= 4.25\text{ mA}$$
$$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (4.25\text{ mA})(2.7\text{ k}\Omega)$$
$$= \mathbf{8.53\text{ V}}$$
$$V_B = -E_{Th} - I_B R_{Th}$$
$$= -(11.53\text{ V}) - (35.39\ \mu\text{A})(1.73\text{ k}\Omega)$$
$$= \mathbf{-11.59\text{ V}}$$

4.10 SUMMARY TABLE

Table 4.1 is a review of the most common single-stage BJT configurations with their respective equations. Note the similarities that exist between the equations for the various configurations.

TABLE 4.1

BJT Bias Configurations

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Voltage-divider bias		EXACT: $R_{Th} = R_1 \| R_2, E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Collector-feedback		$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Emitter-follower		$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
Common-base		$I_E = \frac{V_{EE} - V_{BE}}{R_E}$ $I_B = \frac{I_E}{\beta + 1}, I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$

4.11 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \tag{4.49}$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.49) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from the design specifications. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b.

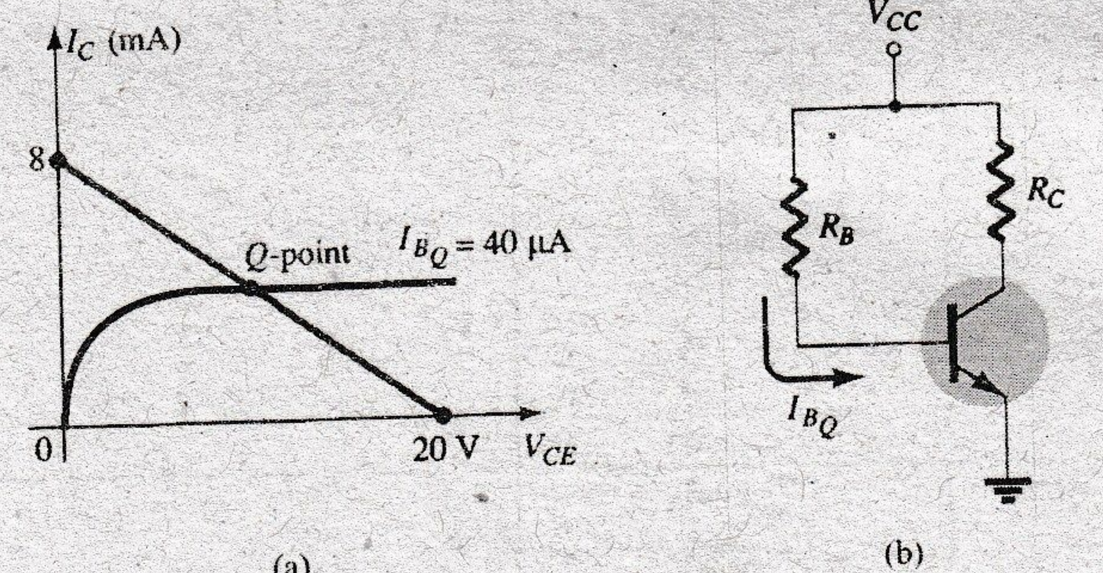


FIG. 4.59
Example 4.21.

Solution: From the load line

$$V_{CC} = 20\ \text{V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ \text{V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = 2.5\ \text{k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{40\ \mu\text{A}} = \frac{19.3\text{ V}}{40\ \mu\text{A}}$$
$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values are
$$R_C = 2.4\text{ k}\Omega$$
$$R_B = 470\text{ k}\Omega$$

Using standard resistor values gives
$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

EXAMPLE 4.22 Given that $I_{C_Q} = 2\text{ mA}$ and $V_{CE_Q} = 10\text{ V}$, determine R_1 and R_C for the network of Fig. 4.60.

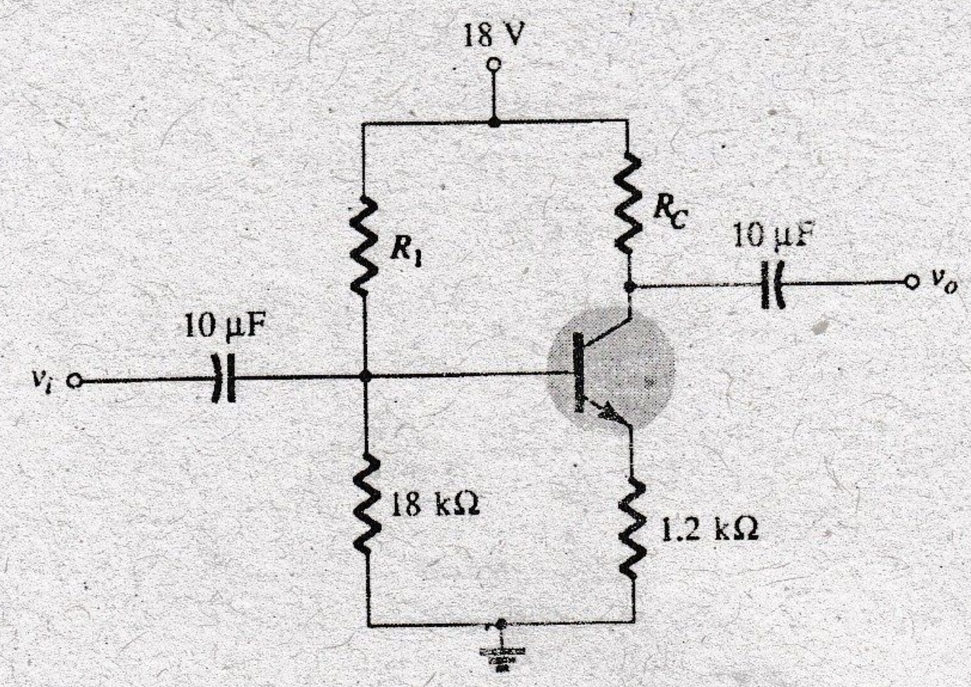


FIG. 4.60
Example 4.22.

Solution:
$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\text{ mA})(1.2\text{ k}\Omega) = 2.4\text{ V}$$
$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\text{ V}$$

and
$$\frac{(18\text{ k}\Omega)(18\text{ V})}{R_1 + 18\text{ k}\Omega} = 3.1\text{ V}$$
$$324\text{ k}\Omega = 3.1R_1 + 55.8\text{ k}\Omega$$
$$3.1R_1 = 268.2\text{ k}\Omega$$
$$R_1 = \frac{268.2\text{ k}\Omega}{3.1} = \mathbf{86.52\ k\Omega}$$

Eq. (4.49): $R_C = \dfrac{V_{R_C}}{I_C} = \dfrac{V_{CC} - V_C}{I_C}$

with
$$V_C = V_{CE} + V_E = 10\text{ V} + 2.4\text{ V} = 12.4\text{ V}$$

and
$$R_C = \frac{18\text{ V} - 12.4\text{ V}}{2\text{ mA}}$$
$$= \mathbf{2.8\ k\Omega}$$

The nearest standard commercial values to R_1 are 82 kΩ and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 4.7 kΩ = 86.7 kΩ would result in a value very close to the design level.

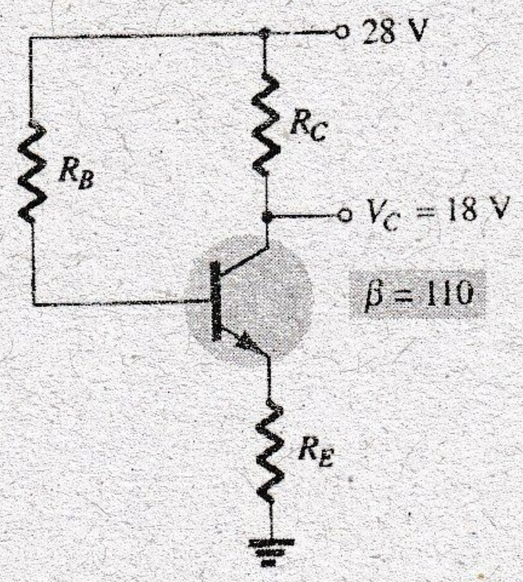


FIG. 4.61
Example 4.23.

EXAMPLE 4.23 The emitter-bias configuration of Fig. 4.61 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{sat}$, $I_{C_{sat}} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C, R_E, and R_B.

Solution:

$$I_{C_Q} = \tfrac{1}{2}I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = \mathbf{2.5\ k\Omega}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

and

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= \mathbf{1\ k\Omega}$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36\ \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36\ \mu\text{A}} - 111 \text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

For standard values,

$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we concentrate on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.62. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector–emitter loop has two unknown quantities present—the resistors R_C and R_E. At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.62 using the criteria just introduced for the emitter voltage.

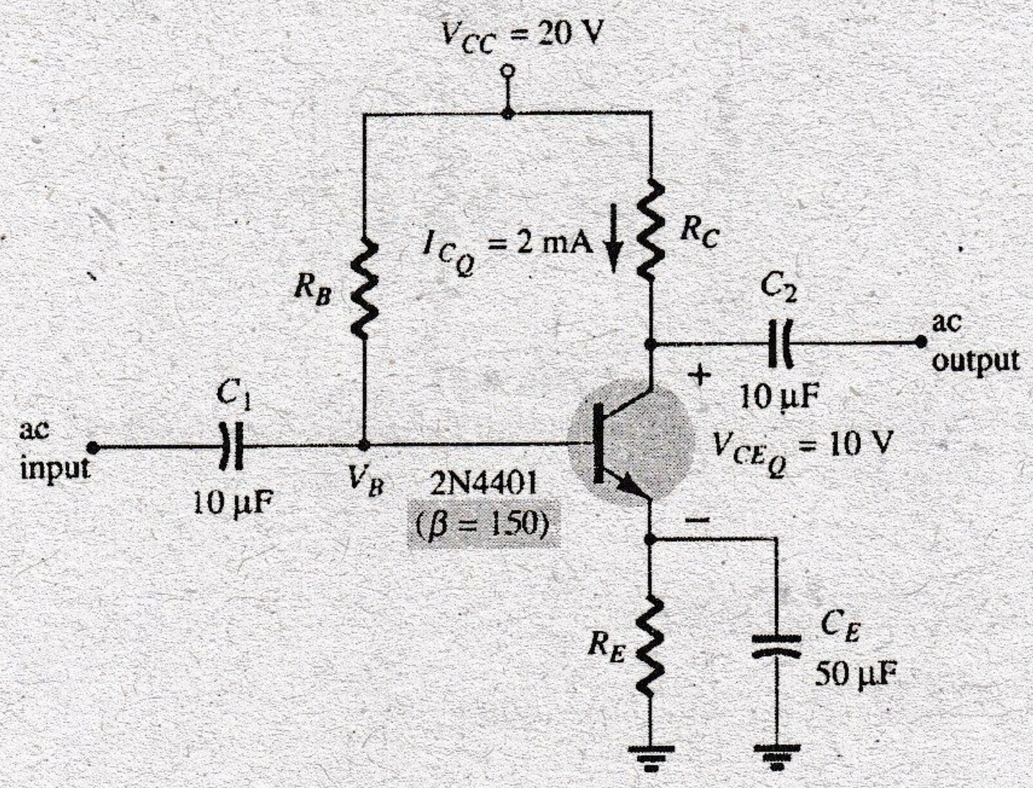


FIG. 4.62
Emitter-stabilized bias circuit for design consideration.

EXAMPLE 4.24 Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\,k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\,k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$

$$\cong \mathbf{1.3\,M\Omega}$$

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.63 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage V_E, as in the previous design consideration, leads to a direct, straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

EXAMPLE 4.25 Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.63 for the operating point indicated.

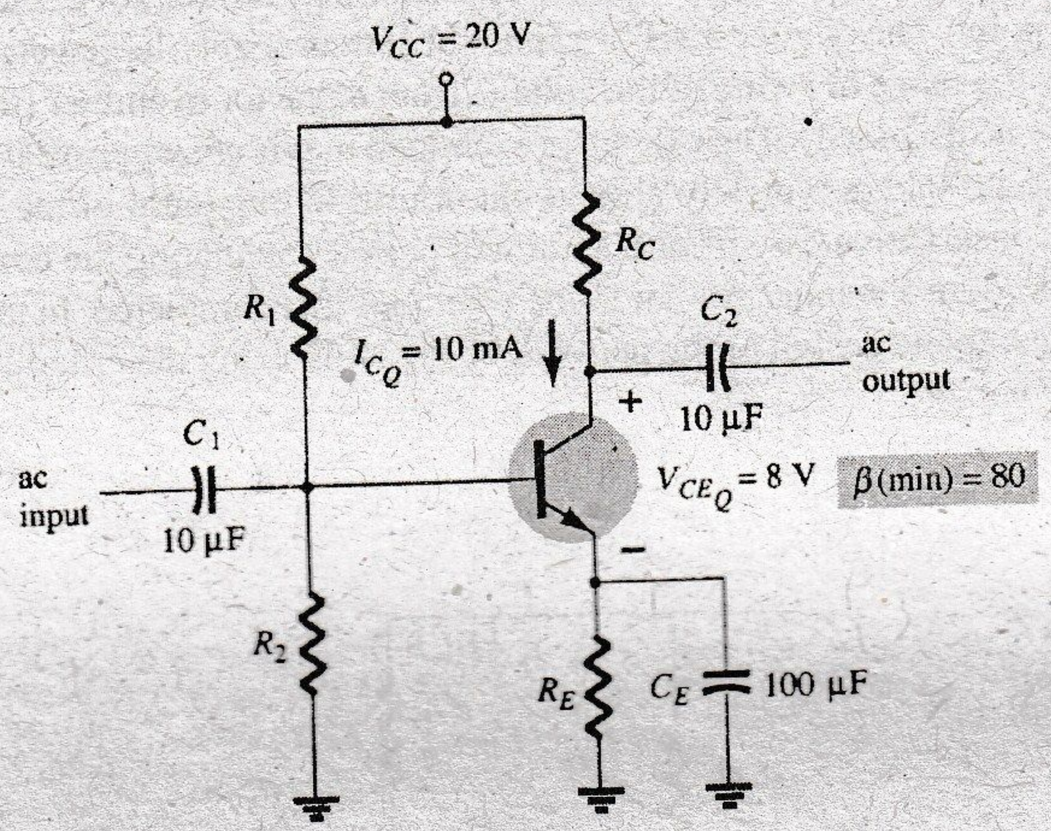


FIG. 4.63
Current-gain-stabilized circuit for design considerations.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

The equations for the calculation of the base resistors R_1 and R_2 will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, R_1 and R_2. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through R_1 and R_2 should be approximately equal to and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

Substitution yields

$$R_2 \leq \tfrac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

and
$$2.7R_1 + 4.32\,\text{k}\Omega = 32\,\text{k}\Omega$$
$$2.7R_1 = 27.68\,\text{k}\Omega$$
$$R_1 = \mathbf{10.25\,k\Omega} \quad (\text{use } 10\,\text{k}\Omega)$$

4.12 MULTIPLE BJT NETWORKS

The BJT networks introduced thus far have only been single-stage configurations. This section will cover some of the most popular networks using multiple transistors. It will demonstrate how the methods introduced thus far in this chapter can be applied to networks with any number of components.

The **R–C coupling** of Fig. 4.64 is probably the most common. The collector output of one stage is fed directly into the base of the next stage using a coupling capacitor C_C. The capacitor is chosen to ensure that it will block dc between the stages and act like a short circuit to any ac signal. The network of Fig. 4.64 has two voltage-divider stages, but the same coupling can be used between any combination of networks such as the fixed-bias or emitter-follower configurations. Substituting an open-circuit equivalent for C_C and the other capacitors of the network will result in the two bias arrangements shown in Fig. 4.65. The methods of analysis introduced in this chapter can then be applied to each stage separately since one stage will not affect the other. Of course, the 20 V dc supply must be applied to each isolated component.

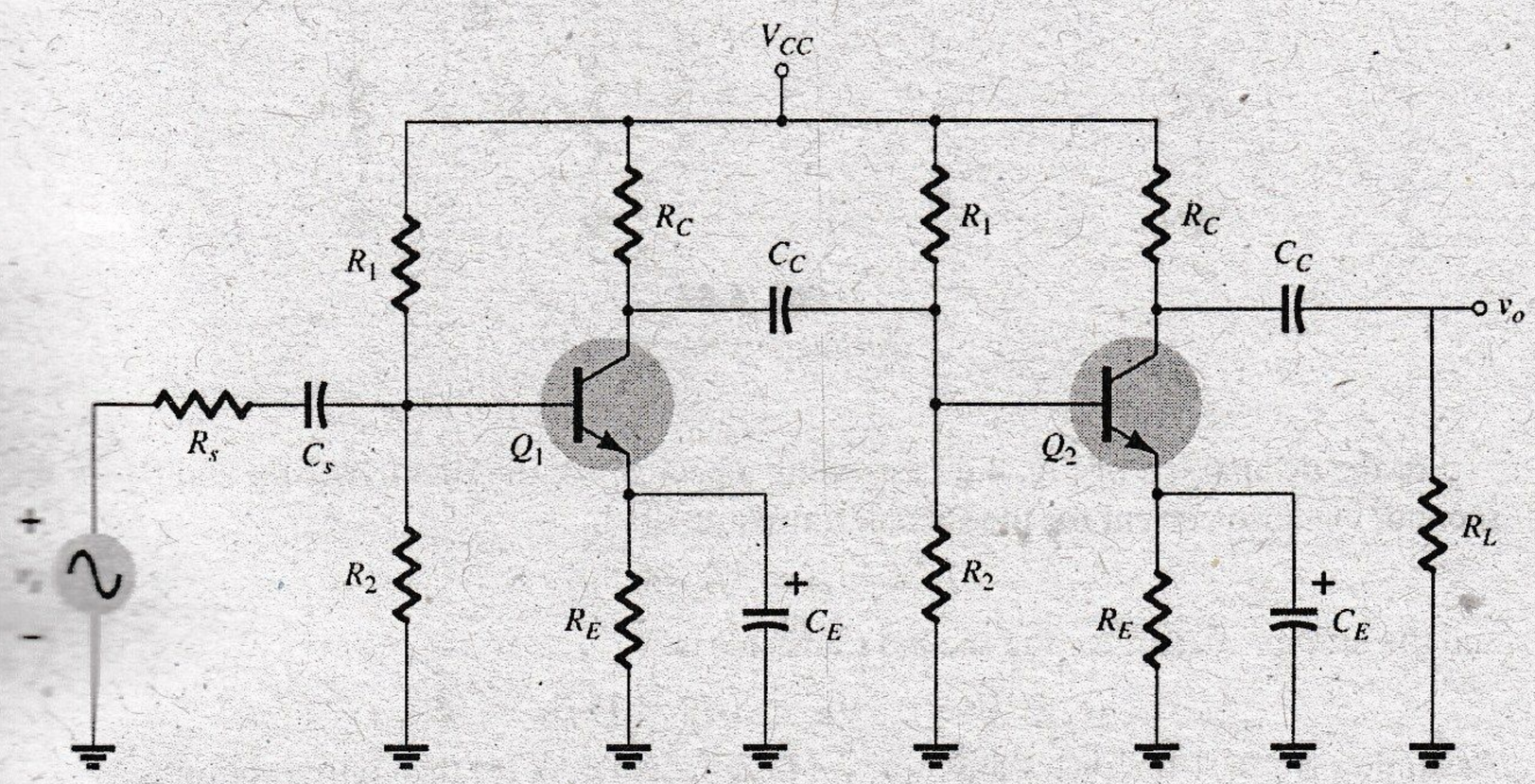


FIG. 4.64
R–C coupled BJT amplifiers.

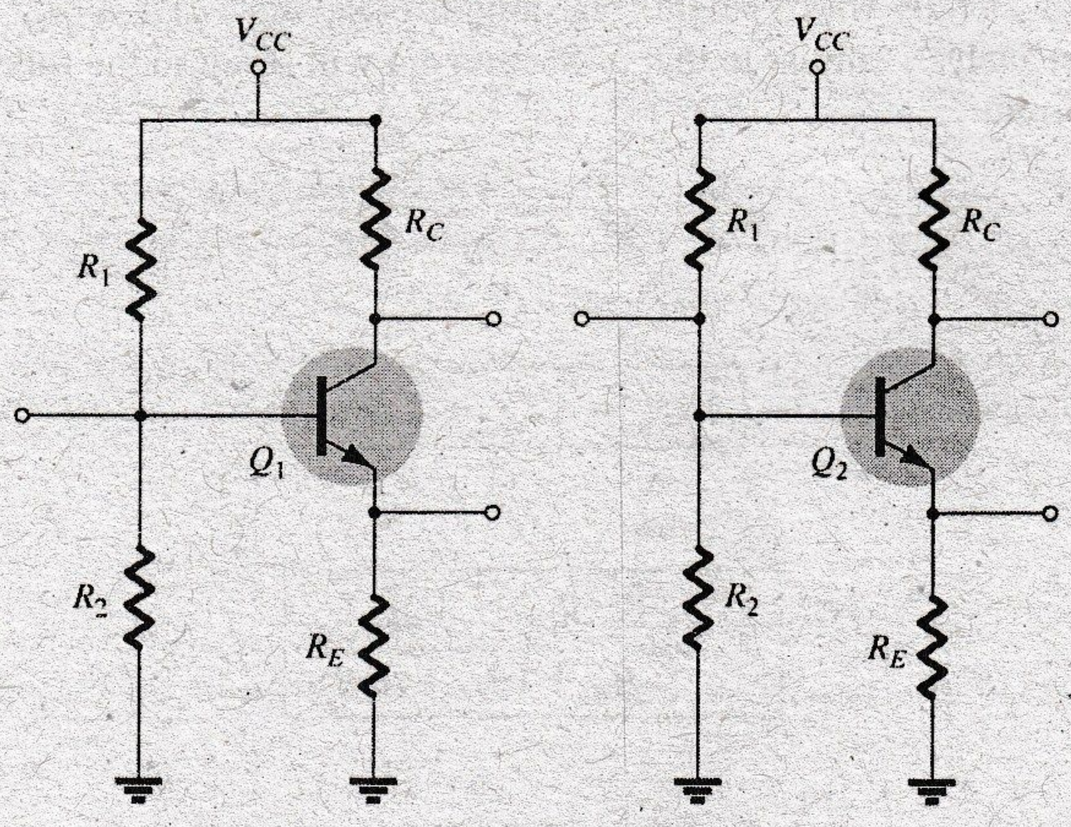


FIG. 4.65
DC equivalent of Fig. 4.64.

The **Darlington** configuration of Fig. 4.66 feeds the output of one stage directly into the input of the succeeding stage. Since the output of Fig. 4.66 is taken directly off the emitter terminal, you will find in the next chapter that the ac gain is very close to 1 but the input impedance is very high, making it attractive for use in amplifiers operating off sources that have a relatively high internal resistance. If a load resistor were added to the collector leg and the output taken off the collector terminal, the configuration would provide a very high gain.

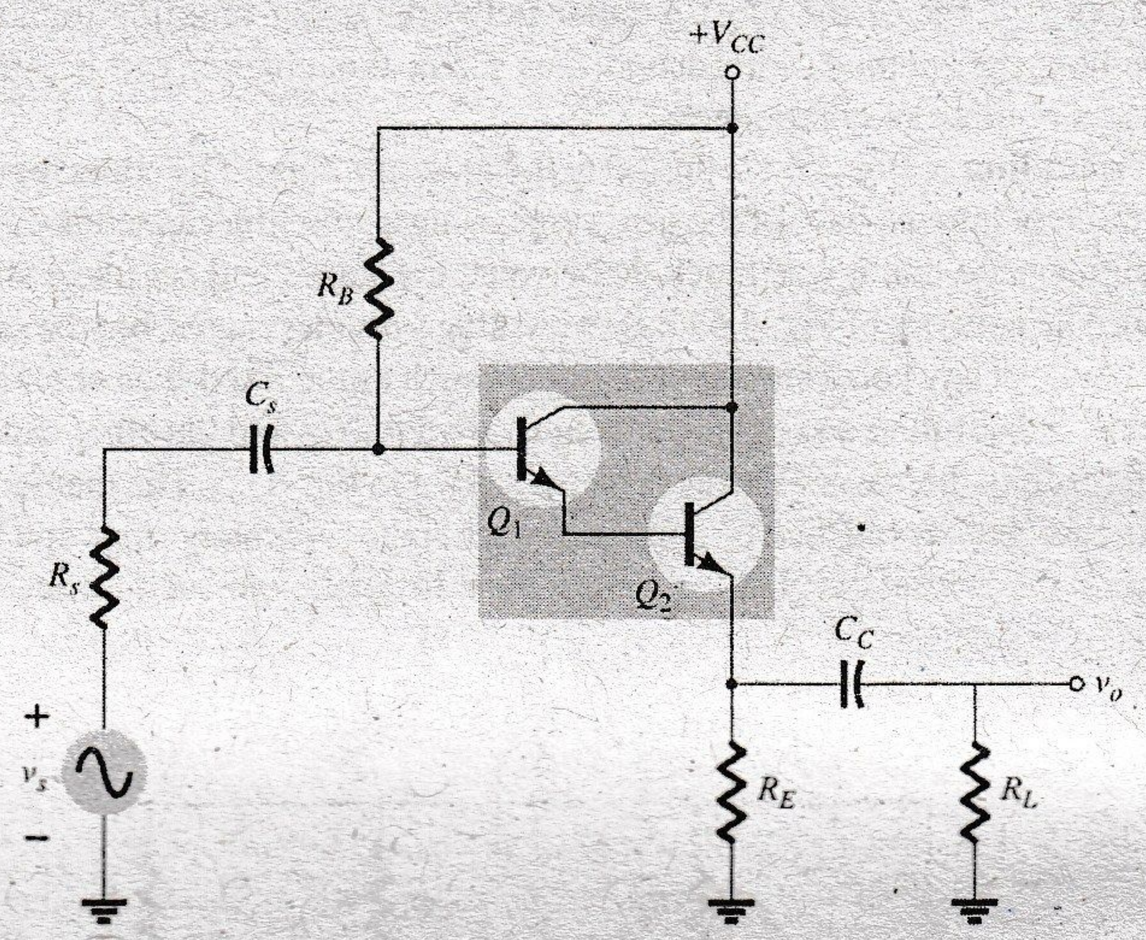


FIG. 4.66
Darlington amplifier.

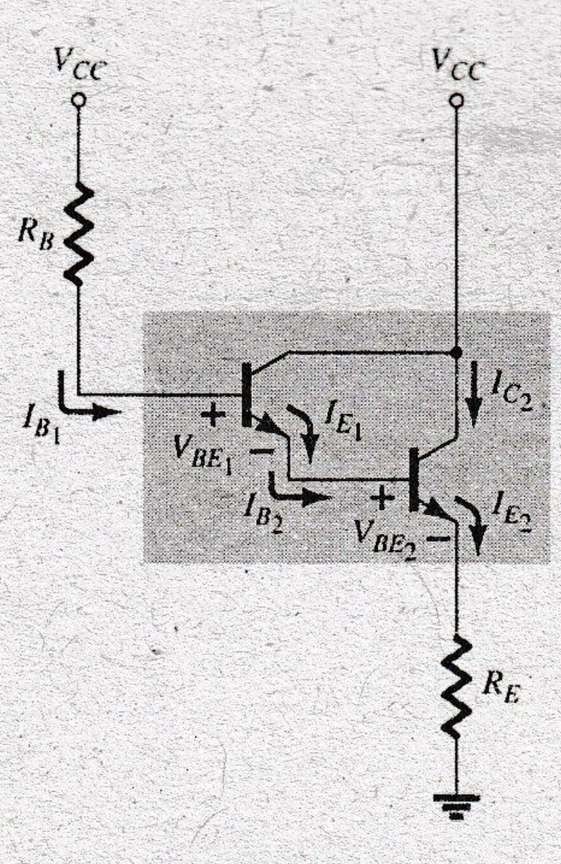


FIG. 4.67
DC equivalent of Fig. 4.66.

For the dc analysis of Fig. 4.67 assuming a beta β_1 for the first transistor and β_2 for the second, the base current for the second transistor is

$$I_{B_2} = I_{E_1} = (\beta_1 + 1)I_{B_1}$$

and the emitter current for the second transistor is

$$I_{E_2} = (\beta_2 + 1)I_{B_2} = (\beta_2 + 1)(\beta_1 + 1)I_{B_1}$$

Assuming $\beta \gg 1$ for each transistor, we find the net beta for the configuration is

$$\boxed{\beta_D = \beta_1\beta_2} \tag{4.50}$$

which compares directly with a single-stage amplifier having a gain of β_D.

Applying an analysis similar to that of Section 4.4 will result in the following equation for the base current:

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

Defining

$$\boxed{V_{BE_D} = V_{BE_1} + V_{BE_2}} \tag{4.51}$$

we have

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E}} \tag{4.52}$$

The currents

$$\boxed{I_{C_2} \cong I_{E_2} = \beta_D I_{B_1}} \tag{4.53}$$

and the dc voltage at the emitter terminal is

$$\boxed{V_{E_2} = I_{E_2}R_E} \tag{4.54}$$

The collector voltage for this configuration is obviously equal to that of the source V.

$$\boxed{V_{C_2} = V_{CC}} \tag{4.55}$$

and the voltage across the output of the transistor is

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

and

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \tag{4.56}$$

The **Cascode** configuration of Fig. 4.68 ties the collector of one transistor to the emitter of the other. In essence it is a voltage-divider network with a common-base configuration at the collector. The result is a network with a high gain and a reduced Miller capacitance—a topic to be examined in Section 9.9.

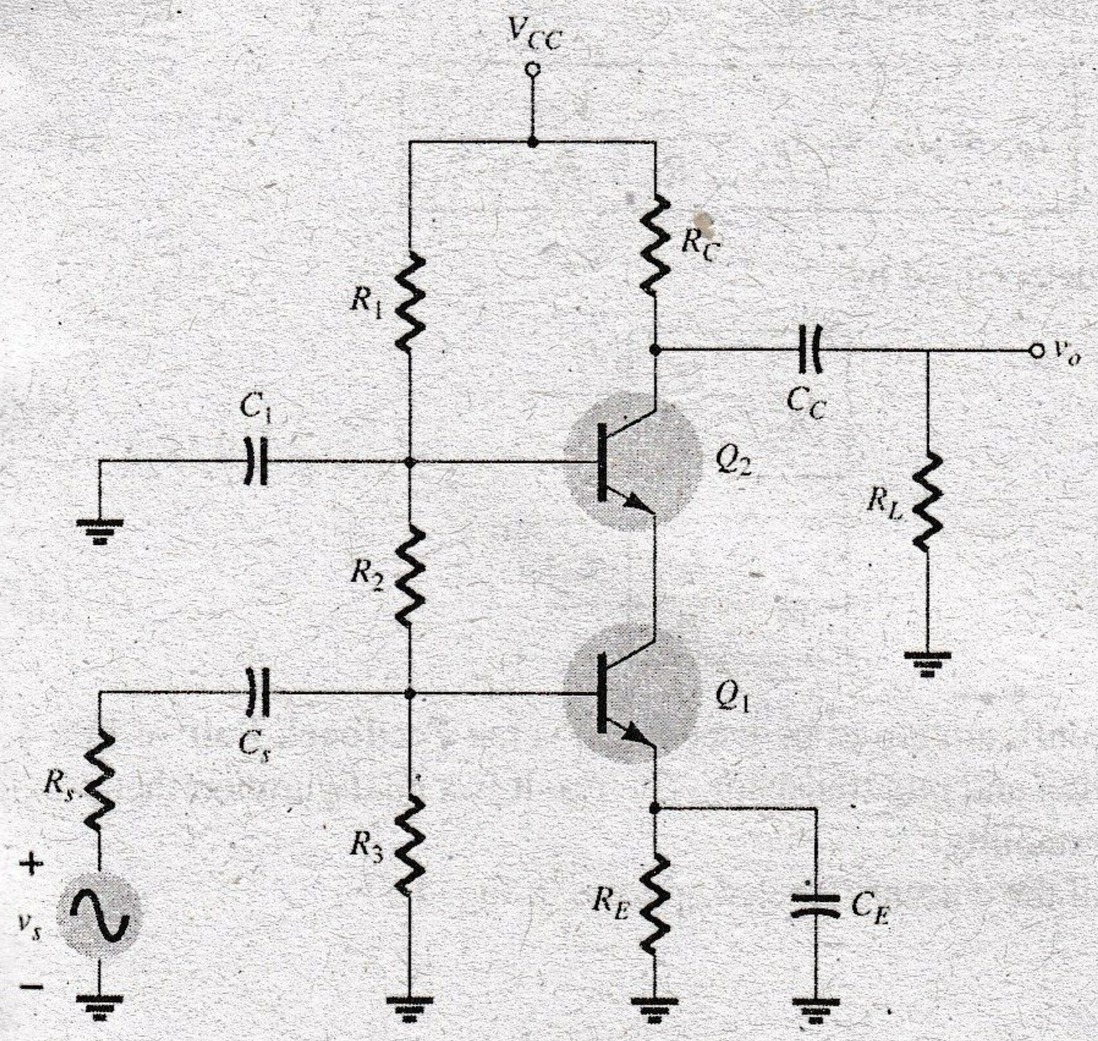


FIG. 4.68
Cascode amplifier.

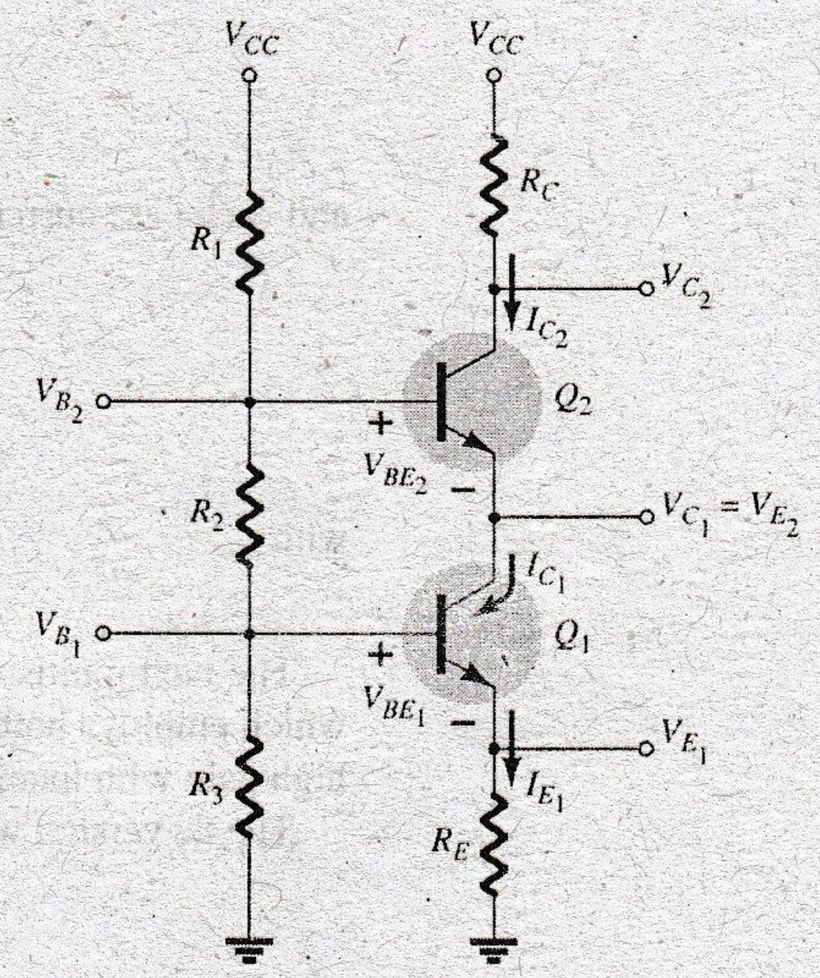


FIG. 4.69
DC equivalent of Fig. 4.68.

The dc analysis is initiated by assuming the current through the bias resistors R_1, R_2, and R_3 of Fig. 4.69 is much larger than the base current of each transistor. That is,

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} \gg I_{B_1} \text{ or } I_{B_2}$$

The result is that the voltage at the base of the transistor Q_1 is simply determined by an application of the voltage-divider rule:

$$\boxed{V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3}V_{CC}} \tag{4.57}$$

The voltage at the base of the transistor Q_2 is found in the same manner:

$$\boxed{V_{B_2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3}V_{CC}} \tag{4.58}$$

The emitter voltages are then determined by

$$V_{E_1} = V_{B_1} - V_{BE_1} \tag{4.59}$$

and

$$V_{E_2} = V_{B_2} - V_{BE_2} \tag{4.60}$$

with the emitter and collector currents determined by:

$$I_{C_2} \cong I_{E_2} \cong I_{C_1} \cong I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_{E_1} + R_{E_2}} \tag{4.61}$$

The collector voltage V_{C_1}:

$$V_{C_1} = V_{B_2} - V_{BE_2} \tag{4.62}$$

and the collector voltage V_{C_2}:

$$V_{C_2} = V_{CC} - I_{C_2}R_C \tag{4.63}$$

The current through the biasing resistors is

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3} \tag{4.64}$$

and each base current is determined by

$$I_{B_1} = \frac{I_{C_1}}{\beta_1} \tag{4.65}$$

with

$$I_{B_2} = \frac{I_{C_2}}{\beta_2} \tag{4.66}$$

The next multistage configuration to be introduced is the **Feedback Pair** of Fig. 4.70, which employs both an *npn* and *pnp* transistor. The result is a configuration that provides high gain with increased stability.

The dc version with all the currents labeled appears in Fig. 4.71.

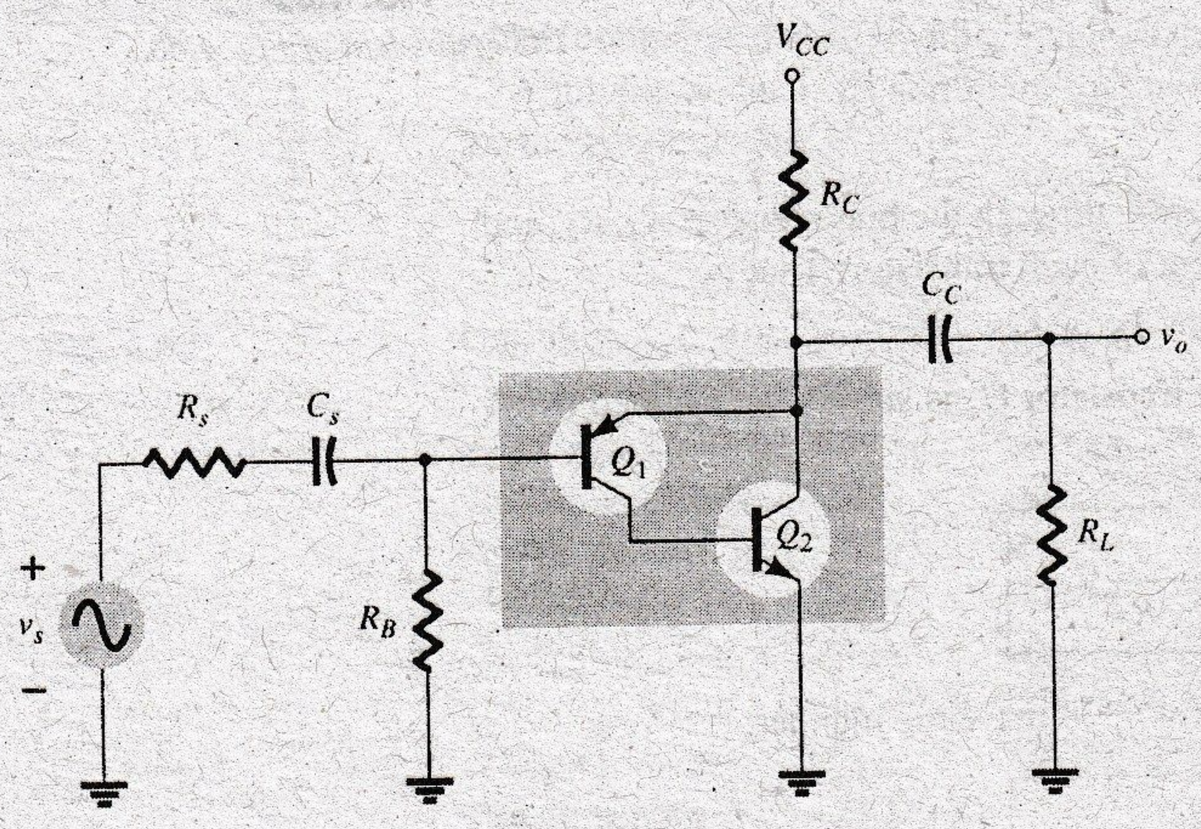


FIG. 4.70
Feedback Pair amplifier.

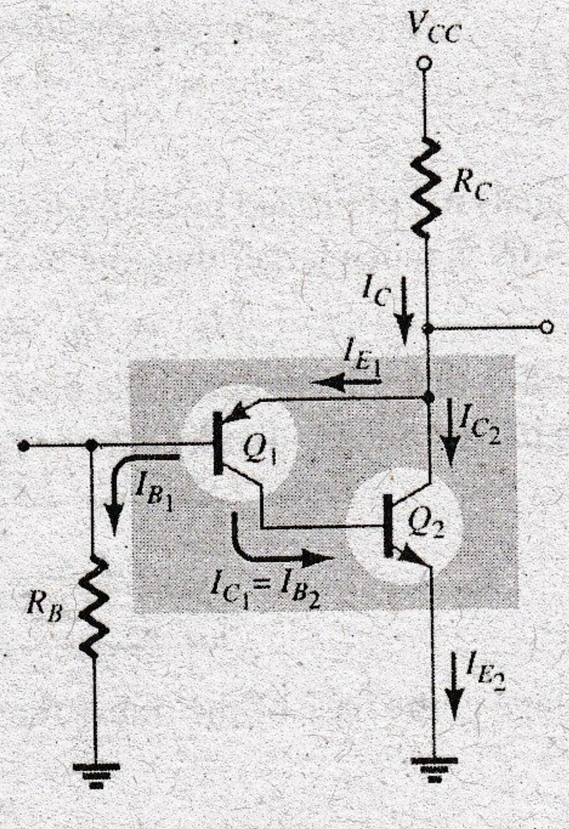


FIG. 4.71
DC equivalent of Fig. 4.70.

The base current

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1}$$

and

$$I_{C_2} = \beta_2 I_{B_2}$$

so that

$$\boxed{I_{C_2} \cong I_{E_2} = \beta_1 \beta_2 I_{B_1}} \tag{4.67}$$

The collector current

$$I_C = I_{E_1} + I_{E_2}$$
$$\cong \beta_1 I_{B_1} + \beta_1 \beta_2 I_{B_1}$$
$$= \beta_1 (1 + \beta_2) I_{B_1}$$

so that

$$\boxed{I_C \cong \beta_1 \beta_2 I_{B_1}} \tag{4.68}$$

Applying Kirchhoff's voltage law down from the source to ground will result in

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

or

$$V_{CC} - V_{EB_1} - \beta_1 \beta_2 I_{B_1} R_C - I_{B_1} R_B = 0$$

and

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1 \beta_2 R_C}} \tag{4.69}$$

The base voltage V_{B_1} is

$$\boxed{V_{B_1} = I_{B_1} R_B} \tag{4.70}$$

and

$$\boxed{V_{B_2} = V_{BE_2}} \tag{4.71}$$

The collector voltage $V_{C_2} = V_{E_1}$ is

$$\boxed{V_{C_2} = V_{CC} - I_C R_C} \tag{4.72}$$

and

$$\boxed{V_{C_1} = V_{BE_2}} \tag{4.73}$$

In this case

$$\boxed{V_{CE_2} = V_{C_2}} \tag{4.74}$$

and

$$V_{EC_1} = V_{E_1} - V_{C_1}$$

so that

$$\boxed{V_{EC_1} = V_{C_2} - V_{BE_2}} \tag{4.75}$$

The last multistage configuration to be introduced is the **Direct Coupled** amplifier such as appearing in Example 4.26. Note the absence of a coupling capacitor to isolate the dc levels of each stage. The dc levels in one stage will directly affect the dc levels in succeeding stages. The benefit is that the coupling capacitor typically limits the low-frequency response of the amplifier. Without coupling capacitors, the amplifier can amplify signals of very low frequency—in fact down to dc. The disadvantage is that any variation in dc levels due to a variety of reasons in one stage can affect the dc levels in the succeeding stages of the amplifier.

EXAMPLE 4.26 Determine the dc levels for the currents and voltages of the direct-coupled amplifier of Fig. 4.72. Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases wherein the input impedance of the next stage is quite low. The common-collector amplifier is acting like a **buffer** between stages.

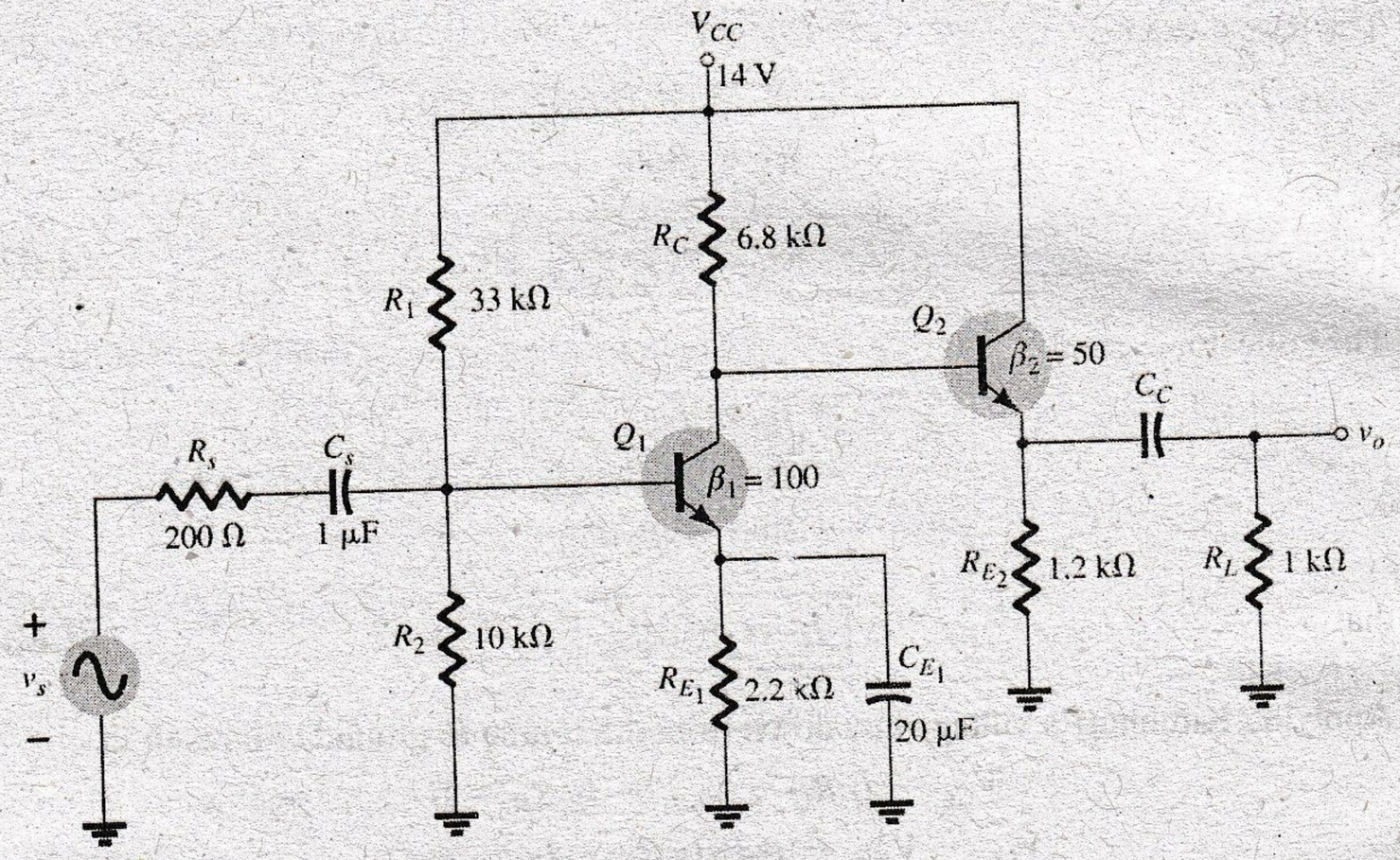


FIG. 4.72
Direct-coupled amplifier.

Solution: The dc equivalent of Fig. 4.72 appears as Fig. 4.73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 4.5.

$$I_{B_1} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_{E_1}}$$

with

$$R_{\text{Th}} = R_1 \| R_2$$

and

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

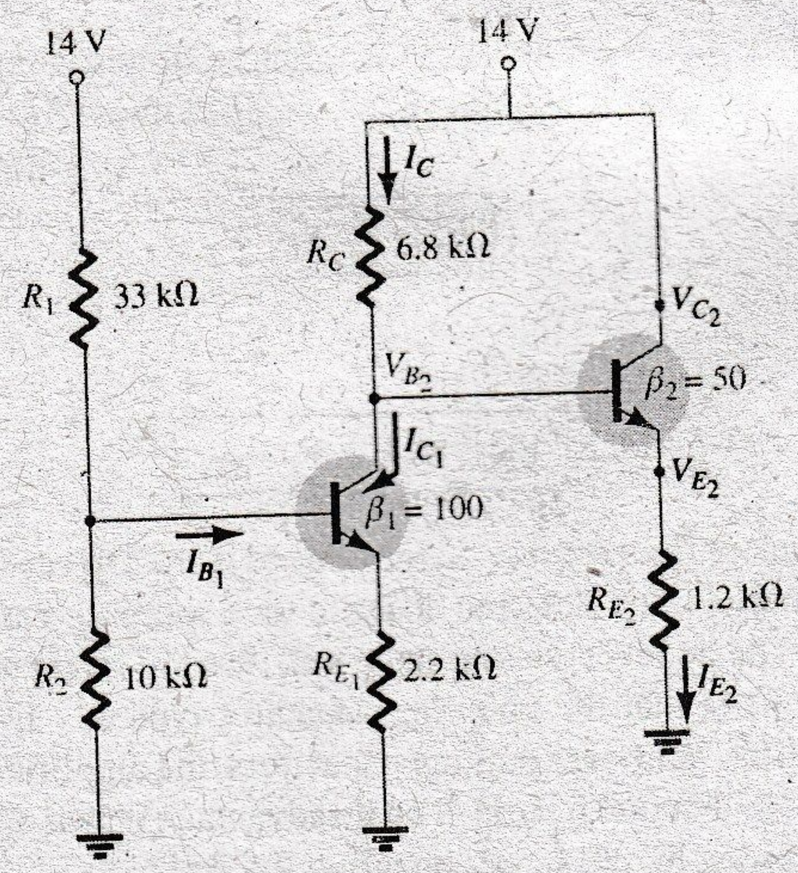


FIG. 4.73
DC equivalent of Fig. 4.72.

In this case,

$$R_{\text{Th}} = 33\ \text{k}\Omega \| 10\ \text{k}\Omega = 7.67\ \text{k}\Omega$$

and

$$E_{\text{Th}} = \frac{10\ \text{k}\Omega(14\ \text{V})}{10\ \text{k}\Omega + 33\ \text{k}\Omega} = 3.26\ \text{V}$$

so that
$$I_{B_1} = \frac{3.26\text{ V} - 0.7\text{ V}}{7.67\text{ k}\Omega + (100 + 1)\,2.2\text{ k}\Omega}$$
$$= \frac{2.56\text{ V}}{229.2\text{ k}\Omega}$$
$$= \mathbf{11.17\ \mu A}$$

with
$$I_{C_1} = \beta I_{B_1}$$
$$= 100\,(11.17\ \mu\text{A})$$
$$= \mathbf{1.12\text{ mA}}$$

In Fig. 4.73 we find that

$$\boxed{V_{B_2} = V_{CC} - I_C R_C} \qquad \textbf{(4.76)}$$

$$= 14\text{ V} - (1.12\text{ mA})(6.8\text{ k}\Omega)$$
$$= 14\text{ V} - 7.62\text{ V}$$
$$= \mathbf{6.38\text{ V}}$$

and
$$V_{E_2} = V_{B_2} - V_{BE_2}$$
$$= 6.38\text{ V} - 0.7\text{ V}$$
$$= \mathbf{5.68\text{ V}}$$

resulting in

$$\boxed{I_{E_2} = \frac{V_{E_2}}{R_{E_2}}} \qquad \textbf{(4.77)}$$

$$= \frac{5.68\text{ V}}{1.2\text{ k}\Omega}$$
$$= \mathbf{4.73\text{ mA}}$$

Obviously,

$$\boxed{V_{C_2} = V_{CC}} \qquad \textbf{(4.78)}$$

$$= 14\text{ V}$$

and
$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \qquad \textbf{(4.79)}$$

$$= 14\text{ V} - 5.68\text{ V}$$
$$= \mathbf{8.32\text{ V}}$$

4.13 CURRENT MIRRORS

The **current mirror** is a dc network in which the current through a load is controlled by a current at another point in the network. That is, if the controlling current is raised or lowered the current through the load will change to the same level. The discussion to follow will demonstrate that the effectiveness of the design is dependent on the fact that the two transistors employed have identical characteristics. The basic configuration appears in Fig. 4.74. Note that the two transistors are back to back and the collector of one is connected to the base of the two transistors.

Assume identical transistors will result in $V_{BE_1} = V_{BE_2}$ and $I_{B_1} = I_{B_2}$ as defined by the base-to-emitter characteristics of Fig. 4.75. Raise the base to emitter voltage, and the current of each will rise to the same value.

Since the base to emitter voltages of the two transistors in Fig. 4.74 are in parallel, they must have the same voltage. The result is that $I_{B_1} = I_{B_2}$ at every set base to emitter voltage.

It is clear from Fig. 4.74 that $I_B = I_{B_1} + I_{B_2}$

and if $I_{B_1} = I_{B_2}$

then $I_B = I_{B_1} + I_{B_1} = 2I_{B_1}$

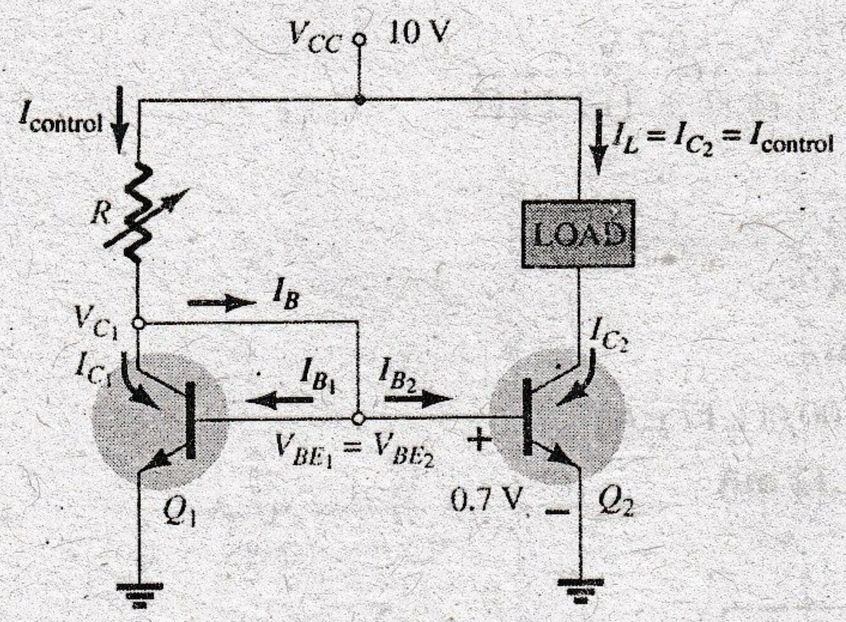


FIG. 4.74
Current mirror using back-to-back BJTs.

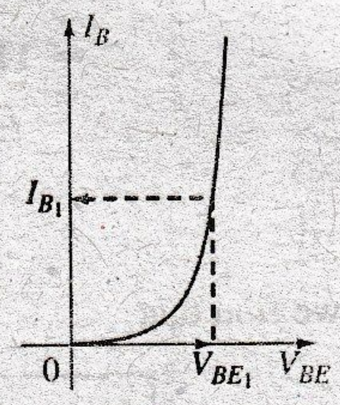


FIG. 4.75
Base characteristics for transistor Q_1 (and Q_2).

In addition,

$$I_{control} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1}$$

but

$$I_{C_1} = \beta_1 I_{B_1}$$

so

$$I_{control} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1}$$

and since β_1 is typically $\gg 2$, $I_{control} \cong \beta_1 I_{B_1}$

or

$$\boxed{I_{B_1} = \frac{I_{control}}{\beta_1}} \tag{4.80}$$

If the control current is raised, the resulting I_{B_1} will increase as determined by Eq. 4.80. If I_{B_1} increases, the voltage V_{BE_1} must increase as dictated by the response curve of Fig. 4.75. If V_{BE_1} increases, then V_{BE_2} must increase by the same amount and I_{B_2} will also increase. The result is that $I_L = I_{C_2} = \beta I_{B_2}$ will also increase to the level established by the control current.

Referring to Fig. 4.74 we find the control current is determined by

$$\boxed{I_{control} = \frac{V_{CC} - V_{BE}}{R}} \tag{4.81}$$

revealing that for a fixed V_{CC}, the resistor R can be used to set the control current.

The network also has a measure of built-in control that will try to ensure that any variation in load current will be corrected by the configuration itself. For instance, if I_L should try to increase for whatever reason, the base current of Q_2 will also increase due to the relationship $I_{B2} = I_{C2}/\beta_2 = I_L/\beta_2$. Returning to Fig. 4.101, we find that an increase in I_{B2} will cause voltage V_{BE_2} to increase also. Because the base of Q_2 is connected directly to the collector of Q_1, the voltage V_{CE_1} will increase also. This action causes the voltage across the control resistor R to decrease, causing I_R to drop. But if I_R drops, the base current I_B will drop, causing both I_{B_1} and I_{B_2} to drop also. A drop in I_{B_2} will cause the collector current and therefore the load current to drop also. The result, therefore, is a sensitivity to unwanted changes that the network will make every effort to correct.

The entire sequence of events just described can be presented on a single line as shown below. Note that at one end the load current is trying to increase, and at the end of the sequence the load current is forced to return to its original level.

$$I_L \uparrow I_{C_2} \uparrow I_{B_2} \uparrow V_{BE_2} \uparrow V_{CE_1} \downarrow, I_R \downarrow, I_B \downarrow, I_{B_2} \downarrow I_{C_2} \downarrow I_L \downarrow$$

Note

EXAMPLE 4.27 Calculate the mirrored current I in the circuit of Fig. 4.76.

Solution: Eq. (4.75):

$$I = I_{control} = \frac{V_{CC} - V_{BE}}{R} = \frac{12\text{ V} - 0.7\text{ V}}{1.1\text{ k}\Omega} = \mathbf{10.27\text{ mA}}$$

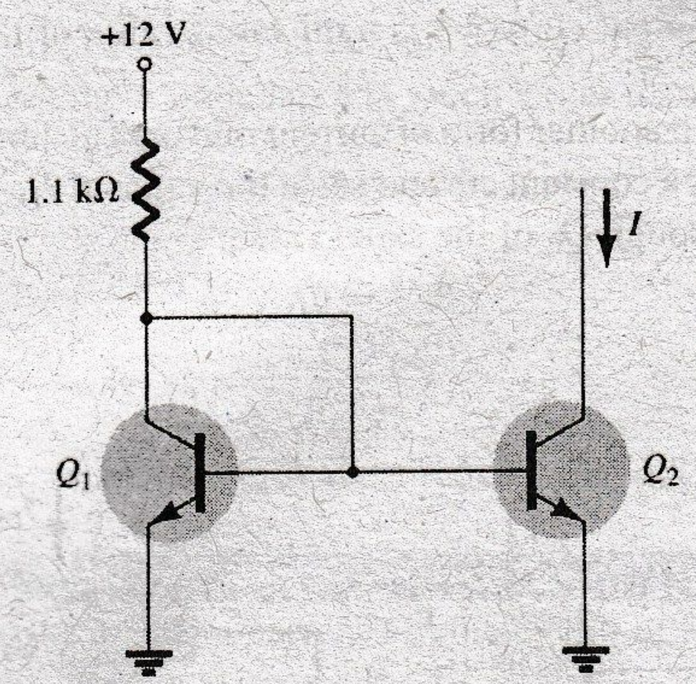


FIG. 4.76
Current mirror circuit for Example 4.27.

EXAMPLE 4.28 Calculate the current I through each of the transistor Q_2 and Q_3 in the circuit of Fig. 4.77.

Solution: Since $V_{BE_1} = V_{BE_2} = V_{BE_3}$ then $I_{B_1} = I_{B_2} = I_{B_3}$

Substituting $I_{B_1} = \dfrac{I_{\text{control}}}{\beta}$ and $I_{B_2} = \dfrac{I}{\beta}$ with $I_{B_3} = \dfrac{I}{\beta}$

we have $$\frac{I_{\text{control}}}{\beta} = \frac{I}{\beta} = \frac{I}{\beta}$$

so I must equal I_{control}

and $$I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{6\text{ V} - 0.7\text{ V}}{1.3\text{ k}\Omega} = \mathbf{4.08\text{ mA}}$$

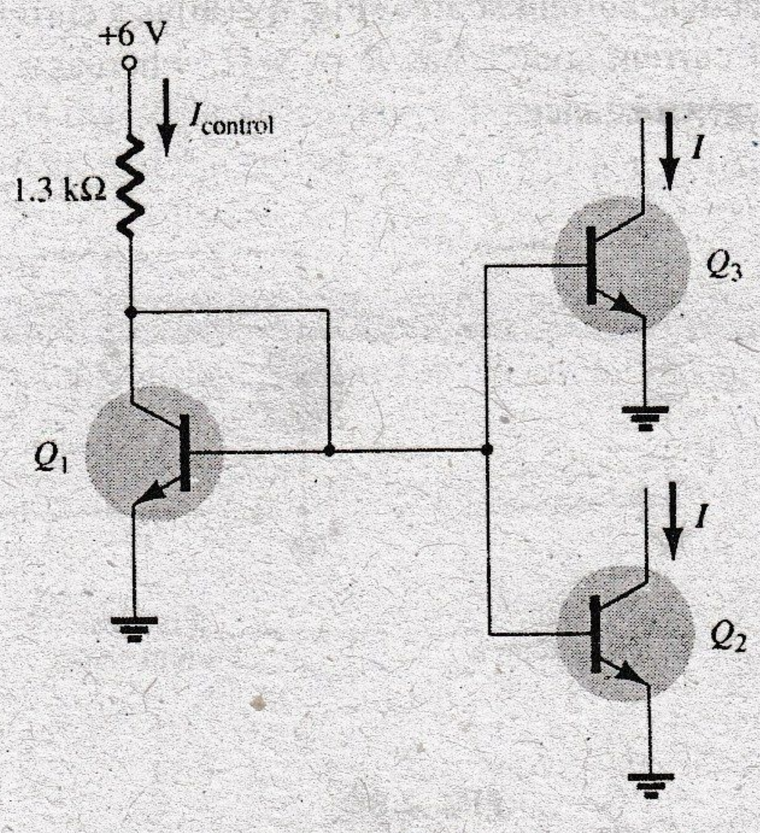


FIG. 4.77
Current mirror circuit for Example 4.28.

Figure 4.78 shows another form of current mirror to provide higher output impedance than that of Fig. 4.74. The control current through R is

$$I_{\text{control}} = \frac{V_{CC} - 2V_{BE}}{R} \approx I_C + \frac{I_C}{\beta} = \frac{\beta + 1}{\beta} I_C \approx I_C$$

Assuming that Q_1 and Q_2 are well matched, we find that the output current I is held constant at

$$I \approx I_C = I_{\text{control}}$$

Again we see that the output current I is a mirrored value of the current set by the fixed current through R.

Figure 4.79 shows still another form of current mirror. The junction field effect transistor (see Chapter 6) provides a constant current set at the value of I_{DSS}. This current is mirrored, resulting in a current through Q_2 of the same value:

$$I = I_{DSS}$$

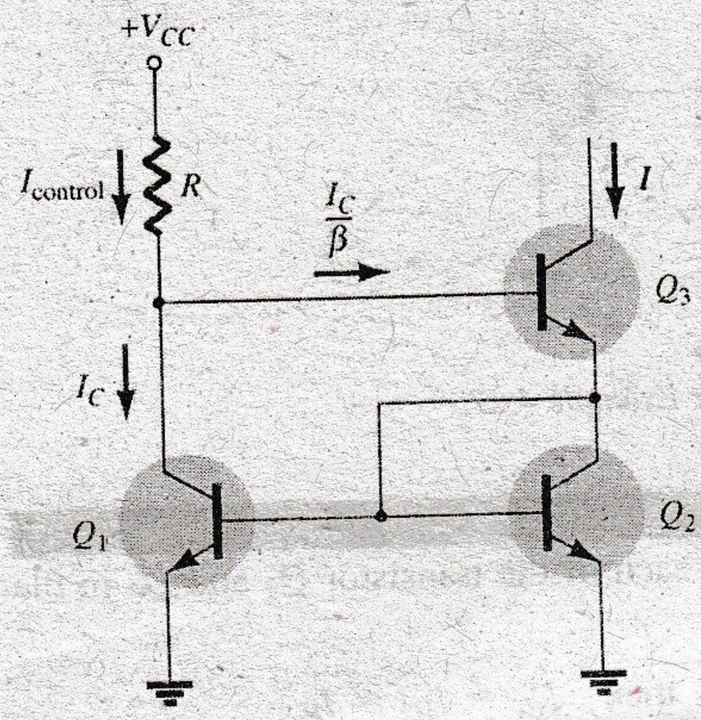


FIG. 4.78
Current mirror circuit with higher output impedance.

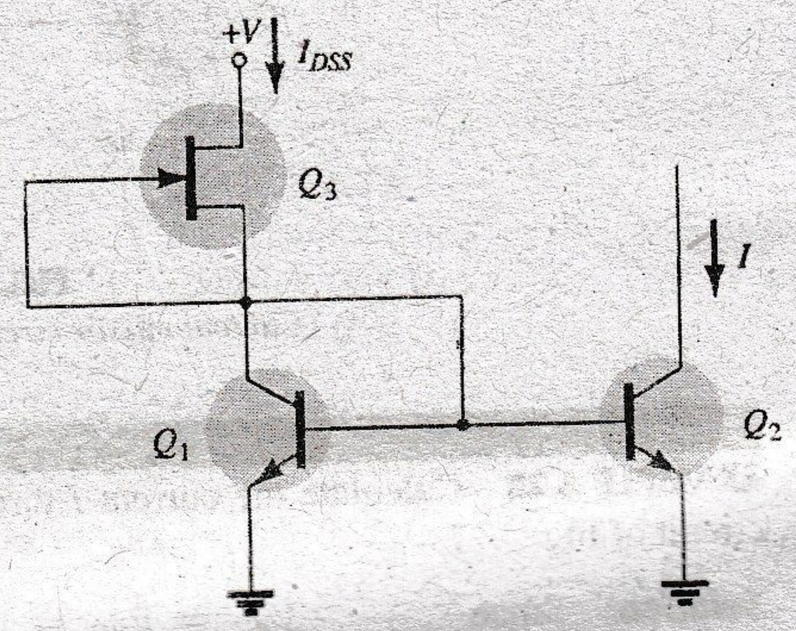


FIG. 4.79
Current mirror connection.

4.14 CURRENT SOURCE CIRCUITS

The concept of a power supply provides the starting point in our consideration of current source circuits. A practical voltage source (Fig. 4.80a) is a voltage supply in series with a resistance. An ideal voltage source has $R = 0$, whereas a practical source includes some small resistance. A practical current source (Fig. 4.80b) is a current supply in parallel with a resistance. An ideal current source has $R = \infty\Omega$, whereas a practical current source includes some very large resistance.

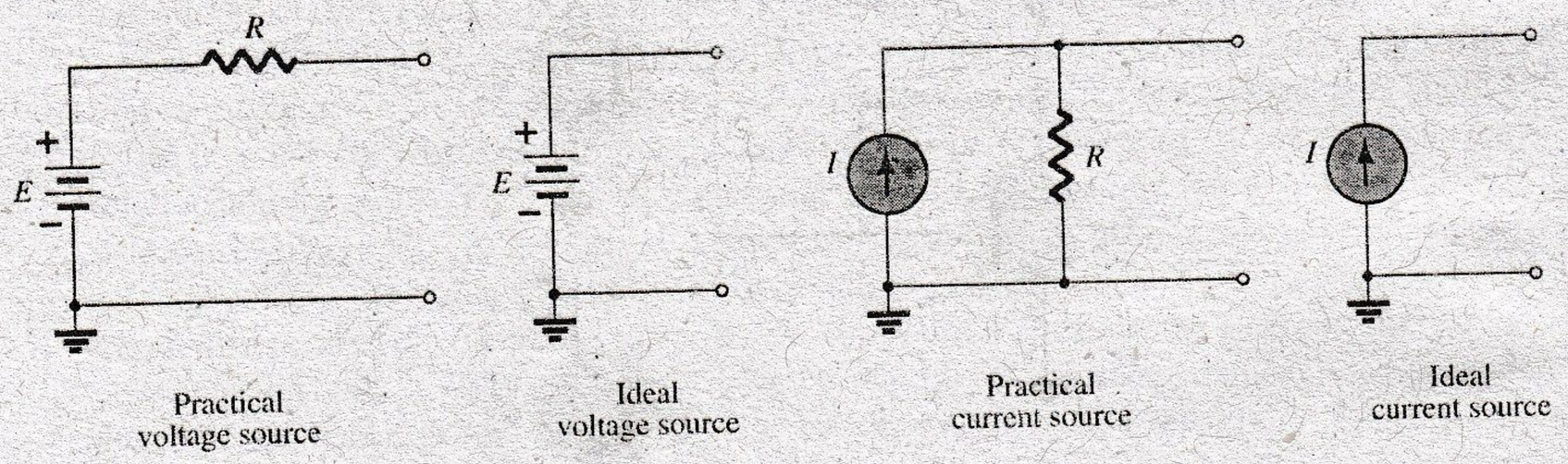


FIG. 4.80
Voltage and current sources.

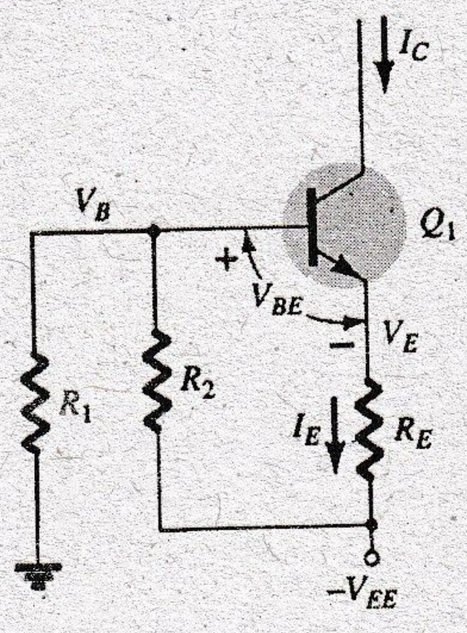


FIG. 4.81
Discrete constant-current source.

An ideal current source provides a constant current regardless of the load connected to it. There are many uses in electronics for a circuit providing a constant current at a very high impedance. Constant-current circuits can be built using bipolar devices, FET devices, and a combination of these components. There are circuits used in discrete form and others more suitable for operation in integrated circuits.

Bipolar Transistor Constant-Current Source

Bipolar transistors can be connected in a circuit that acts as a constant-current source in a number of ways. Figure 4.81 shows a circuit using a few resistors and an *npn* transistor for

operation as a constant-current circuit. The current through I_E can be determined as follows. Assuming that the base input impedance is much larger than R_1 or R_2, we have

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE})$$

and

$$V_E = V_B - 0.7\,\text{V}$$

with

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C \tag{4.82}$$

where I_C is the constant current provided by the circuit of Fig. 4.81.

EXAMPLE 4.29 Calculate the constant current I in the circuit of Fig. 4.82.

Solution:

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE}) = \frac{5.1\,\text{k}\Omega}{5.1\,\text{k}\Omega + 5.1\,\text{k}\Omega}(-20\,\text{V}) = -10\,\text{V}$$

$$V_E = V_B - 0.7\,\text{V} = 10\,\text{V} - 0.7\,\text{V} = -10.7\,\text{V}$$

$$I = I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-10.7\,\text{V} - (-20\,\text{V})}{2\,\text{k}\Omega}$$

$$= \frac{9.3\,\text{V}}{2\,\text{k}\Omega} = \mathbf{4.65\,mA}$$

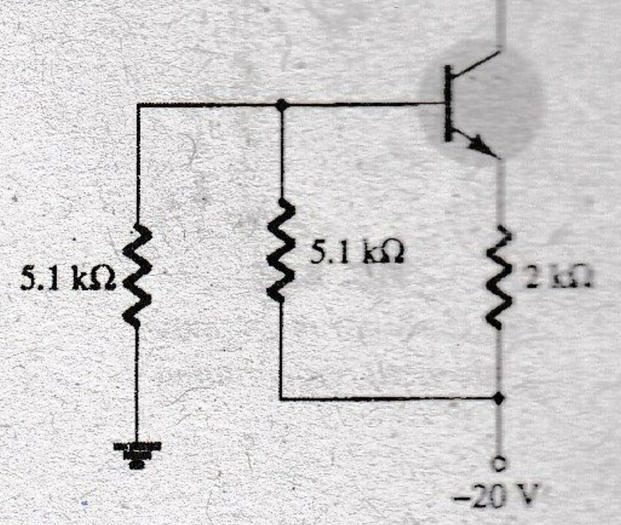


FIG. 4.82
Constant-current source for Example 4.29.

Transistor/Zener Constant-Current Source

Replacing resistor R_2 with a Zener diode, as shown in Fig. 4.83, provides an improved constant-current source over that of Fig. 4.81. The Zener diode results in a constant current calculated using the base-emitter KVL (Kirchhoff voltage loop) equation. The value of I can be calculated using

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E} \tag{4.83}$$

A major point to consider is that the constant current depends on the Zener diode voltage, which remains quite constant, and the emitter resistor R_E. The voltage supply V_{EE} has no effect on the value of I.

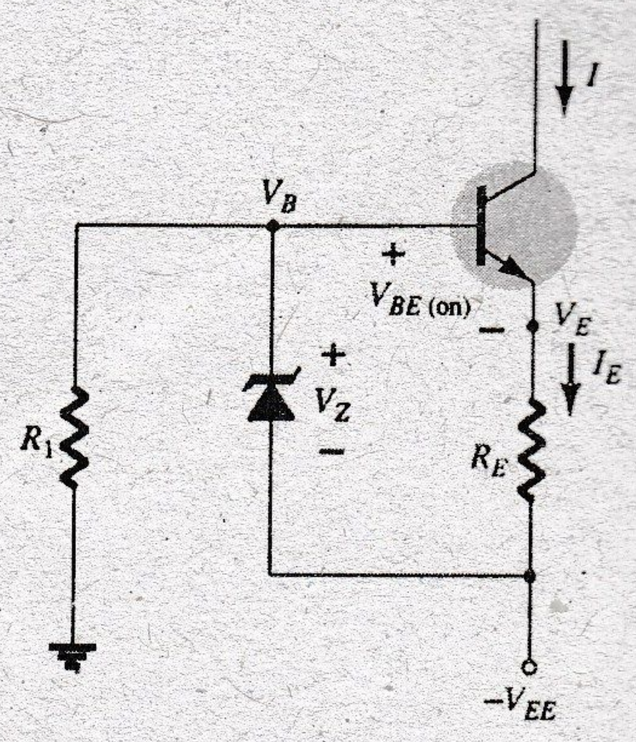


FIG. 4.83
Constant-current circuit using Zener diode.

EXAMPLE 4.30 Calculate the constant current I in the circuit of Fig. 4.84.

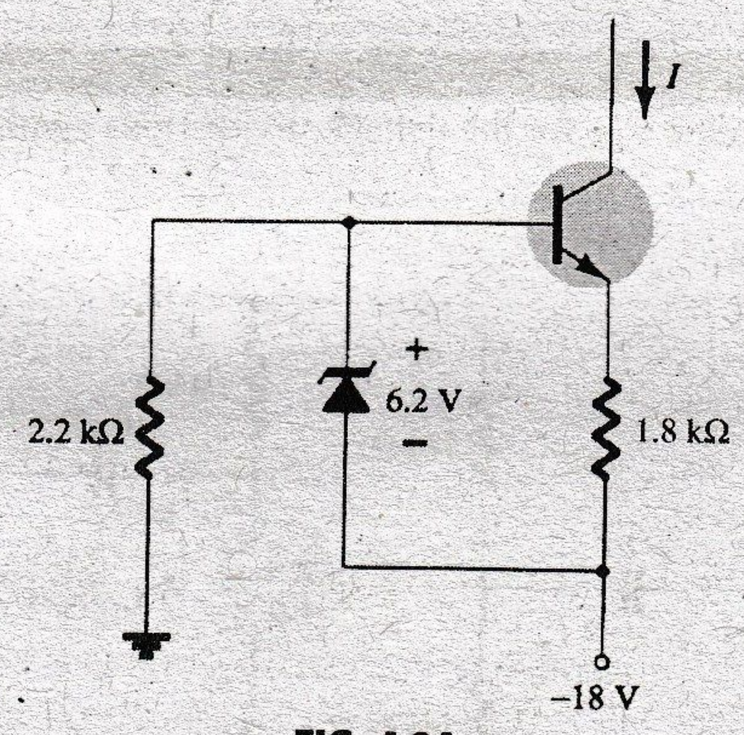


FIG. 4.84
Constant-current circuit for Example 4.30.

Solution:

$$\text{Eq. (4.83):}\quad I = \frac{V_Z - V_{BE}}{R_E} = \frac{6.2\,\text{V} - 0.7\,\text{V}}{1.8\,\text{k}\Omega} = 3.06\,\text{mA} \approx \mathbf{3\,mA}$$

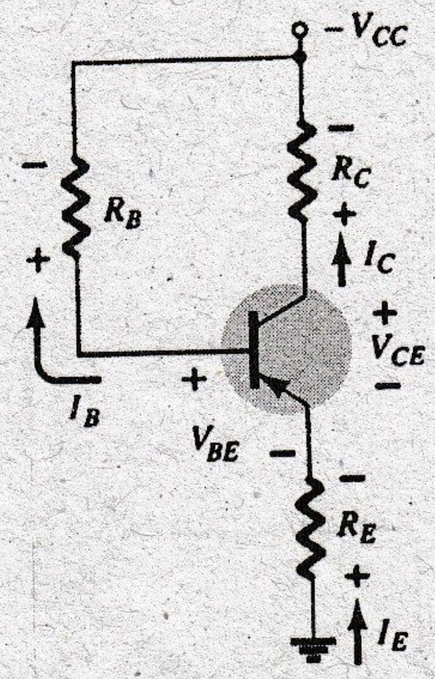


FIG. 4.85
pnp transistor in an emitter-stabilized configuration.

4.15 *pnp* TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of I_B is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

As noted in Fig. 4.85, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.85, both V_{BE} and V_{CE} will be negative quantities.

Applying Kirchhoff's voltage law to the base–emitter loop results in the following equation for the network of Fig. 4.85:

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$\boxed{I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E}} \qquad (4.84)$$

The resulting equation is the same as Eq. (4.17) except for the sign for V_{BE}. However, in this case $V_{BE} = -0.7$ V and the substitution of values results in the same sign for each term of Eq. (4.84) as Eq. (4.17). Keep in mind that the direction of I_B is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.85.

For V_{CE} Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ gives

$$\boxed{V_{CE} = -V_{CC} + I_C(R_C + R_E)} \qquad (4.85)$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Because V_{CC} will be larger than the magnitude of the succeeding term, the voltage V_{CE} will have a negative sign, as noted in an earlier paragraph.

EXAMPLE 4.31 Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.86.

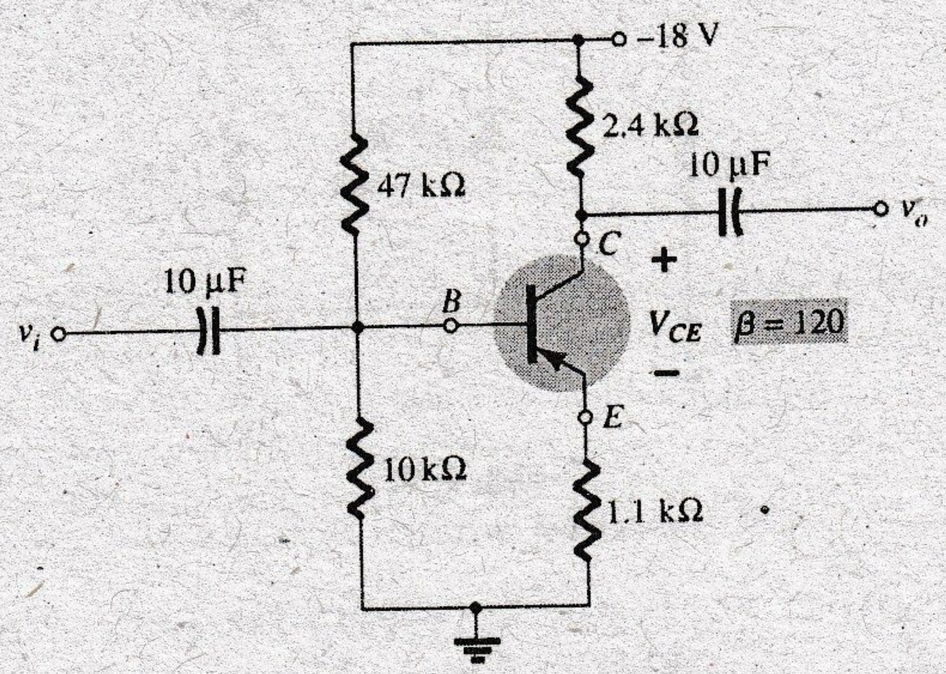


FIG. 4.86
pnp transistor in a voltage-divider bias configuration.

Solution: Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$(120)(1.1\,\text{k}\Omega) \geq 10(10\,\text{k}\Omega)$$
$$132\,\text{k}\Omega \geq 100\,\text{k}\Omega \quad (\textit{satisfied})$$

Solving for V_B, we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10\,\text{k}\Omega)(-18\,\text{V})}{47\,\text{k}\Omega + 10\,\text{k}\Omega} = -3.16\,\text{V}$$

Note the similarity in format of the equation with the resulting negative voltage for V_B.

Applying Kirchhoff's voltage law around the base–emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$V_E = -3.16\,\text{V} - (-0.7\,\text{V})$$
$$= -3.16\,\text{V} + 0.7\,\text{V}$$
$$= -2.46\,\text{V}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation $V_E = V_B - V_{BE}$ would be exactly the same. The only difference surfaces when the values are substituted.

The current is

$$I_E = \frac{V_E}{R_E} = \frac{2.46\,\text{V}}{1.1\,\text{k}\Omega} = 2.24\,\text{mA}$$

For the collector–emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

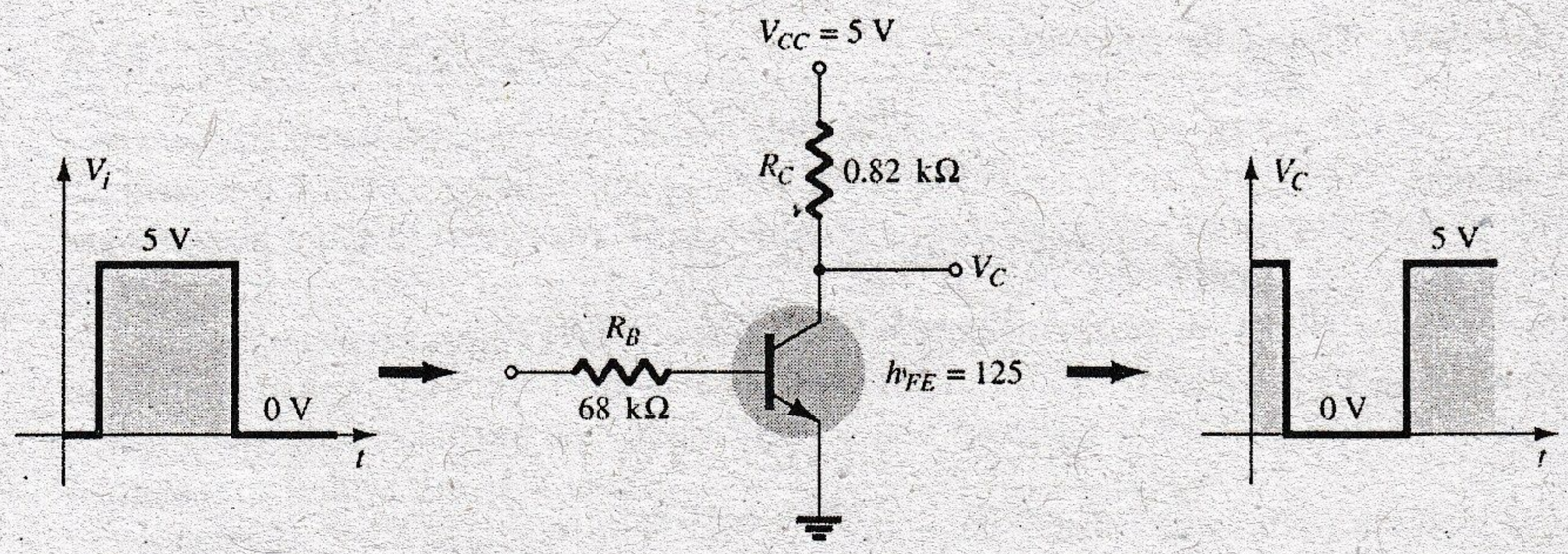
$$V_{CE} = -18\,\text{V} + (2.24\,\text{mA})(2.4\,\text{k}\Omega + 1.1\,\text{k}\Omega)$$
$$= -18\,\text{V} + 7.84\,\text{V}$$
$$= \mathbf{-10.16\,V}$$

4.16 TRANSISTOR SWITCHING NETWORKS

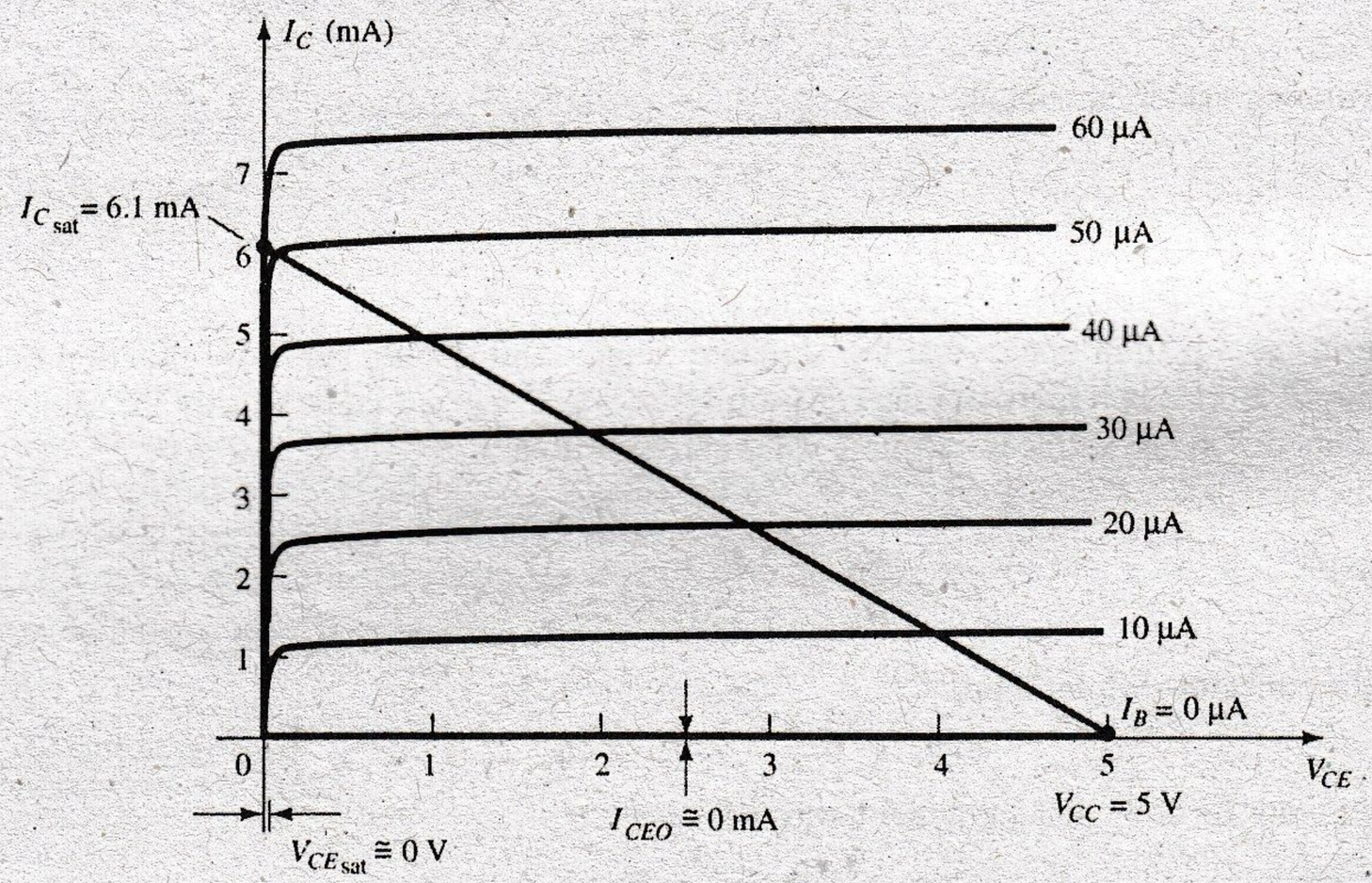
The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can be used as switches for computer and control applications. The network of Fig. 4.87a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V. The resistor R_B will ensure that the full applied voltage of 5 V will not appear across the base-to-emitter junction. It will also set the I_B level for the "on" condition.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.87b. For our purposes we will assume that $I_C = I_{CEO} \cong 0\,\text{mA}$ when $I_B = 0\,\mu\text{A}$ (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.87b. In addition, we will assume that $V_{CE} = V_{CE_{sat}} \cong 0\,\text{V}$ rather than the typical 0.1-V to 0.3-V level.

When $V_i = 5\,\text{V}$, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing



(a)



(b)

FIG. 4.87
Transistor inverter.

near the saturation level. In Fig. 4.87b, this requires that $I_B > 50\ \mu A$. The saturation level for the collector current for the circuit of Fig. 4.87a is defined by

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.86}$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$I_B > \frac{I_{C_{sat}}}{\beta_{dc}} \tag{4.87}$$

For the network of Fig. 4.87b, when $V_i = 5$ V, the resulting level of I_B is

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (4.87) gives

$$I_B = 63\,\mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\,\mu\text{A}$$

which is satisfied. Certainly, any level of I_B greater than 60 μA will pass through a Q-point on the load line that is very close to the vertical axis.

For $V_i = 0$ V, $I_B = 0\,\mu$A, and because we are assuming that $I_C = I_{CEO} = 0$ mA, the voltage drop across R_C as determined by $V_{RC} = I_C R_C = 0$ V, resulting in $V_C = +5$ V for the response indicated in Fig. 4.87a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current I_C is quite high and the voltage V_{CE} very low. The result is a resistance level between the two terminals determined by

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

and is depicted in Fig. 4.88.

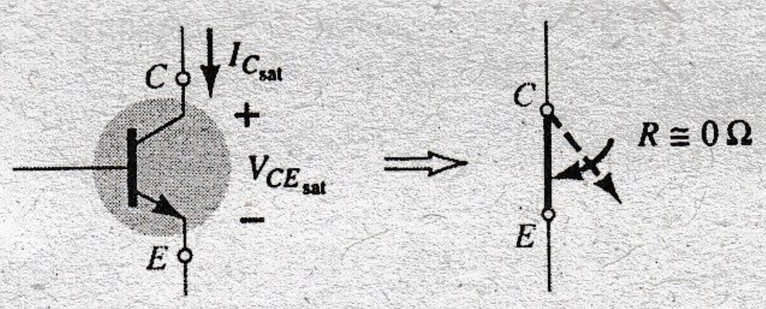


FIG. 4.88
Saturation conditions and the resulting terminal resistance.

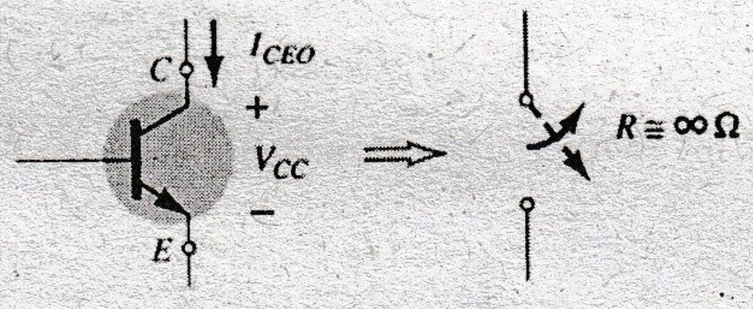


FIG. 4.89
Cutoff conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{sat}}$ such as 0.15 V gives

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\,\Omega$$

which is a relatively low value and can be considered as approximately 0 Ω when placed in series with resistors in the kilohm range.

For $V_i = 0$ V, as shown in Fig. 4.89, the cutoff condition results in a resistance level of the following magnitude:

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \infty\,\Omega$$

resulting in the open-circuit equivalence. For a typical value of $I_{CEO} = 10\,\mu$A, the magnitude of the cutoff resistance is

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\,\mu\text{A}} = \mathbf{500\text{ k}\Omega}$$

which certainly approaches an open-circuit equivalence for many situations.

EXAMPLE 4.32 Determine R_B and R_C for the transistor inverter of Fig. 4.90 if $I_{C_{sat}} = 10$ mA.

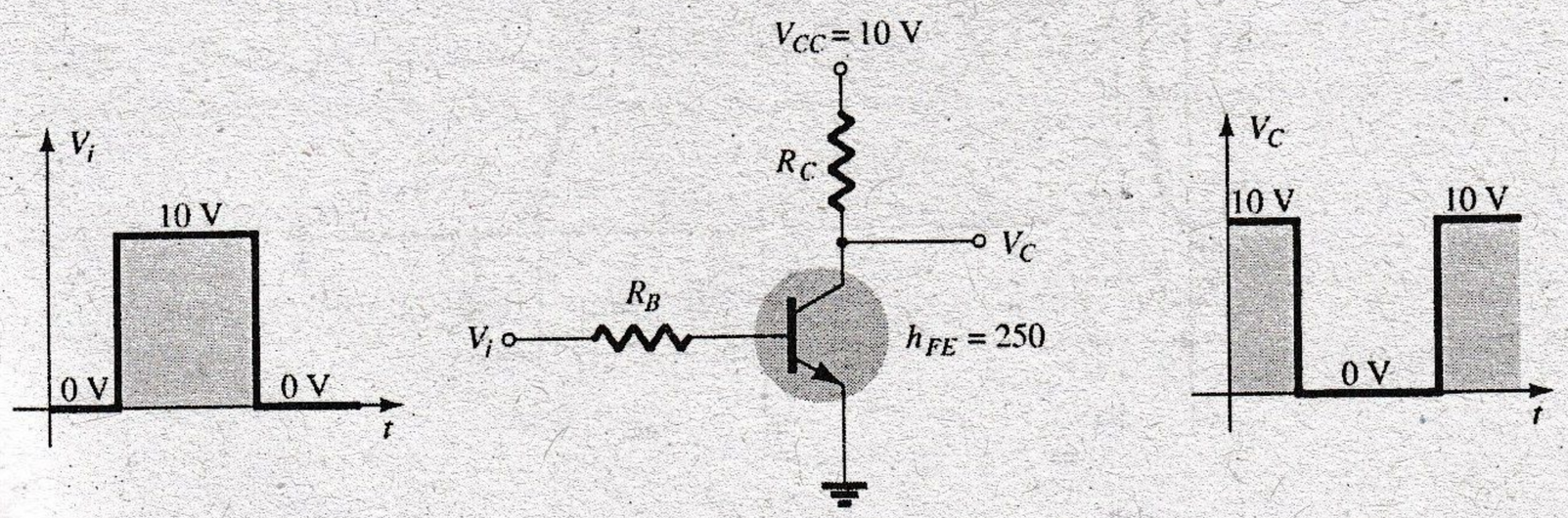


FIG. 4.90
Inverter for Example 4.32.

Solution: At saturation,

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation,

$$I_B \cong \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{10\text{ mA}}{250} = 40\ \mu\text{A}$$

Choosing $I_B = 60\ \mu$A to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain

$$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\ \mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\text{ k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\ \mu\text{A}$$

and

$$I_B = 62\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = 40\ \mu\text{A}$$

Therefore, use $R_B = \mathbf{150\text{ k}\Omega}$ and $R_C = \mathbf{1\text{ k}\Omega}$.

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.91. The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and is defined by

$$\boxed{t_{on} = t_r + t_d} \tag{4.88}$$

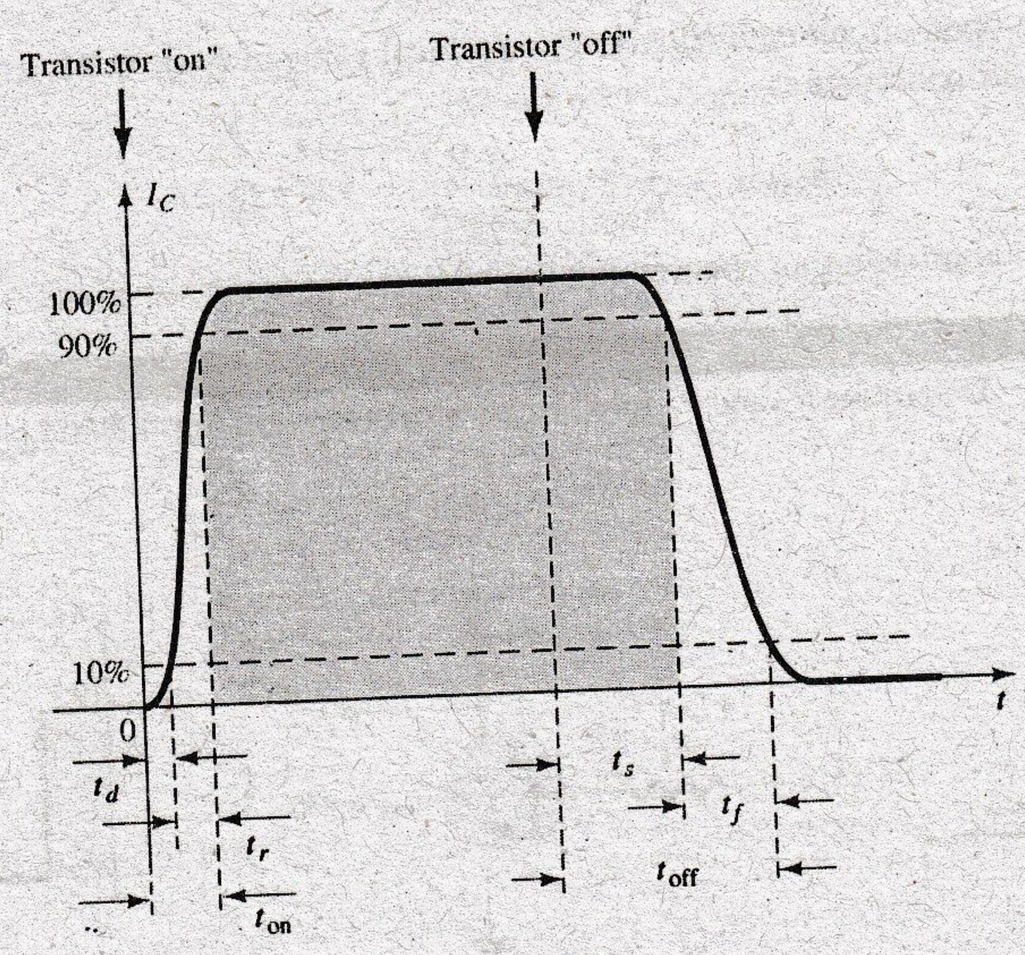


FIG. 4.91
Defining the time intervals of a pulse waveform.

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$\boxed{t_{off} = t_s + t_f} \tag{4.89}$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at $I_C = 10$ mA, we find that

$$t_s = 120 \text{ ns}$$
$$t_d = 25 \text{ ns}$$
$$t_r = 13 \text{ ns}$$

and $$t_f = 12 \text{ ns}$$

so that $$t_{on} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = \mathbf{38 \text{ ns}}$$

and $$t_{off} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = \mathbf{132 \text{ ns}}$$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises:

$$t_{on} = \mathbf{12 \text{ ns}} \text{ and } t_{off} = \mathbf{18 \text{ ns}}$$

4.17 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

For an "on" transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.

The proper connections for measuring V_{BE} appear in Fig. 4.92. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V or a negative value, would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used, but a negative reading should be expected.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of V_{CE} in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless it is being employed in a switching mode. However:

For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

For $V_{CC} = 20$ V, a reading of V_{CE} of 1 V to 2 V or from 18 V to 20 V as measured in Fig. 4.93 is certainly an uncommon result, and unless the device was knowingly designed for this response, the design and operation should be investigated. If $V_{CE} = 20$ V (with $V_{CC} = 20$ V) at least two possibilities exist—either the device (BJT) is damaged and has the characteristics

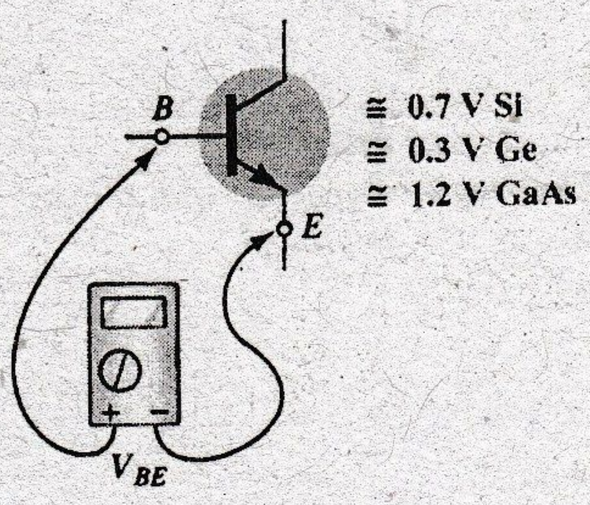


FIG. 4.92
Checking the dc level of V_{BE}.

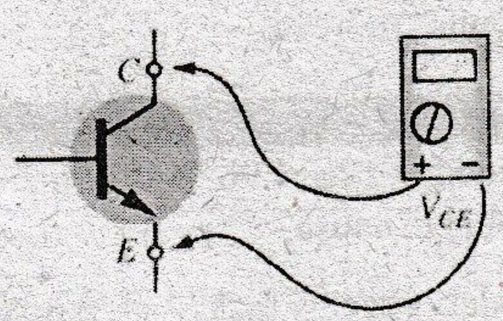


FIG. 4.93
Checking the dc level of V_{CE}.

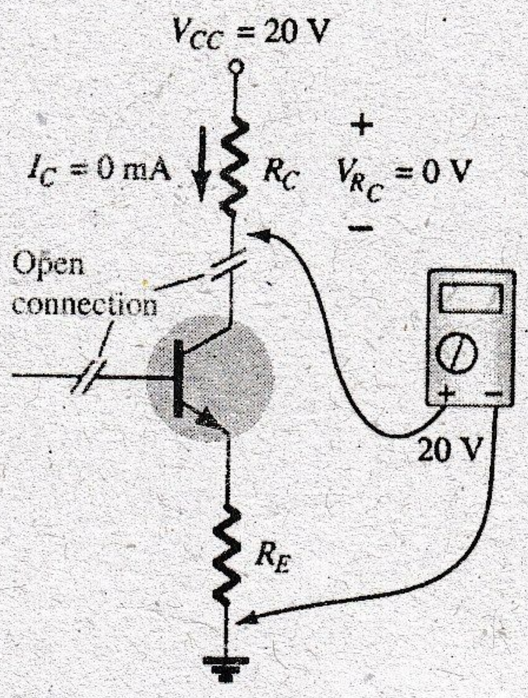


FIG. 4.94
Effect of a poor connection or damaged device.

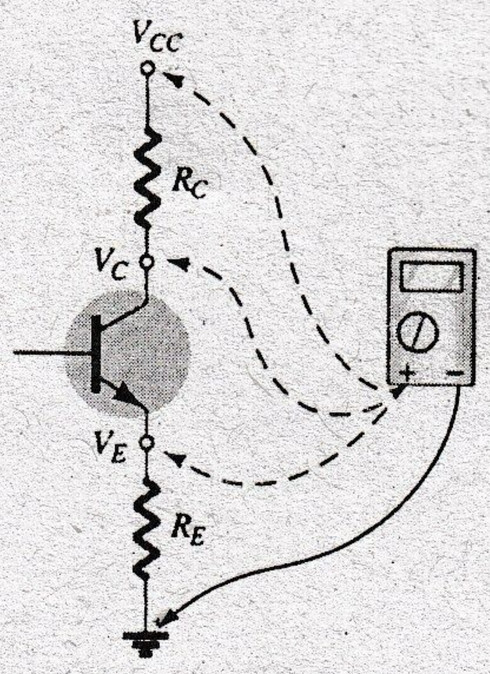


FIG. 4.95
Checking voltage levels with respect to ground.

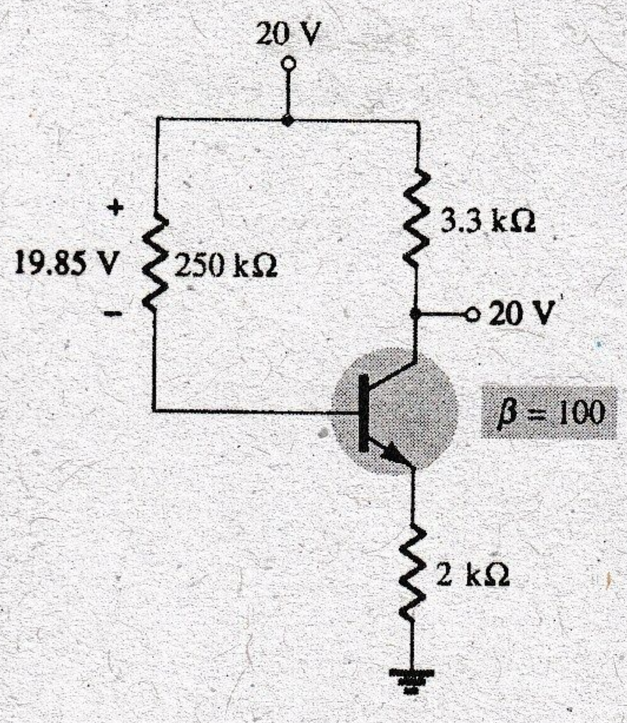


FIG. 4.96
Network for Example 4.33.

of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.94, establishing I_C at 0 mA and $V_{R_C} = 0$ V. In Fig. 4.94, the black lead of the voltmeter is connected to the common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a consequent zero voltage drop across R_C will result in a reading of 20 V. If the meter is connected between the collector terminal and ground of the BJT, the reading will be 0 V because V_{CC} is blocked from the active device by the open circuit. One of the most common errors in the laboratory is the use of the wrong resistance value for a given design. Imagine the impact of using a 680-Ω resistor for R_B rather than the design value of 680 kΩ. For $V_{CC} = 20$ V and a fixed-bias configuration, the resulting base current would be

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\ \Omega} = 28.4\text{ mA}$$

rather than the desired 28.4 μA—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Because actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is measurements closer to theoretical levels and some insurance that the correct resistance value is being employed.

There are times when frustration will develop. You check the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection of a lead is faulty? How often has simply touching a lead at the proper point created a "make or break" situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader is the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and "touching" the important terminals with the red (positive) lead. In Fig. 4.95, if the red lead is connected directly to V_{CC}, it should read V_{CC} volts because the network has one common ground for the supply and network parameters. At V_C the reading should be less, as determined by the drop across R_C, and V_E should be less than V_C by the collector–emitter voltage V_{CE}. The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If V_{R_C} and V_{R_E} are reasonable values but V_{CE} is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if V_{CE} registers a level of about 0.3 V as defined by $V_{CE} = V_C - V_E$ (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than "breaking" the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.

EXAMPLE 4.33 Based on the readings provided in Fig. 4.96, determine whether the network is operating properly and, if not, the probable cause.

Solution: The 20 V at the collector immediately reveals that $I_C = 0$ mA, due to an open circuit or a nonoperating transistor. The level of $V_{R_B} = 19.85$ V also reveals that the transistor is "off" because the difference of $V_{CC} - V_{R_B} = 0.15$ V is less than that required

to turn "on" the transistor and provide some voltage for V_E. In fact, if we assume a short-circuit condition from base to emitter, we obtain the following current through R_B:

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20\text{ V}}{252\text{ k}\Omega} = 79.4\ \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85\text{ V}}{250\text{ k}\Omega} = 79.4\ \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (101)(2\text{ k}\Omega)} = \frac{19.3\text{ V}}{452\text{ k}\Omega} = 42.7\ \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

EXAMPLE 4.34 Based on the readings appearing in Fig. 4.97, determine whether the transistor is "on" and the network is operating properly.

Solution: Based on the resistor values of R_1 and R_2 and the magnitude of V_{CC}, the voltage $V_B = 4$ V seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an "on" transistor. However, the 20 V at the collector reveals that $I_C = 0$ mA, although the connection to the supply must be "solid" or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between R_C and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohm-meter, and if it is okay, check the transistor using one of the methods described in Chapter 3.

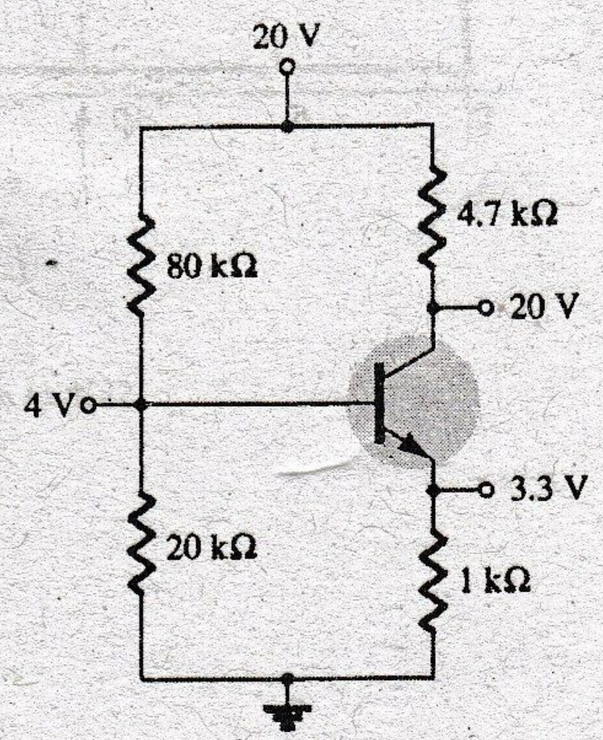


FIG. 4.97
Network for Example 4.34.

4.18 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 2.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.2 reveals how the levels of I_{CO} and V_{BE} change with increase in temperature for a particular transistor. At room temperature (about 25°C) $I_{CO} = 0.1$ nA, whereas at 100°C (boiling point of water) I_{CO} is about 200 times larger, at 20 nA. For the same temperature variation, β increases from 50 to 80 and V_{BE} drops from 0.65 V to 0.48 V. Recall that I_B is quite sensitive to the level of V_{BE}, especially for levels beyond the threshold value.

TABLE 4.2
Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE} (V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

The effect of changes in leakage current (I_{CO}) and current gain (β) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.98a and b. Figure 4.98 shows how the transistor collector characteristics change from a temperature of

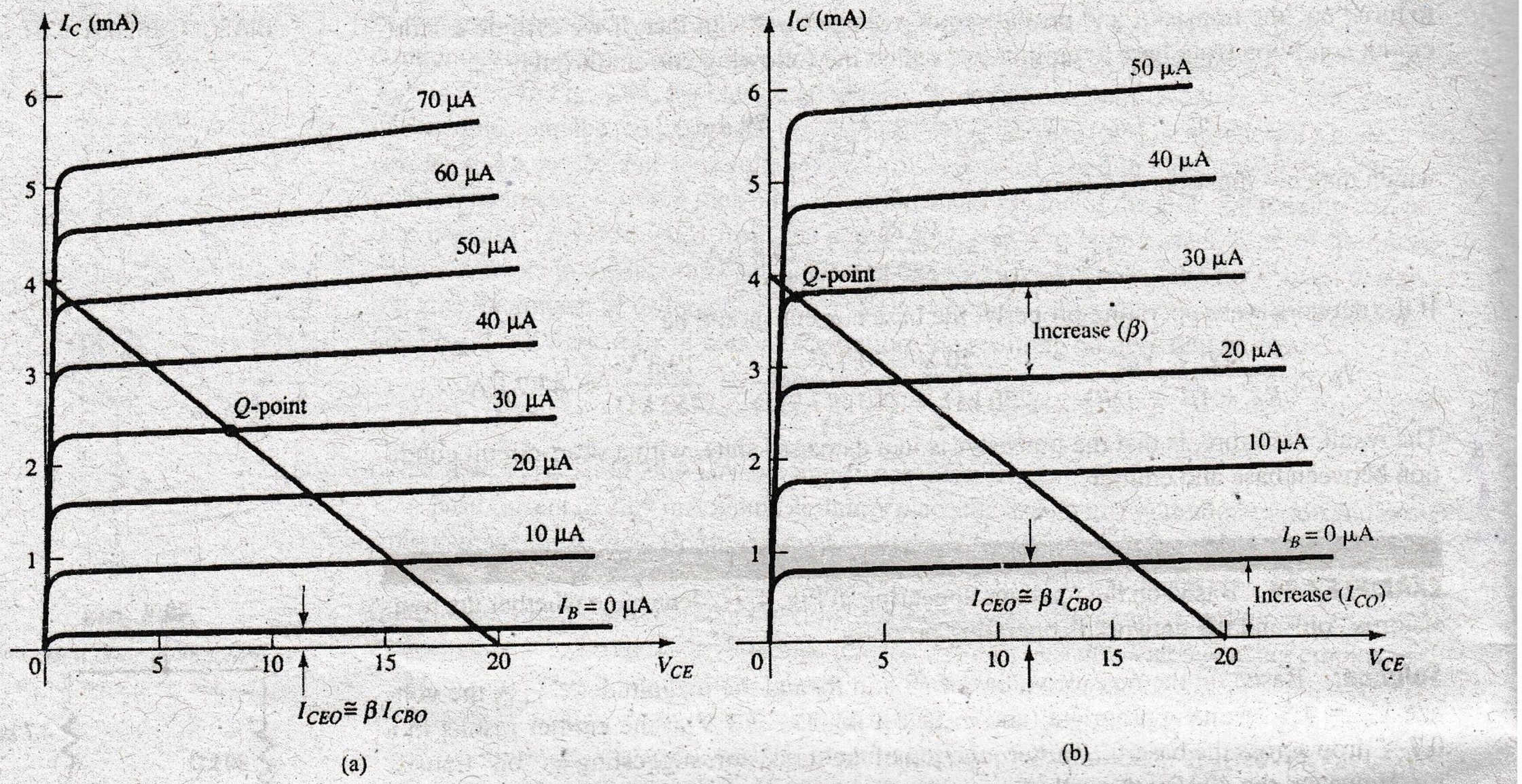


FIG. 4.98

Shift in dc bias point (Q-point) due to change in temperature: (a) 25°C; (b) 100°C.

25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise, but also causes an increase in beta, as revealed by the larger spacing between curves.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.98a at $I_B = 30\,\mu A$. Because the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.98b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector–emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

Stability Factors $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor S is defined for each of the parameters affecting bias stability as follows:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \tag{4.90}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \tag{4.91}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \tag{4.92}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity

in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.90) through (4.92) to be sensitivity factors because:

The higher the stability factor, the more sensitive is the network to variations in that parameter.

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject. Our analysis will begin with the $S(I_{CO})$ level for each configuration.

$S(I_{CO})$

Fixed-Bias Configuration

For the fixed-bias configuration, the following equation results:

$$\boxed{S(I_{CO}) \cong \beta} \tag{4.93}$$

Emitter-Bias Configuration

For the emitter-bias configuration of Section 4.4, an analysis of the network results in

$$\boxed{S(I_{CO}) \cong \frac{\beta(1 + R_B/R_E)}{\beta + R_B/B_E}} \tag{4.94}$$

For $R_B/R_E \gg \beta$, Eq. (4.94) reduces to the following:

$$\boxed{S(I_{CO}) \cong \beta}_{R_B/R_E \gg \beta} \tag{4.95}$$

as shown on the graph of $S(I_{CO})$ versus R_B/R_E in Fig. 4.99.

For $R_B/R_E \ll 1$, Eq. (4.94) will approach the following level (as shown in Fig. 4.99):

$$\boxed{S(I_{CO}) \cong 1}_{R_B/R_E \ll 1} \tag{4.96}$$

revealing that the stability factor will approach its lowest level as R_E becomes sufficiently large. Keep in mind, however, that good bias control normally requires that R_B be greater than R_E. The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.99 that the lowest value of $S(I_{CO})$ is 1, revealing that I_C will always increase at a rate equal to or greater than I_{CO}.

For the range where R_B/R_E ranges between 1 and $(\beta + 1)$, the stability factor will be determined by

$$\boxed{S(I_{CO}) \cong \frac{R_B}{R_E}} \tag{4.97}$$

The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches β.

Note that the equation for the fixed-bias configuration matches the maximum value for emitter-bias configuration. The result clearly reveals that the fixed-bias configuration a poor stability factor and a high sensitivity to variations in I_{CO}.

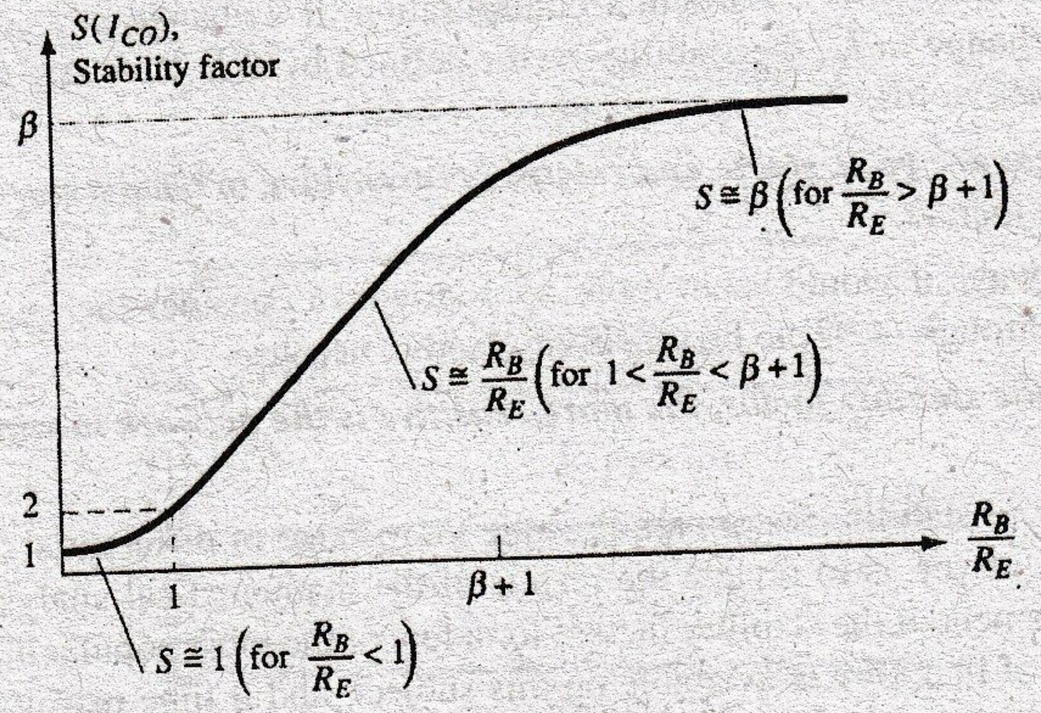


FIG. 4.99
Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the emitter-bias configuration.

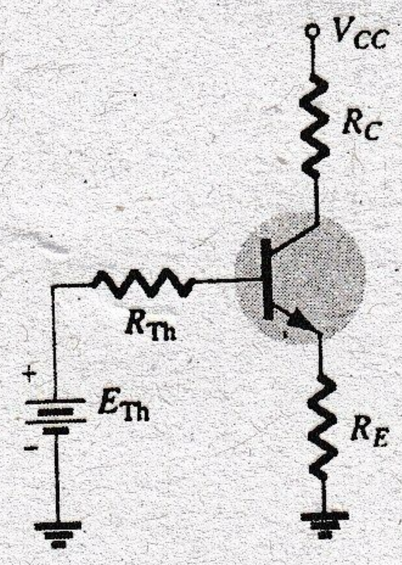


FIG. 4.100
Equivalent circuit for the voltage-divider configuration.

Voltage-Divider Bias Configuration

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.100, for the voltage-divider bias configuration. For the network of Fig. 4.100, the equation for $S(I_{CO})$ is the following:

$$S(I_{CO}) \cong \frac{\beta(1 + R_{Th}/R_E)}{\beta + R_{Th}/R_E} \tag{4.98}$$

Note the similarities with Eq. (4.94), where it was determined that $S(I_{CO})$ had its lowest level and the network had its greatest stability when $R_E > R_B$. For Eq. (4.98), the corresponding condition is $R_E > R_{Th}$, or R_{Th}/R_E should be as small as possible. For the voltage-divider bias configuration, R_{Th} can be much less than the corresponding R_{Th} of the emitter-bias configuration and still have an effective design.

Feedback-Bias Configuration ($R_E = 0\ \Omega$)

In this case,

$$S(I_{CO}) \cong \frac{\beta(1 + R_B/R_C)}{\beta + R_B/R_C} \tag{4.99}$$

Because the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.101a, the equation for the base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$I_C = \beta I_B + (\beta + 1)I_{CO} \tag{4.100}$$

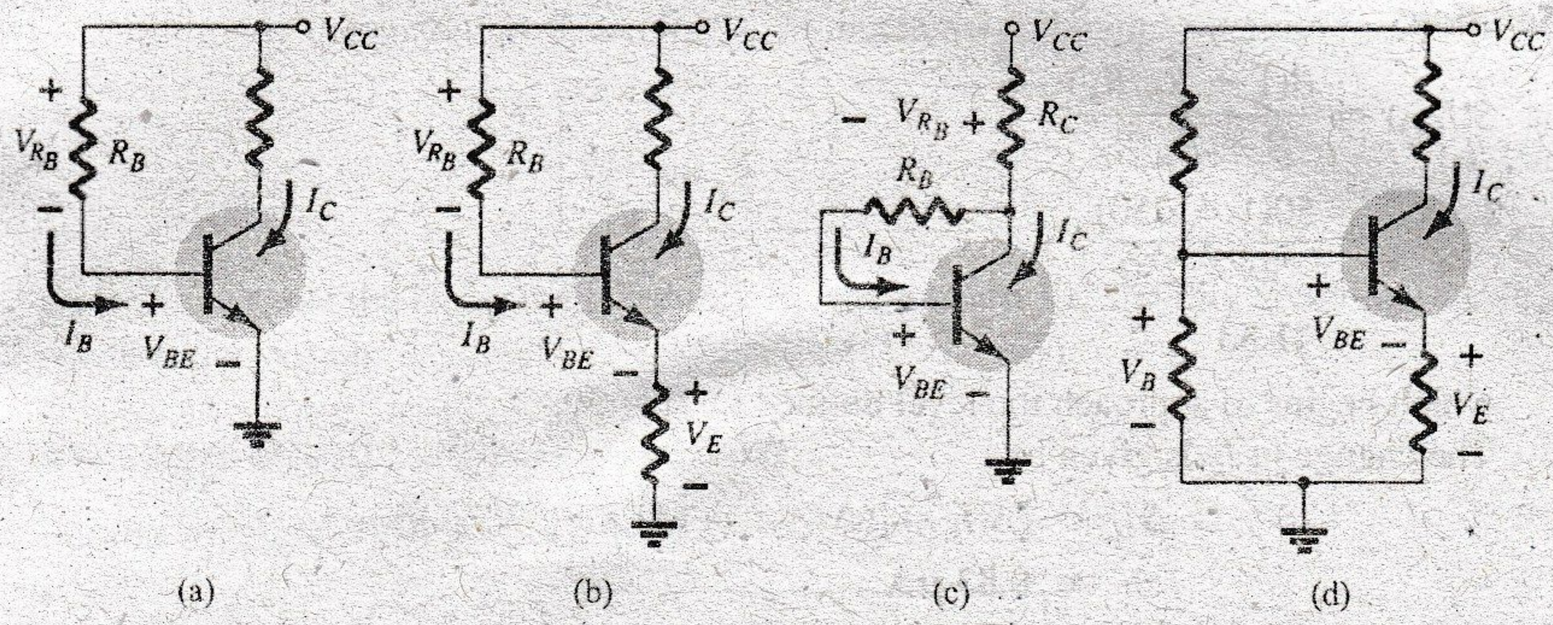


FIG. 4.101
Review of biasing managements and the stability factor $S(I_{CO})$.

If I_C as defined by Eq. (4.93) should increase due to an increase in I_{CO}, there is nothing in the equation for I_B that would attempt to offset this undesirable increase in current level (assuming V_{BE} remains constant). In other words, the level of I_C would continue to rise with temperature, with I_B maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.101b, however, an increase in I_C due to an increase in I_{CO} will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of I_B as determined by the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B} \tag{4.101}$$

A drop in I_B will have the effect of reducing the level of I_C through transistor action and thereby offset the tendency of I_C to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.101c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If I_C should increase due to an increase in temperature, the level of V_{R_C} will increase in the equation

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C} \uparrow}{R_B} \tag{4.102}$$

and the level of I_B will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant I_C begins to rise, the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.101d. If the condition $\beta R_E \gg 10R_2$ is satisfied, the voltage V_B will remain fairly constant for changing levels of I_C. The base-to-emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If I_C should increase, V_E will increase as described above, and for a constant V_B the voltage V_{BE} will drop. A drop in V_{BE} will establish a lower level of I_B, which will try to offset the increased level of I_C.

EXAMPLE 4.35 Calculate the stability factor and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.2 for the following emitter-bias arrangements:

a. $R_B/R_E = 250$ $(R_B = 250R_E)$.
b. $R_B/R_E = 10$ $(R_B = 10R_E)$.
c. $R_B/R_E = 0.01$ $(R_E = 100R_B)$.

Solution:

a. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E}$$

$$= \frac{50(1 + 250)}{50 + 250}$$

$$\cong \mathbf{41.83}$$

which begins to approach the level defined by $\beta = 50$.

The change in I_C is given by

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (41.83)(19.9\text{ nA})$$

$$\cong \mathbf{0.83\ \mu A}$$

b. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E}$$

$$= \frac{50(1 + 10)}{50 + 10}$$

$$\cong \mathbf{9.17}$$

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (9.17)(19.9\text{ nA})$$

$$\cong \mathbf{0.18\ \mu A}$$

c. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E}$$

$$= \frac{50(1 + 0.01)}{50 + 0.01}$$

$$\cong \mathbf{1.01}$$

which is certainly very close to the level of 1 forecast if $R_B/R_E \ll 1$.

We have

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = 1.01(19.9\text{ nA})$$

$$= \mathbf{20.1\ nA}$$

Example 4.35 reveals how lower and lower levels of I_{CO} for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in I_C is considerably different in a circuit having ideal stability ($S = 1$) from one having a stability factor of 41.83, the change in I_C is not that significant. For example, the amount of change in I_C from a dc bias current set at, say, 2 mA, would be from 2 mA to 2.00083 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of I_{CO} have had a very positive impact on the stability question.

$S(V_{BE})$

The stability factor $S(V_{BE})$ is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

Fixed-Bias Configuration

For the fixed-bias configuration:

$$\boxed{S(V_{BE}) \cong \frac{-\beta}{R_B}} \tag{4.103}$$

Emitter-Bias Configuration

For the emitter-bias configuration:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + R_B/R_E}} \tag{4.104}$$

Substituting the condition $\beta \gg R_B/R_E$ results in the following equation for $S(V_{BE})$:

$$S(V_{BE}) \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E} \tag{4.105}$$

which shows that the larger the resistance R_E, the lower is the stability factor and the more stable is the system.

Voltage-Divider Configuration

For the voltage-divider configuration:

$$S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_{Th}/R_E} \tag{4.106}$$

Feedback-Bias Configuration

For the feedback-bias configuration:

$$S(V_{BE}) = \frac{-\beta/R_C}{\beta + R_B/R_C} \tag{4.107}$$

EXAMPLE 4.36 Determine the stability factor $S(V_{BE})$ and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.2 for the following bias arrangements.

a. Fixed-bias with $R_B = 240\ \text{k}\Omega$ and $\beta = 100$.
b. Emitter-bias with $R_B = 240\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, and $\beta = 100$.
c. Emitter-bias with $R_B = 47\ \text{k}\Omega$, $R_E = 4.7\ \text{k}\Omega$, and $\beta = 100$.

Solution:

a. Eq. (4.103): $$S(V_{BE}) = -\frac{\beta}{R_B} = -\frac{100}{240\ \text{k}\Omega} = \mathbf{-0.417 \times 10^{-3}}$$

and
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE}) = (-0.417 \times 10^{-3})(0.48\ \text{V} - 0.65\ \text{V}) = (-0.417 \times 10^{-3})(-0.17\ \text{V}) = \mathbf{70.9\ \mu A}$$

b. In this case, $\beta = 100$ and $R_B/R_E = 240$. The condition $\beta \gg R_B/R_E$ is not satisfied, negating the use of Eq. (4.105) and requiring the use of Eq. (4.104).

Eq. (4.104): $$S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_B/R_E} = \frac{-(100)/(1\ \text{k}\Omega)}{100 + (240\ \text{k}\Omega/1\ \text{k}\Omega)} = \frac{-0.1}{100 + 240} = \mathbf{-0.294 \times 10^{-3}}$$

which is about 30% less than the fixed-bias value due to the additional R_E term in the denominator of the $S(V_{BE})$ equation. We have

$$\Delta I_C = [S(V_{BE})](\Delta V_{BE}) = (-0.294 \times 10^{-3})(-0.17\ \text{V}) \cong \mathbf{50\ \mu A}$$

c. In this case,

$$\beta = 100 \gg \frac{R_B}{R_E} = \frac{47\ \text{k}\Omega}{4.7\ \text{k}\Omega} = 10 \quad (\textit{satisfied})$$

Eq. (4.105):
$$S(V_{BE}) = -\frac{1}{R_E}$$
$$= -\frac{1}{4.7\ \text{k}\Omega}$$
$$= \mathbf{-0.212 \times 10^{-3}}$$

and
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$
$$= (-0.212 \times 10^{-3})(-0.17\ \text{V})$$
$$= \mathbf{36.04\ \mu A}$$

In Example 4.36, the increase of 70.9 μA will have some impact on the level of I_{C_Q}. For a situation where $I_{C_Q} = 2$ mA, the resulting collector current increases to a 3.5% increase.

$$I_{C_Q} = 2\,\text{mA} + 70.9\ \mu\text{A}$$
$$= 2.0709\ \text{mA}$$

For the voltage-divider configuration, the level of R_B will be changed to R_{Th} in Eq. (4.104) (as defined by Fig. 4.100). In Example 4.36, the use of $R_B = 47\ \text{k}\Omega$ is a questionable design. However, R_{Th} for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for $S(V_{BE})$ for the feedback network will be similar to that of Eq. (4.104) with R_E replaced by R_C.

$S(\beta)$

The last stability factor to be investigated is that of $S(\beta)$. The mathematical development is more complex than that encountered for $S(I_{CO})$ and $S(V_{BE})$, as suggested by some of the following equations.

Fixed-Bias Configuration

For the fixed-bias configuration

$$\boxed{S(\beta) = \frac{I_{C_1}}{\beta_1}} \qquad \textbf{(4.108)}$$

Emitter-Bias Configuration

For the emitter-bias configuration

$$\boxed{S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(\beta_2 + R_B/R_E)}} \qquad \textbf{(4.109)}$$

The notation I_{C_1} and β_1 is used to define their values under one set of network conditions, whereas the notation β_2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

EXAMPLE 4.37 Determine I_{C_Q} at a temperature of 100°C if $I_{C_Q} = 2$ mA at 25°C for the emitter-bias configuration. Use the transistor described by Table 4.2, where $\beta_1 = 50$ and $\beta_2 = 80$, and a resistance ratio R_B/R_E of 20.

Solution:

Eq. (4.109):
$$S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$
$$= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050}$$
$$= \mathbf{8.32 \times 10^{-6}}$$

and
$$\Delta I_C = [S(\beta)][\Delta\beta]$$
$$= (8.32 \times 10^{-6})(30)$$
$$\cong \mathbf{0.25\ mA}$$

In conclusion, therefore, the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

Voltage-Divider Bias Configuration

For the voltage-divider bias configuration

$$S(\beta) = \frac{I_{C_1}(1 + R_{Th}/R_E)}{\beta_1(\beta_2 + R_{Th}/R_E)} \tag{4.110}$$

Feedback-bias Configuration

For the collector feedback-bias configuration

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + \beta_2 R_C)} \tag{4.111}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation for each configuration

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \tag{4.112}$$

The equation may initially appear quite complex, but note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in I_C from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.78) becomes

$$\Delta I_C = \beta\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta \tag{4.113}$$

after substituting the stability factors as derived in this section. Let us now use Table 4.2 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\Delta I_{CO} = 20\ \text{nA} - 0.1\ \text{nA} = 19.9\ \text{nA}$$
$$\Delta V_{BE} = 0.48\ \text{V} - 0.65\ \text{V} = -0.17\ \text{V} \quad \text{(note the sign)}$$

and
$$\Delta\beta = 80 - 50 = 30$$

Starting with a collector current of 2 mA with an R_B of 240 kΩ, we obtain the resulting change in I_C due to an increase in temperature of 75°C as follows:

$$\Delta I_C = (50)(19.9\ \text{nA}) - \frac{50}{240\ \text{k}\Omega}(-0.17\ \text{V}) + \frac{2\ \text{mA}}{50}(30)$$
$$= 1\ \mu\text{A} + 35.42\ \mu\text{A} + 1200\ \mu\text{A}$$
$$= 1.236\ \text{mA}$$

which is a significant change due primarily to the change in β. The collector current has increased from 2 mA to 3.236 mA, but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration is employed with a ratio $R_{Th}/R_E = 2$ and $R_E = 4.7\ \text{k}\Omega$, then

$$S(I_{CO}) = 2.89, \quad S(V_{BE}) = -0.2 \times 10^{-3}, \quad S(\beta) = 1.445 \times 10^{-6}$$

and
$$\Delta I_C = (2.89)(19.9\text{ nA}) - 0.2 \times 10^{-3}(-0.17\text{ V}) + 1.445 \times 10^{-6}(30)$$
$$= 57.51\text{ nA} + 34\,\mu\text{A} + 43.4\,\mu\text{A}$$
$$= 0.077\text{ mA}$$

The resulting collector current is 2.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case, $S(\beta)$ did not override the other two factors, and the effects of $S(V_{BE})$ and $S(I_{CO})$ were equally important. In fact, at higher temperatures, the effects of $S(I_{CO})$ and $S(V_{BE})$ will be greater than $S(\beta)$ for the device of Table 4.2. For temperatures below 25°C, I_C will decrease with increasingly negative temperature levels.

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques, which continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

> ***General Conclusion:***
>
> ***The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.***

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

4.19 PRACTICAL APPLICATIONS

As with the diodes in Chapter 2, it would be virtually impossible to provide even a surface treatment of the broad areas of application of BJTs. However, a few applications are chosen here to demonstrate how different facets of the characteristics of BJTs are used to perform various functions.

BJT Diode Usage and Protective Capabilities

As you begin to scan complex networks you will often find transistors being used where all three terminals are not connected in the network—particularly the collector lead. In such cases it is most likely being used as a diode rather than a transistor. There are a number of reasons for such use, including the fact that it is cheaper to buy a large number of transistors rather than a smaller bundle and then pay separately for specific diodes. Also, in ICs the manufacturing process may be more direct to make additional transistors that introduce the diode construction sequence. Two examples of its use as a diode appear in Fig. 4.102. In Fig. 4.102a it is being used in a simple diode network. In Fig. 4.102b it is being used to establish a reference level.

Often times you will see a diode connected directly across a device as shown in Fig. 4.103 to simply ensure that the voltage across a device or system with the polarity shown cannot exceed the forward bias voltage of 0.7 V. In the reverse direction if the breakdown strength is sufficiently high it will simply appear as an open circuit. Again, however, only two terminals of the BJT are being employed.

The point to be made is that one should not assume that every BJT transistor in a network is being used for amplification or as a buffer between stages. The number of areas of application for BJTs beyond these areas is quite extensive.

Relay Driver

This application is in some ways a continuation of the discussion introduced for diodes about how the effects of inductive kick can be minimized through proper design. In Fig. 4.104a, a transistor is used to establish the current necessary to energize the relay in the

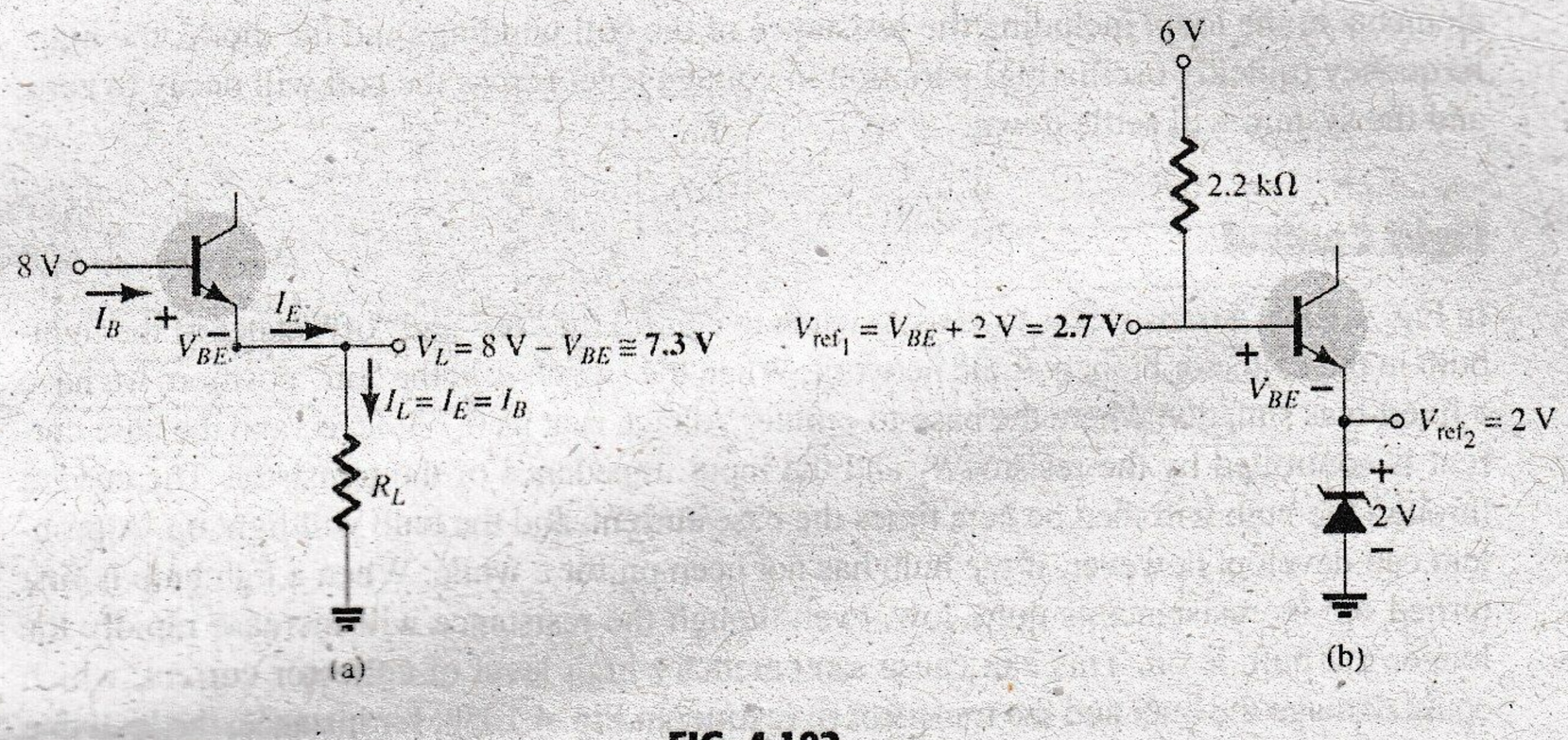


FIG. 4.102

BJT applications as a diode: (a) simple series diode circuit; (b) setting a reference level.

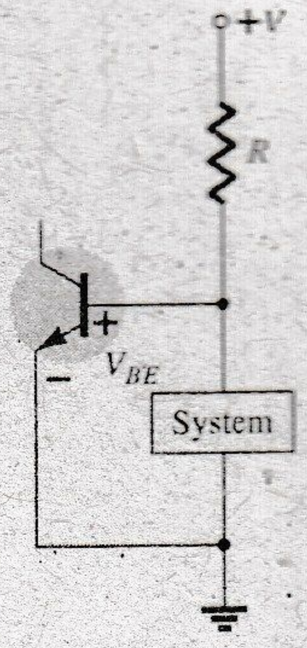


FIG. 4.103

Acting as a protective device.

collector circuit. With no input at the base of the transistor, the base current, collector current, and coil current are essentially 0 A, and the relay sits in the unenergized state (normally open, NO). However, when a positive pulse is applied to the base, the transistor turns on, establishing sufficient current through the coil of the electromagnet to close the relay. Problems can now develop when the signal is removed from the base to turn off the transistor and deenergize the relay. Ideally, the current through the coil and the transistor will quickly drop to zero, the arm of the relay will be released, and the relay will simply remain dormant until the next "on" signal. However, we know from our basic circuit courses that the current through a coil cannot change instantaneously, and, in fact, the more quickly it changes, the greater the induced voltage across the coil as defined by $v_L = L(di_L/dt)$. In this case, the rapidly changing current through the coil will develop a large voltage across the coil with the polarity shown in Fig. 4.104a, which will appear directly across the output of the transistor. The chances are likely that its magnitude will exceed the maximum ratings of the transistor, and the semiconductor device will be permanently damaged. The voltage across the coil will not remain at its highest switching level but will oscillate as shown until its level drops to zero as the system settles down.

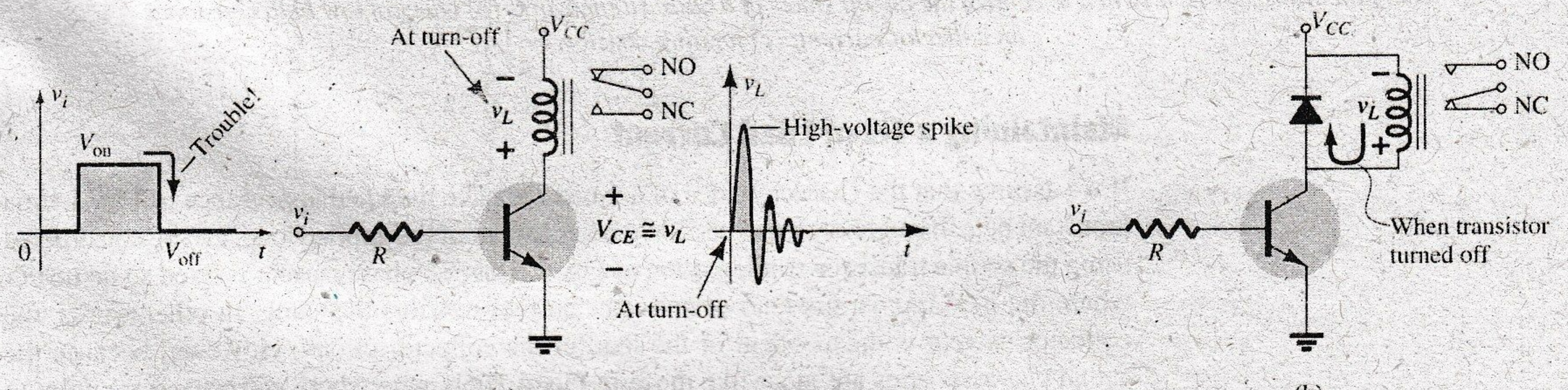


FIG. 4.104

Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.

This destructive action can be subdued by placing a diode across the coil as shown in Fig. 4.104b. During the "on" state of the transistor, the diode is back-biased; it sits like an open circuit and doesn't affect a thing. However, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its "on" state. The current through the inductor established during the "on" state of the transistor can then continue to flow through the diode, eliminating the severe change in current level. Because the inductive current is switched to the diode almost instantaneously after the "off" state is established, the diode must have a current rating to match the current through the inductor and the transistor when in the "on" state. Eventually, because of the resistive

elements in the loop, including the resistance of the coil windings and the diode, the high-frequency (quickly oscillating) variation in voltage level across the coil will decay to zero, and the system will settle down.

Light Control

In Fig. 4.105a, a transistor is used as a switch to control the "on" and "off" states of the lightbulb in the collector branch of the network. When the switch is in the "on" position, we have a fixed-bias situation where the base-to-emitter voltage is at its 0.7-V level, and the base current is controlled by the resistor R_1 and the input impedance of the transistor. The current through the bulb will then be beta times the base current, and the bulb will light up. A problem can develop, however, if the bulb has not been on for a while. When a lightbulb is first turned on, its resistance is quite low, even though the resistance will increase rapidly the longer the bulb is on. This can cause a momentary high level of collector current, which could damage the bulb and the transistor over time. In Fig. 4.105b, for instance, the load line for the same network with a cold and a hot resistance for the bulb is included. Note that even though the base current is set by the base circuit, the intersection with the load line results in a higher current for the cold lightbulb. Any concern about the turn-on level can easily be corrected by inserting an additional small resistor in series with the lightbulb, as shown in Fig. 43.105c, just to ensure a limit on the initial surge in current when the bulb is first turned on.

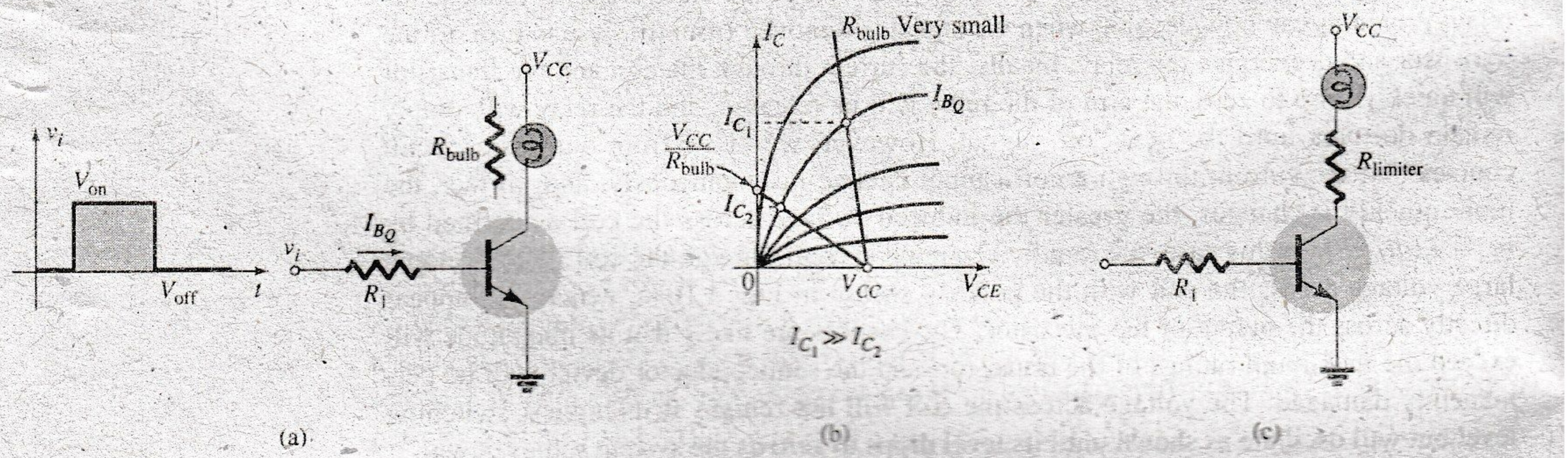


FIG. 4.105

Using the transistor as a switch to control the on–off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

Maintaining a Fixed Load Current

If we assume that the characteristics of a transistor have the ideal appearance of Fig. 4.106a (constant beta throughout) a source, fairly independent of the applied load, can be constructed using the simple transistor configuration of Fig. 4.106b. The base current is fixed so no matter where the load line is, the load or collector current remains the same. In other words, the collector current is independent of the load in the collector circuit. However, because the actual characteristics are more like those in Fig. 4.106b, where beta will vary from point to point, and even though the base current may be fixed by the configuration, the beta will vary from point to point with the load intersection, and $I_C = I_L$ will vary—not characteristic of a good current source. Recall, however, that the voltage-divider configuration resulted in a low level of sensitivity to beta, so perhaps if that biasing arrangement is used, the current source equivalent is closer to reality. In fact, that is the case. If a biasing arrangement such as shown in Fig. 4.107 is employed, the sensitivity to changes in operating point due to varying loads is much less, and the collector current will remain fairly constant for changes in load resistance in the collector branch. In fact, the emitter voltage is determined by

$$V_E = V_B - 0.7\,\text{V}$$

with the collector or load current determined by

$$I_C \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7\,\text{V}}{R_E}$$

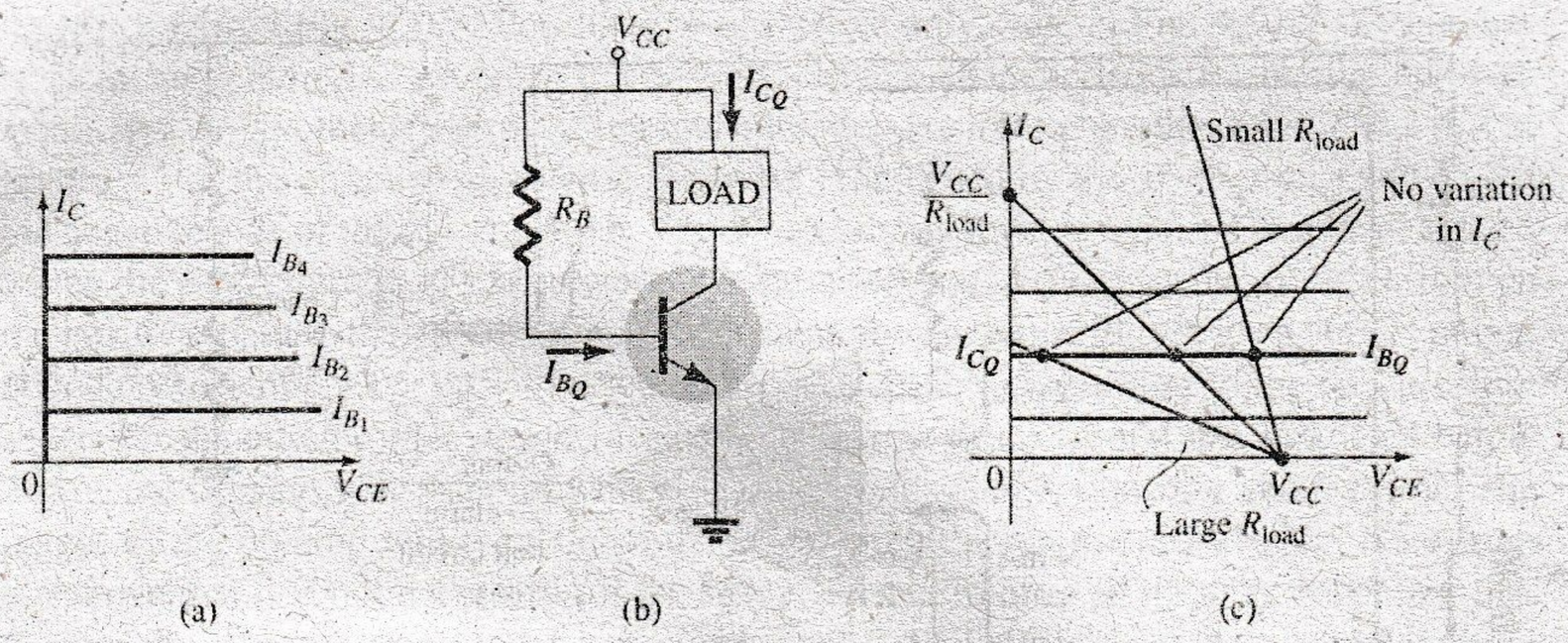


FIG. 4.106

Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why I_C remains constant.

Using Fig. 4.107, we can describe the improved stability by examining the case where I_C may be trying to rise for any number of reasons. The result is that $I_E = I_C$ will also rise and the voltage $V_{R_E} = I_E R_E$ will increase. However, if we assume V_B to be fixed (a good assumption because its level is determined by two fixed resistors and a voltage source), the base-to-emitter voltage $V_{B_E} = V_B - V_{R_E}$ will drop. A drop in V_{BE} will cause I_B and therefore I_C ($= \beta I_B$) to drop. The result is a situation where any tendency for I_C to increase will be met with a network reaction that will work against the change to stabilize the system.

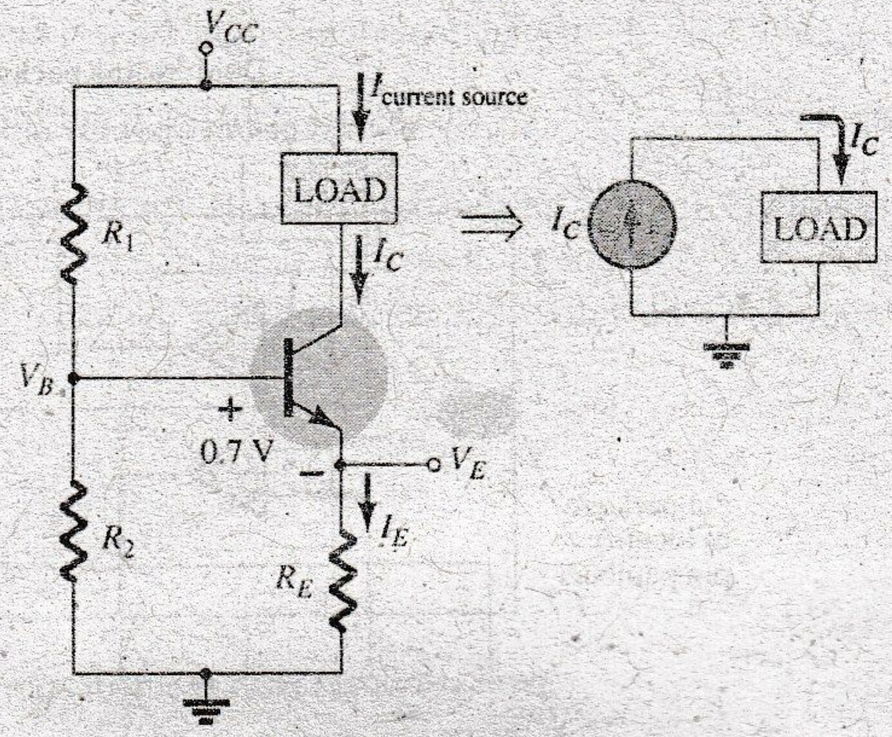


FIG. 4.107

Network establishing a fairly constant current source due to its reduced sensitivity to changes in beta.

Alarm System with a CCS

An alarm system with a constant-current source of the type just introduced appears in Fig. 4.108. Because $\beta R_E = (100)(1\,\text{k}\Omega) = 100\,\text{k}\Omega$ is much greater than R_1, we can use the approximate approach and find the voltage V_{R_1},

$$V_{R_1} = \frac{2\,\text{k}\Omega(16\,\text{V})}{2\,\text{k}\Omega + 4.7\,\text{k}\Omega} = 4.78\,\text{V}$$

and then the voltage across R_E,

$$V_{R_E} = V_{R_1} - 0.7\,\text{V} = 4.78\,\text{V} - 0.7\,\text{V} = 4.08\,\text{V}$$

and finally the emitter and collector current,

$$I_E = \frac{V_{R_E}}{R_E} = \frac{4.08\,\text{V}}{1\,\text{k}\Omega} = 4.08\,\text{mA} \cong 4\,\text{mA} = I_C$$

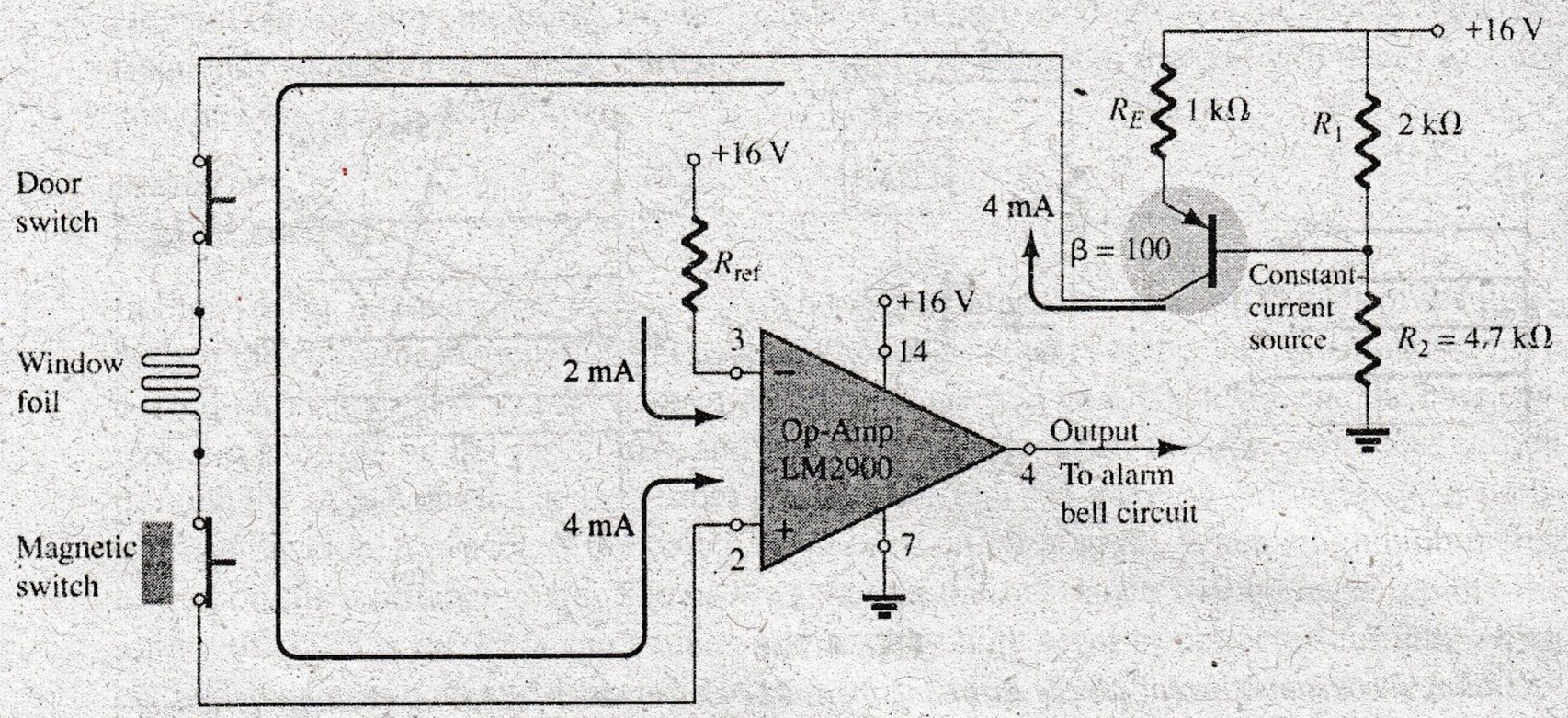
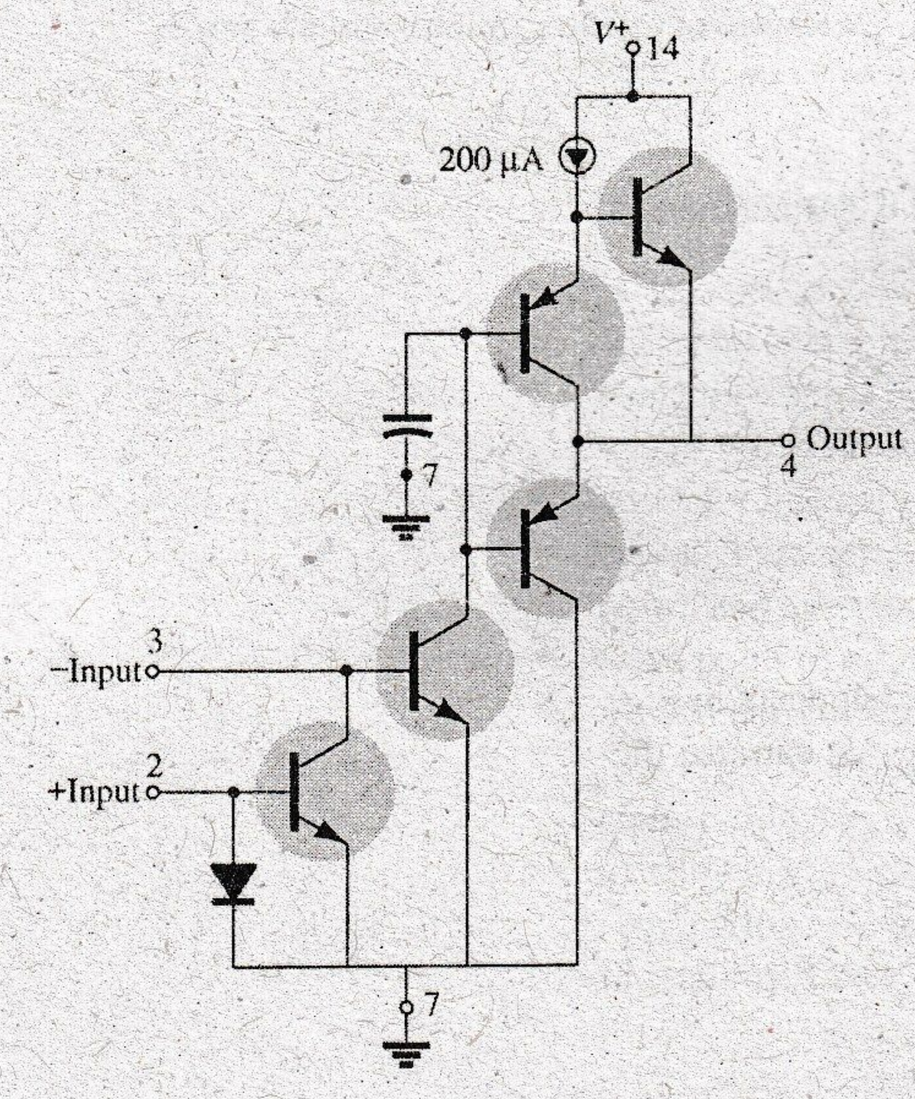


FIG. 4.108

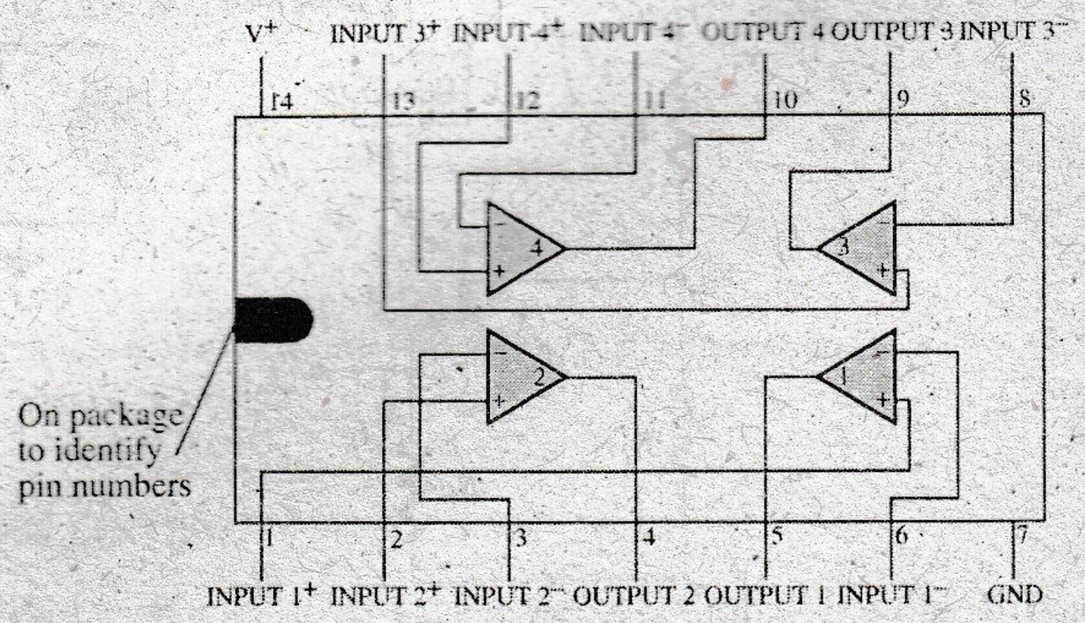
An alarm system with a constant-current source and an op-amp comparator.

Because the collector current is the current through the circuit, the 4-mA current will remain fairly constant for slight variations in network loading. Note that the current passes through a series of sensor elements and finally into an op-amp designed to compare the 4-mA level with the set level of 2 mA. (Although the op-amp may be a new device to you, it will be discussed in detail in Chapter 10—you will not need to know the details of its behavior for this application.)

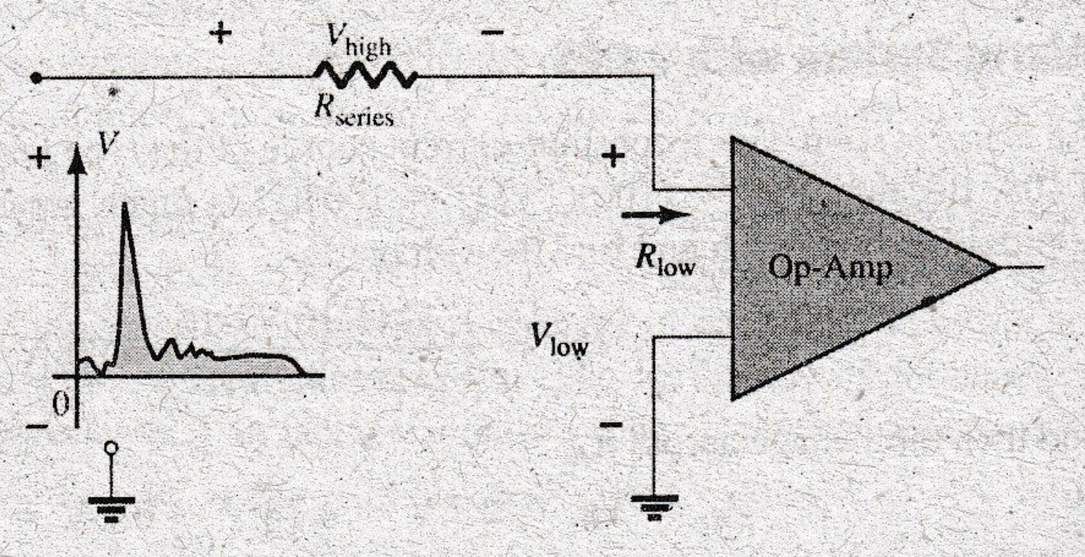
The LM2900 operational amplifier of Fig. 4.108 is one of four found in the dual-in-line integrated circuit package appearing in Fig. 4.109a. Pins 2, 3, 4, 7, and 14 were used



(b)



(a)



(c)

FIG. 4.109

LM2900 operational amplifier: (a) dual-in-line package (DIP); (b) components; (c) impact of low-input impedance.

for the design of Fig. 4.108. For the sake of interest only, note in Fig. 4.109b the number of elements required to establish the desired terminal characteristics for the op-amp—as mentioned earlier, the details of its internal operation are left for another time. The 2 mA at terminal 3 of the op-amp is a *reference* current established by the 16-V source and R_{ref} at the negative side of the op-amp input. The 2-mA current level is required as a level against which the 4-mA current of the network is to be compared. As long as the 4-mA current on the positive input to the op-amp remains constant, the op-amp will provide a "high" output voltage, exceeding 13.5 V, with a typical level of 14.2 V (according to the specification sheets for the op-amp). However, if the sensor current drops from 4 mA to a level below 2 mA, the op-amp will respond with a "low" output voltage, typically about 0.1 V. The output of the op-amp will then signal the alarm circuit about the disturbance. Note from the above that it is not necessary for the sensor current to drop all the way down to 0 mA to signal the alarm circuit. Only a variation around the reference level that appears unusual is required—a good alarm feature.

One very important characteristic of this particular op-amp is the low-input impedance as shown in Fig. 4.109c. This feature is important because one does not want alarm circuits reacting to every voltage spike or turbulence that comes down the line because of some external switching action or outside forces such as lightning. In Fig. 4.109c, for instance, if a high-voltage spike should appear at the input to the series configuration, most of the voltage will appear across the series resistor rather than the op-amp—thus preventing a false output and an activation of the alarm.

Logic Gates

In this application we will expand on the coverage of transistor switching networks in Section 4.15. To review, the collector-to-emitter impedance of a transistor is quite low near or at saturation and large near or at cutoff. For instance, the load line defines *saturation* as the point where the current is quite high and the collector-to-emitter voltage quite low as shown in Fig. 4.110. The resulting resistance, defined by $R_{sat} = \frac{V_{CE_{sat}(low)}}{I_{C_{sat}(high)}}$, is quite low and is often approximated as a short circuit. At *cutoff*, the current is relatively low and the voltage near its maximum value as shown in Fig. 4.110, resulting in a very high impedance between the collector and emitter terminal, which is often approximated by an open circuit.

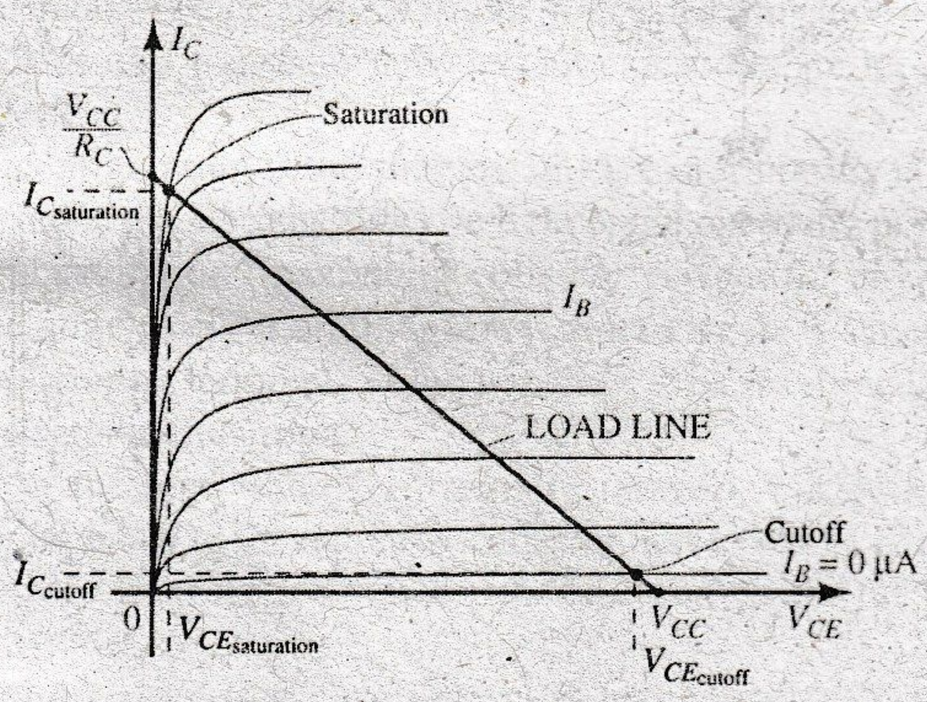
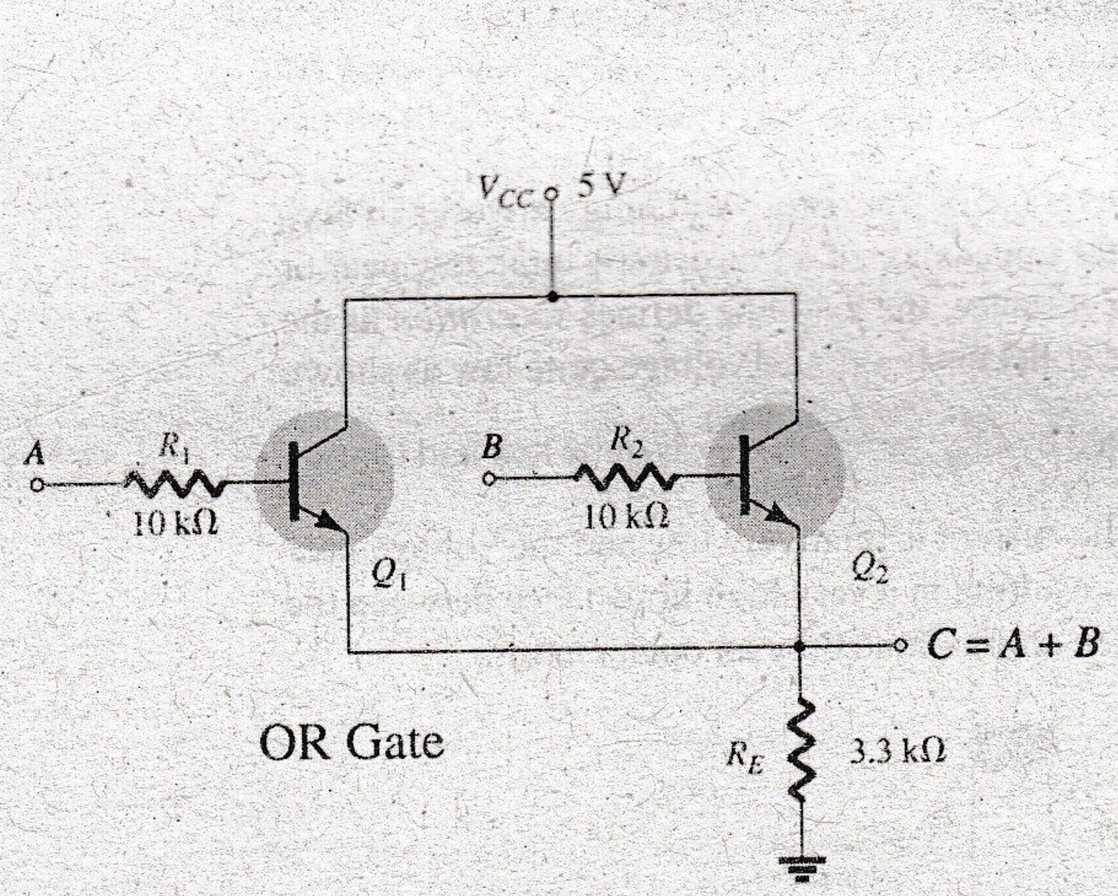


FIG. 4.110
Points of operation for a BJT logic gate.

The above impedance levels established by "on" and "off" transistors make it relatively easy to understand the operation of the logic gates of Fig. 4.111. Because there are two inputs to each gate, there are four possible combinations of voltages at the input to the transistors. A 1, or "on," state is defined by a high voltage at the base terminal to turn the transistor on. A 0, or "off," state is defined by 0 V at the base, ensuring that transistor is off. If both *A* and *B* of the OR gate of Fig. 4.111a have a low or 0-V input, both transistors are off (cutoff), and the impedance between the collector and the emitter of each transistor can be approximated by an open circuit. Mentally replacing both transistors by open circuits

between the collector and the emitter will remove any connection between the applied bias of 5 V and the output. The result is zero current through each transistor and through the 3.3-kΩ resistor. The output voltage is therefore 0 V, or "low"—a 0 state. On the other hand, if transistor Q_1 is on and Q_2 is off due to a positive voltage at the base of Q_1 and 0 V at the base of Q_2, then the short-circuit equivalent between the collector and emitter for transistor Q_1 can be applied, and the voltage at the output is 5 V, or "high"—a 1 state. Finally, if both transistors are turned on by a positive voltage applied to the base of each, they will both ensure that the output voltage is 5 V, or "high"—a 1 state. The operation of the OR gate is properly defined: an output if either input terminal has applied turn-on voltage or if both are in the "on" state. A 0 state exists only if both do not have a 1 state at the input terminals.

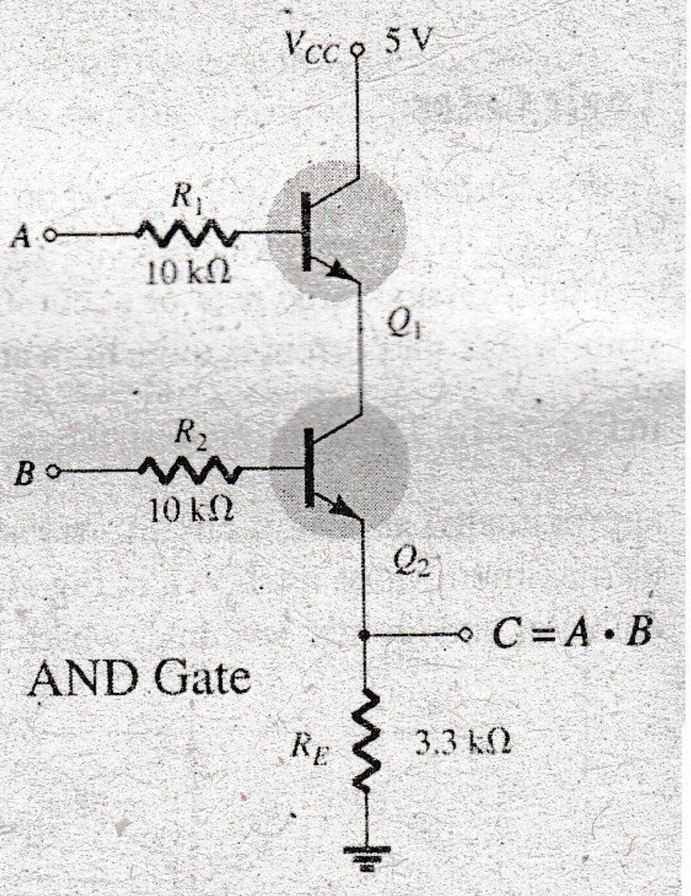
The AND gate of Fig. 4.111b requires that the output be high only if both inputs have a turn-on voltage applied. If both are in the "on" state, a short-circuit equivalent can be used for the connection between the collector and the emitter of each transistor, providing a direct path from the applied 5-V source to the output—thereby establishing a high, or 1, state at the output terminal. If one or both transistors are off due to 0 V at the input terminal, an open circuit is placed in series with the path from the 5-V supply voltage to the output, and the output voltage is 0 V, or an "off" state.



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

1 = high
0 = low

(a)



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(b)

FIG. 4.111
BJT logic gates: (a) OR; (b) AND.

Voltage Level Indicator

The last application to be introduced in this section, the voltage level indicator, includes three of the elements introduced thus far: the transistor, the Zener diode, and the LED. The voltage level indicator is a relatively simple network using a green LED to indicate when the source voltage is close to its monitoring level of 9 V. In Fig. 4.112 the potentiometer is set to establish 5.4 V at the point indicated. The result is sufficient voltage to turn on both

the 4.7-V Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED.

Once the potentiometer is set, the LED will emit its green light as long as the supply voltage is near 9 V. However, if the terminal voltage of the 9-V battery should decrease, the voltage set up by the voltage-divider network may drop to 5 V from 5.4 V. At 5 V there is insufficient voltage to turn on both the Zener and the transistor, and the transistor will be in the "off" state. The LED will immediately turn off, revealing that the supply voltage has dropped below 9 V or that the power source has been disconnected.

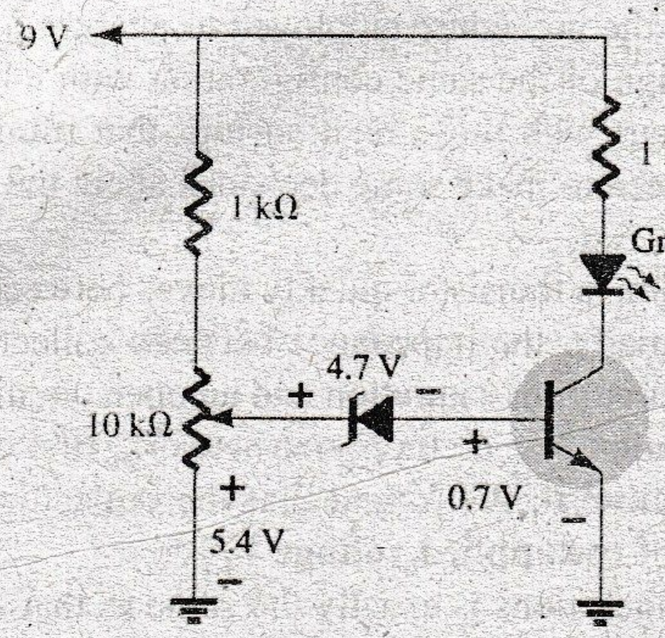


FIG. 4.112
Voltage level indicator.

4.20 SUMMARY

Important Conclusions and Concepts

1. No matter what type of configuration a transistor is used in, the basic relationships between the currents are **always the same**, and the base-to-emitter voltage is the **threshold value** if the transistor is in the "on" state.
2. The operating point defines where the transistor will operate on its characteristic curves under **dc conditions**. For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.
3. For most configurations the dc analysis begins with a determination of the **base current**.
4. For the dc analysis of a transistor network, all capacitors are replaced by an **open-circuit equivalent**.
5. The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable due its **sensitivity to beta** at the operating point.
6. Determining the saturation (maximum) collector current for any configuration can usually be done quite easily if an **imaginary short circuit** is superimposed between the collector and emitter terminals of the transistor. The resulting current through the short is then the saturation current.
7. The equation for the load line of a transistor network can be found by applying **Kirchhoff's voltage law** to the output or collector network. The Q-point is then determined by finding the **intersection** between the base current and the load line drawn on the device characteristics.
8. The emitter-stabilized biasing arrangement is less sensitive to changes in beta—providing more stability for the network. Keep in mind, however, that any resistance in the emitter leg is "seen" at the base of the transistor as a much **larger resistor**, a fact that will reduce the base current of the configuration.
9. The voltage-divider bias configuration is probably the most common of all the configurations. Its popularity is due primarily to its **low sensitivity** to changes in beta from one transistor to another of the same lot (with the same transistor label). The exact analysis can be applied to any configuration, but the approximate one can be applied only if the reflected emitter resistance as seen at the base **is much larger** than the lower resistor of the voltage-divider bias arrangement connected to the base of the transistor.

10. When analyzing the dc bias with a voltage feedback configuration, be sure to remember that ***both*** the emitter resistor and the collector resistor are reflected back to the base circuit by beta. The least sensitivity to beta is obtained when the reflected resistance is much larger than the feedback resistor between the base and the collector.
11. For the common-base configuration the **emitter current is normally determined first** due to the presence of the base-to-emitter junction in the same loop. Then the fact that the emitter and the collector currents are essentially of the same magnitude is employed.
12. A clear understanding of the procedure employed to analyze a dc transistor network will usually permit a design of the same configuration with a minimum of difficulty and confusion. Simply start with those relationships that **minimize the number of unknowns** and then proceed to make some decisions about the unknown elements of the network.
13. In a switching configuration, a transistor quickly moves between **saturation and cutoff, or vice versa**. Essentially, the impedance between collector and emitter can be approximated as a short circuit for saturation and an open circuit for cutoff.
14. When checking the operation of a dc transistor network, first check that the base-to-emitter voltage is very close to **0.7 V** and that the collector-to-emitter voltage is between **25% and 75% of the applied voltage V_{CC}**.
15. The analysis of *pnp* configurations is exactly the same as that applied to *npn* transistors with the exception that current directions will **reverse** and voltages will have the **opposite** polarities.
16. Beta is very sensitive to **temperature**, and V_{BE} **decreases** about 2.5 mV (0.0025 V) for each 1° increase in temperature on a Celsius scale. The reverse saturation current typically **doubles** for every 10° increase in Celsius temperature.
17. Keep in mind that networks that are the **most stable** and least sensitive to temperature changes have the **smallest stability factors**.

Equations

$$V_{BE} \cong 0.7\text{ V}, \qquad I_E = (\beta + 1)I_B \cong I_C, \qquad I_C = \beta I_B$$

Fixed bias:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \qquad I_C = \beta I_B$$

Emitter stabilized:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \qquad R_i = (\beta + 1)R_E$$

Voltage-divider bias:

$$\textit{Exact:} \quad R_{\text{Th}} = R_1 \| R_2, \qquad E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

$$\textit{Approximate: Test} \quad \beta R_E \geq 10R_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad V_E = V_B - V_{BE}, \qquad I_E = \frac{V_E}{R_E} \cong I_C$$

DC bias with voltage feedback:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}, \qquad I_C' \cong I_C \cong I_E$$

Common base:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}, \qquad I_C \cong I_E$$

Transistor switching networks:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}, \qquad I_B > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}}, \qquad R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}, \qquad t_{\text{on}} = t_r + t_d, \qquad t_{\text{off}} = t_s + t_f$$

Stability factors:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}, \qquad S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}, \qquad S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$S(I_{CO})$:

$$\textit{Fixed bias:} \quad S(I_{CO}) \cong \beta$$

$$\textit{Emitter bias:} \quad S(I_{CO}) = \frac{\beta(1 + R_B/R_E)^*}{\beta + R_B/R_E}$$

*Voltage-divider bias: Change R_B to R_{Th} in above equation.

*Feedback bias: Change R_E to R_C in above equation.

$S(V_{BE})$:

$$\textit{Fixed bias:} \quad S(V_{BE}) = -\frac{\beta}{R_B}$$

$$\textit{Emitter bias:} \quad S(V_{BE}) = \frac{-\beta/R_E{}^\dagger}{\beta + R_B/R_E}$$

†Voltage-divider bias: Change R_B to R_{Th} in above equation.

†Feedback bias: Change R_E to R_C in above equation.

$S(\beta)$:

$$\textit{Fixed bias:} \quad S(\beta) = \frac{I_{C_1}}{\beta_1}$$

$$\textit{Emitter bias:} \quad S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)^\ddagger}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

‡Voltage-divider bias: Change R_B to R_{Th} in above equation.

‡Feedback bias: Change R_E to R_C in above equation.

4.21 COMPUTER ANALYSIS

Cadence OrCAD

Voltage-Divider Configuration The results of Example 4.8 will now be verified using Cadence OrCAD. Using methods described in detail in the previous chapters, we can construct the network of Fig. 4.113. Recall from the previous chapter that the transistor is found under the **EVAL** library, the dc source under the **SOURCE** library, and the resistors under the **ANALOG** library. The capacitor has not been called up earlier but can also be found in the **ANALOG** library. For the transistor, the list of available transistors can be found in the **EVAL** library.

The value of beta is changed to 140 to match Example 4.8 by first clicking on the transistor symbol on the screen. It will then appear boxed in red to reveal it is in an active status. Then proceed with **Edit-PSpice Model**, and the **PSpice Model Editor Demo** dialog box will appear in which **Bf** can be changed to **140**. As you try to leave the dialog box the **Model Editor/16.3** dialog box will appear asking if you want to save the changes in the network library. Once they are saved, the screen will automatically return with beta set at its new value.

The analysis can then proceed by selecting the **New simulation profile** key (looks like a printout with an asterisk in the top left corner) to obtain the **New Simulation** dialog box. Insert Fig. 4.113 and select **Create**. The **Simulation Settings** dialog box will appear in which **Bias Point** is selected under the **Analysis Type** heading. An **OK**, and the system is ready for simulation.

Proceed by selecting the **Run PSpice** key (white arrow in green background) or the sequence **PSpice–Run**. The bias voltages will appear as shown in Fig. 4.113 if the **V** option selected. The collector-to-emitter voltage is 13.19 V − 1.333 V = 11.857 V versus 12.22 V of Example 4.8. The difference is primarily due to the fact that we are using an actual transistor whose parameters are very sensitive to the operating conditions. Also recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

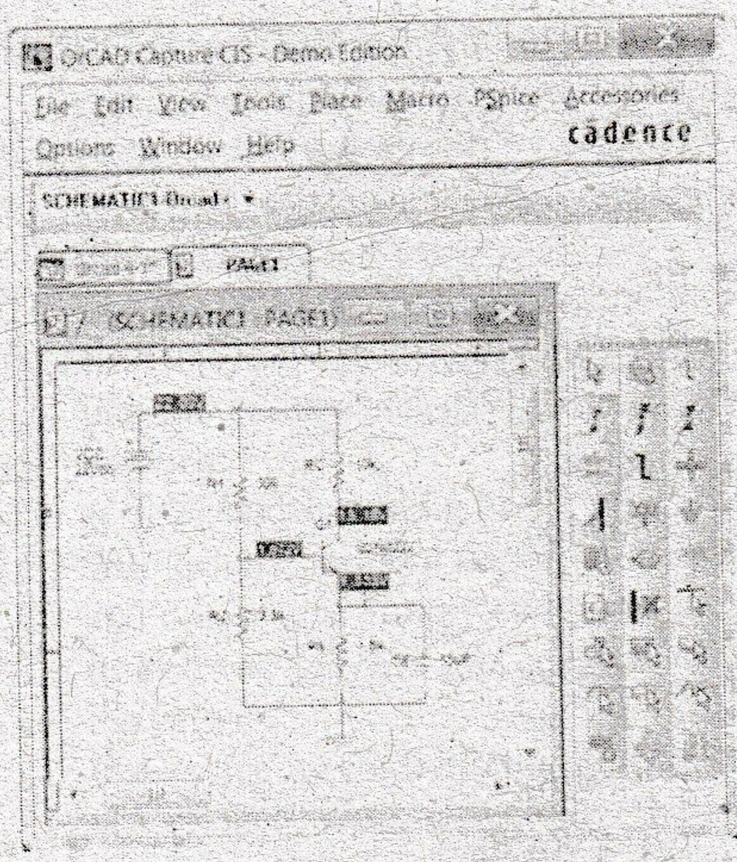


FIG. 4.113
Applying PSpice Windows to the voltage-divider configuration of Example 4.8.

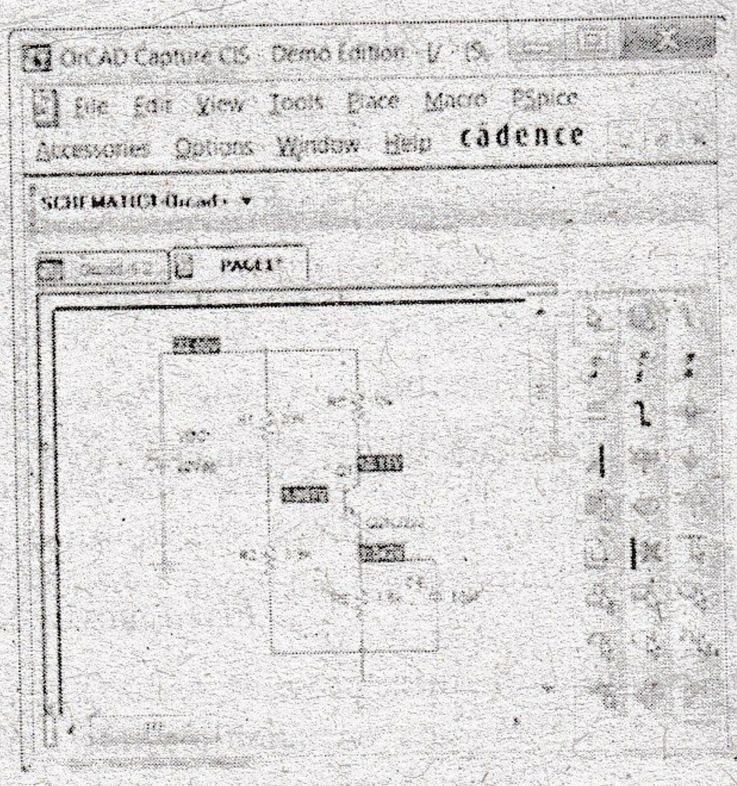


FIG. 4.114
Response obtained after changing β from 140 to 255.9 for the network of Fig. 4.113.

Because the voltage-divider network has a low sensitivity to changes in beta, let us return to the transistor specifications and replace beta by the default value of 255.9 and see how the results change. The result is the printout of Fig. 4.114, with voltage levels very close to those obtained in Fig. 4.113.

Note the distinct advantage of having the network set up in memory. Any parameter can now be changed and a new solution obtained almost instantaneously—a wonderful advantage in the design process.

Fixed-Bias Configuration Although the voltage-divider bias network is relatively insensitive to changes in the beta value, the fixed-bias configuration is very sensitive to beta variations. This can be demonstrated by setting up the fixed-bias configuration of Example 4.1 using a beta of 50 for the first run. The results of Fig. 4.115 demonstrate that the design is a fairly good one. The collector or collector-to-emitter voltage is appropriate for the applied source. The resulting base and collector currents are fairly common for a good design.

However, if we now go back to the transistor specifications and change beta back to the default value of 255.9, we obtain the results of Fig. 4.116. The collector voltage is now only 0.113 V at a current of 5.4 mA—a terrible operating point. Any applied ac signal would be severely truncated due to the low collector voltage.

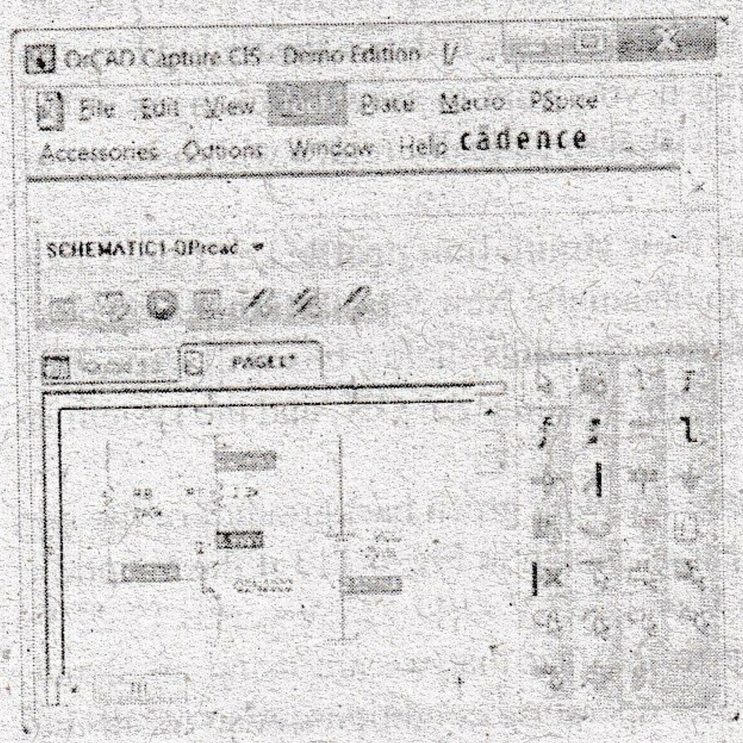


FIG. 4.115
Fixed-bias configuration with a β of 50.

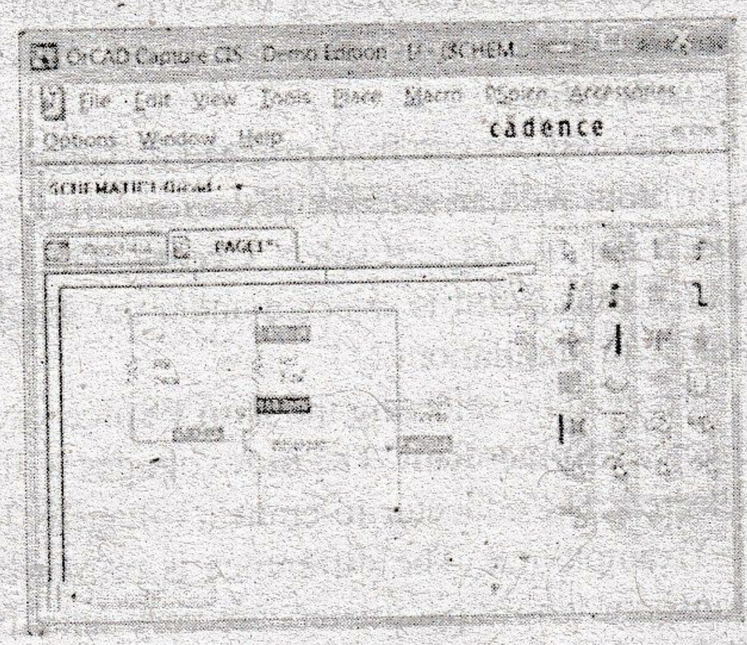


FIG. 4.116
Network of Fig. 4.115 with a β of 255.9.

Clearly, therefore, from the preceding analysis, the voltage-divider configuration is the preferred design if there is any concern about beta variations.

Multisim

Multisim will now be applied to the fixed-bias network of Example 4.4 to provide an opportunity to review the transistor options internal to the software package and to compare results with the handwritten approximate solution.

All the components of Fig. 4.117 except the transistor can be entered using the procedure described in Chapter 2. Transistors are available through the **Transistor** key pad, which is the fourth option down on the **Component** toolbar: When it is selected, the **Select a Component** dialog box will appear, from which **BJT_NPN** is chosen. The result is a **Component** list, from which **2N2222A** can be selected. An **OK**, and the transistor will appear on the screen with the labels **Q1** and **2N2222A**. The label **Bf = 50** can be added by first selecting **Place** in the top toolbar followed by the **Text** option. Place the resulting marker in the area you want to place the text and click once more. The result is a blank space with a blinking marker for where the text will appear when entered. When finished, a second double-click, and the label is set. To move the label to the position shown in Fig. 4.117, simply click on the label to place the four small squares around the device. Then click it once more and drag it to the desired position. Release the clicker, and it is in place. Another click, and the four small markers will disappear.

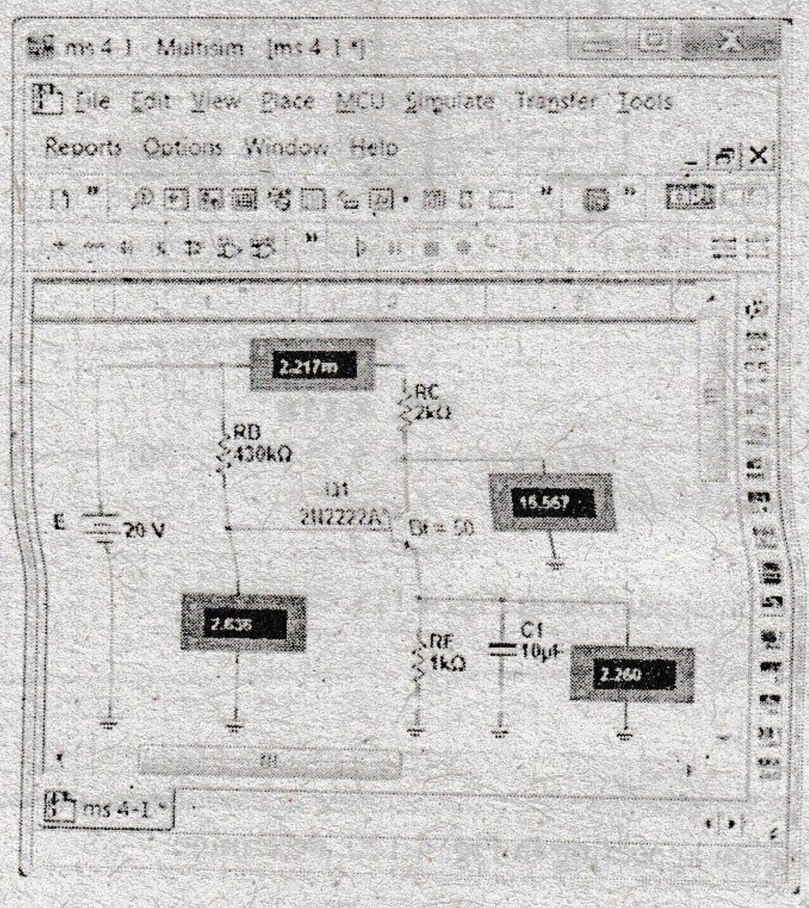


FIG. 4.117
Verifying the results of Example 4.4 using Multisim.

Even though the label may say **Bf = 50**, the transistor will still have the default parameters stored in memory. To change the parameters, the first step is to click on the device to establish the device boundaries. Then select **Edit**, followed by **Properties**, to obtain the **BJT_NPN** dialog box. If it is not already present, select **Value** and then **Edit Model**. The result will be the **Edit Model** dialog box in which β and I_s can be set to 50 and 1 nA, respectively. Then choose **Change Part Model** to obtain the **BJT_NPN** dialog box again and select **OK**. The transistor symbol on the screen will now have an asterisk to indicate that the default parameters have been modified. One more click to remove the four markers, and the transistor is set with its new parameters.

The indicators appearing in Fig. 4.117 were set as described in the previous chapter.

Finally, the network must be simulated using one of the methods described in Chapter 2. For this example the switch was set to the **1** position and then back to the **0** position after the Indicator values stabilized. The relatively low levels of current were partially responsible for the low level of this voltage.

The results are a close match with those of Example 4.4 with $I_C = 2.217$ mA, $V_B = 2.636$ V, $V_C = 15.557$ V, and $V_E = 2.26$ V.

The relatively few comments required here to permit the analysis of transistor networks is a clear indication that the breadth of analysis using Multisim can be expanded dramatically without having to learn a whole new set of rules—a very welcome characteristic of most technology software packages.

PROBLEMS

Note: Asterisks indicate more difficult problems.

4.3 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 4.118, determine:
   a. I_{B_Q}.
   b. I_{C_Q}.
   c. V_{CE_Q}.
   d. V_C.
   e. V_B.
   f. V_E.

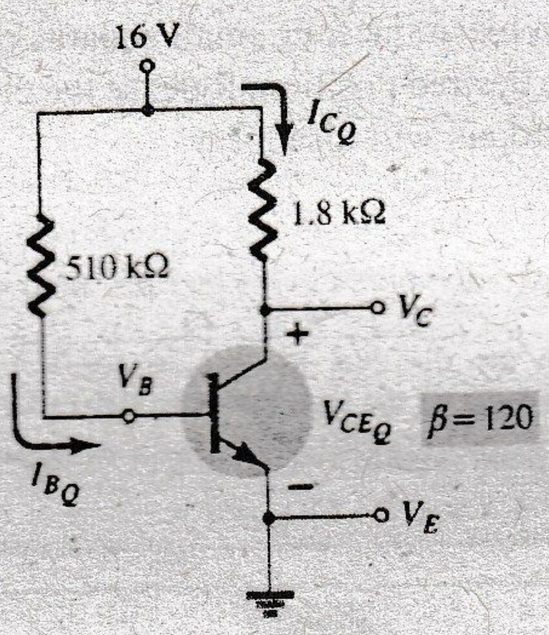


FIG. 4.118
Problems 1, 4, 6, 7, 14, 65, 69, 71, and 75.

2. Given the information appearing in Fig. 4.119, determine:
   a. I_C.
   b. R_C.
   c. R_B.
   d. V_{CE}.
3. Given the information appearing in Fig. 4.120, determine:
   a. I_C.
   b. V_{CC}.
   c. β.
   d. R_B.

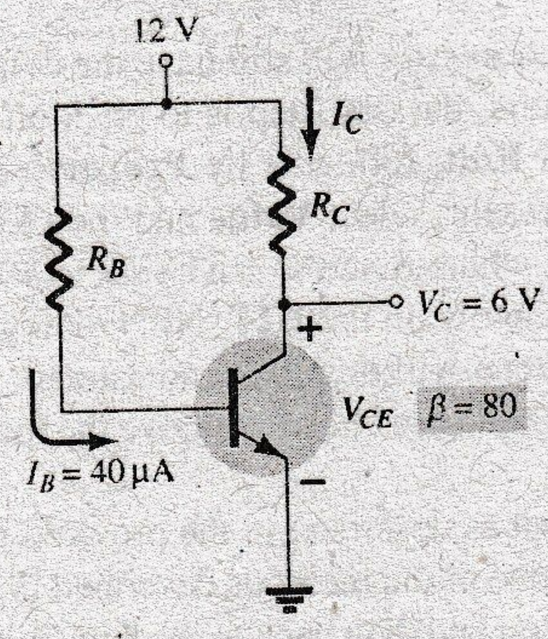


FIG. 4.119
Problem 2.

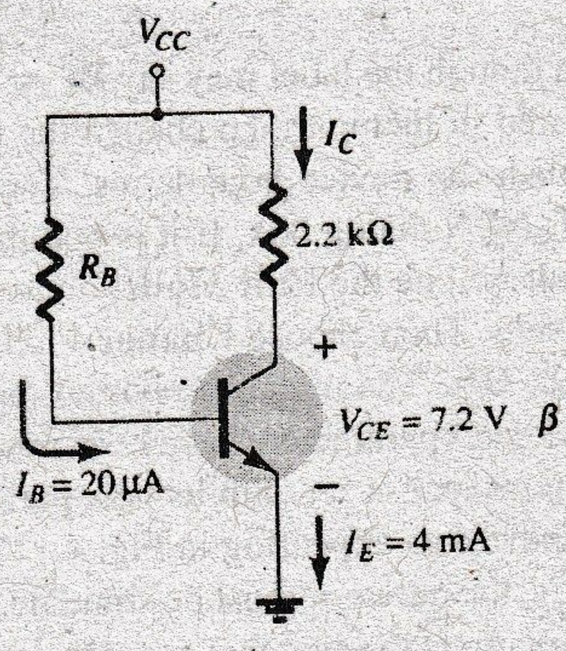


FIG. 4.120
Problem 3.

4. Find the saturation current ($I_{C_{sat}}$) for the fixed-bias configuration of Fig. 4.118.

*5. Given the BJT transistor characteristics of Fig. 4.121:
   a. Draw a load line on the characteristics determined by $E = 21$ V and $R_C = 3\,\text{k}\Omega$ for a fixed-bias configuration.
   b. Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point.
   c. What are the resulting values of I_{C_Q} and V_{CE_Q}?
   d. What is the value of β at the operating point?
   e. What is the value of α defined by the operating point?
   f. What is the saturation current ($I_{C_{sat}}$) for the design?
   g. Sketch the resulting fixed-bias configuration.
   h. What is the dc power dissipated by the device at the operating point?
   i. What is the power supplied by V_{CC}?
   j. Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

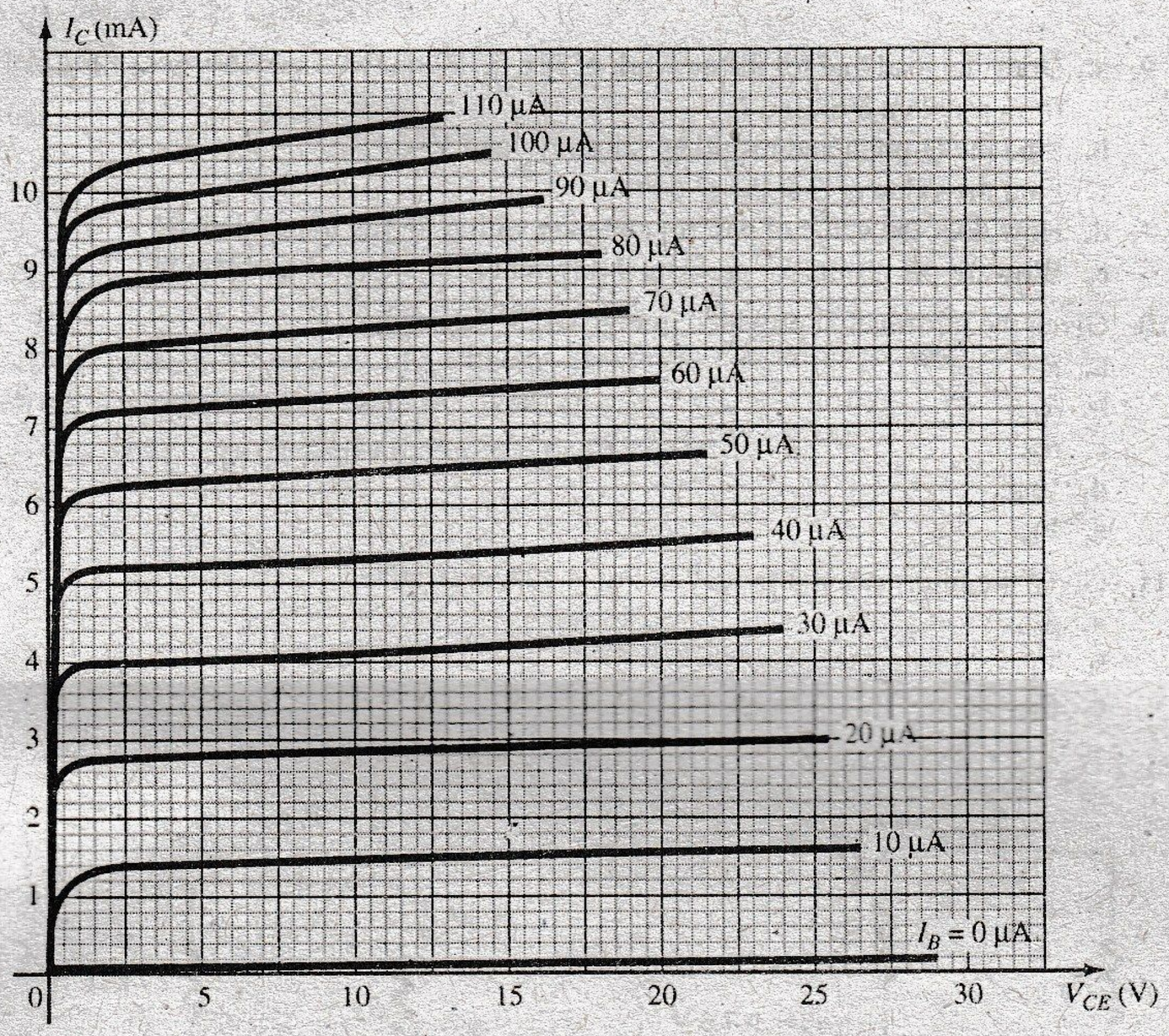


FIG. 4.121
Problems 5, 6, 9, 13, 24, 44, and 57.

6. a. Ignoring the provided value of $\beta_{(120)}$ draw the load line for the network of Fig. 4.118 on the characteristics of Fig. 4.121.
   b. Find the Q-point and the resulting I_{C_Q} and V_{CE_Q}.
   c. What is the beta value at this Q-point?

7. If the base resistor of Fig. 4.118 is increased to 910 kΩ, find the new Q-point and resulting values of I_{C_Q} and V_{CE_Q}.

4.4 Emitter-Bias Configuration

8. For the emitter-stabilized bias circuit of Fig. 4.122, determine:
   a. I_{B_Q}.
   b. I_{C_Q}.
   c. V_{CE_Q}.
   d. V_C.
   e. V_B.
   f. V_E.

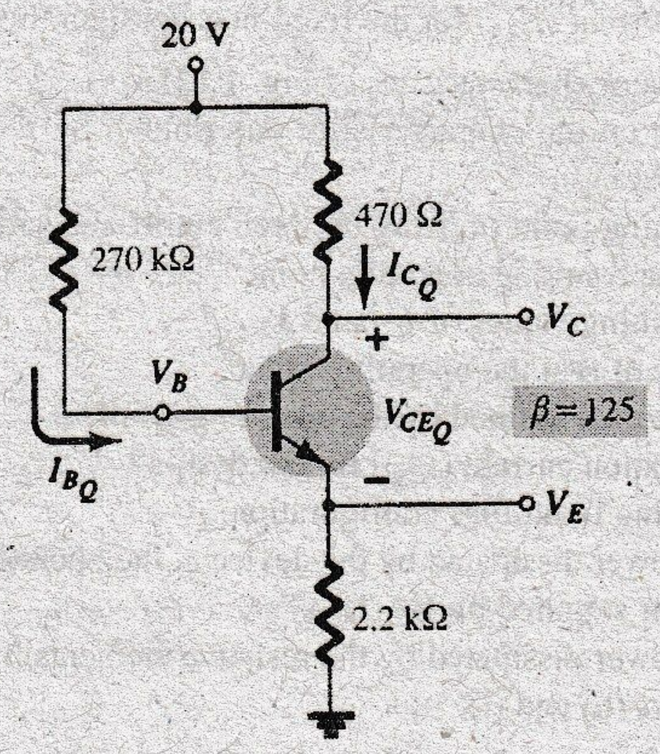


FIG. 4.122
Problems 8, 9, 12, 14, 66, 69, 72, and 76.

9. **a.** Draw the load line for the network of Fig. 4.122 on the characteristics of Fig. 4.121 using β from problem 8 to find I_{B_Q}.
   b. Find the Q-point and resulting values I_{C_Q} and V_{CE_Q}.
   c. Find the value of β at the Q-point.
   d. How does the value of part (c) compare with $\beta = 125$ in problem 8?
   e. Why are the results for problem 9 different from those of problem 8?
10. Given the information provided in Fig. 4.123, determine:
   a. R_C.
   b. R_E.
   c. R_B.
   d. V_{CE}.
   e. V_B.
11. Given the information provided in Fig. 4.124, determine:
   a. β.
   b. V_{CC}.
   c. R_B.

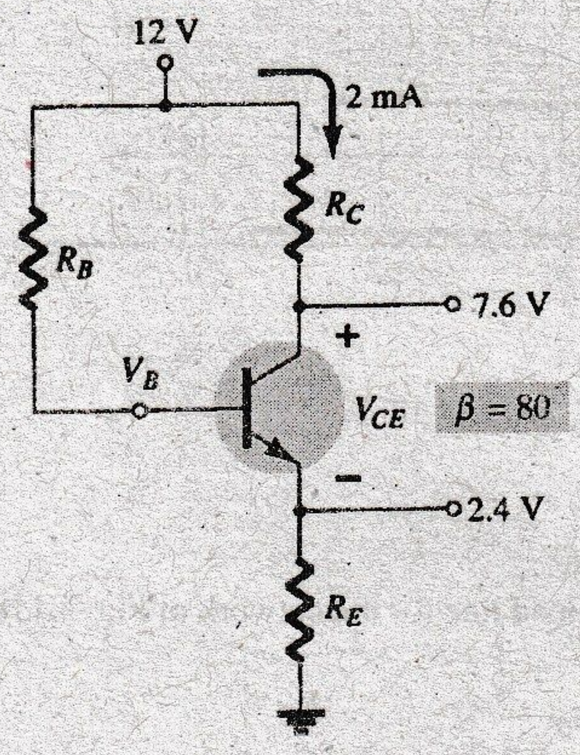


FIG. 4.123
Problem 10.

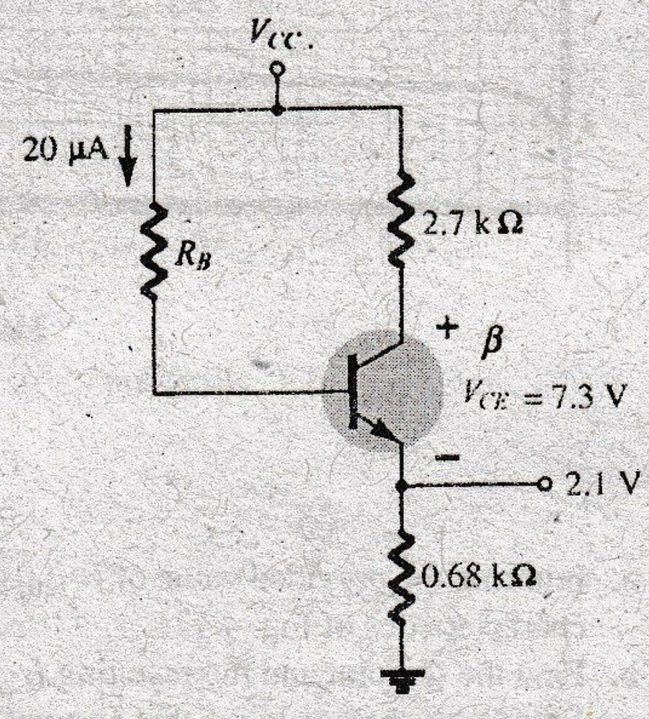


FIG. 4.124
Problem 11.

12. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.122.
*13. Using the characteristics of Fig. 4.121, determine the following for an emitter-bias configuration if a Q-point is defined at $I_{C_Q} = 4$ mA and $V_{CE_Q} = 10$ V.
   a. R_C if $V_{CC} = 24$ V and $R_E = 1.2$ kΩ.
   b. β at the operating point.
   c. R_B.
   d. Power dissipated by the transistor.
   e. Power dissipated by the resistor R_C.

*14. a. Determine I_C and V_{CE} for the network of Fig. 4.118.
b. Change β to 180 and determine the new value of I_C and V_{CE} for the network of Fig. 4.118.
c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}}\right| \times 100\%$$

d. Determine I_C and V_{CE} for the network of Fig. 4.122.
e. Change β to 187.5 and determine the new value of I_C and V_{CE} for the network of Fig. 4.122.
f. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part c})}} - I_{C_{(\text{part d})}}}{I_{C_{(\text{part d})}}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part c})}} - V_{CE_{(\text{part d})}}}{V_{CE_{(\text{part d})}}}\right| \times 100\%$$

g. In each of the above, the magnitude of β was increased 50%. Compare the percentage change in I_C and V_{CE} for each configuration, and comment on which seems to be less sensitive to changes in β.

4.5 Voltage-Divider Bias Configuration

15. For the voltage-divider bias configuration of Fig. 4.125, determine:
a. I_{B_Q}.
b. I_{C_Q}.
c. V_{CE_Q}.
d. V_C.
e. V_E.
f. V_B.

16. a. Repeat problem 15 for $\beta = 140$ using the general approach (not the approximate).
b. What levels are affected the most? Why?

17. Given the information provided in Fig. 4.126, determine:
a. I_C.
b. V_E.
c. V_B.
d. R_1.

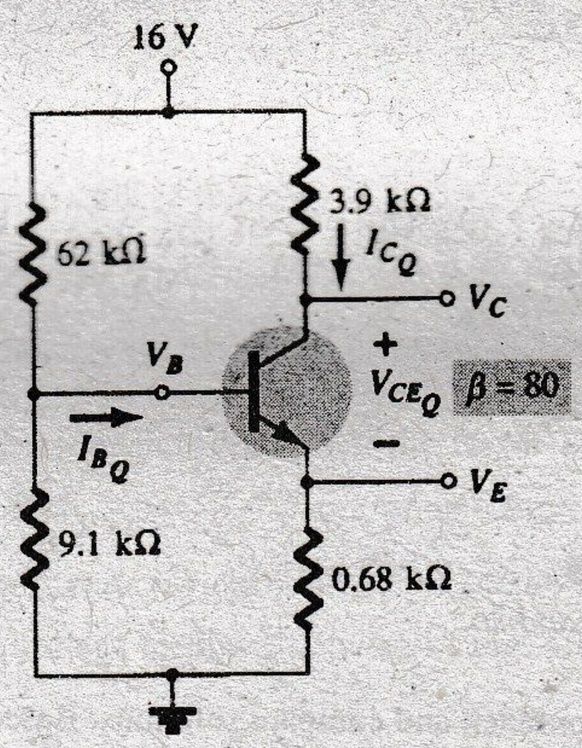


FIG. 4.125
Problems 15, 16, 20, 23, 25, 67, 69, 70, 73, and 77.

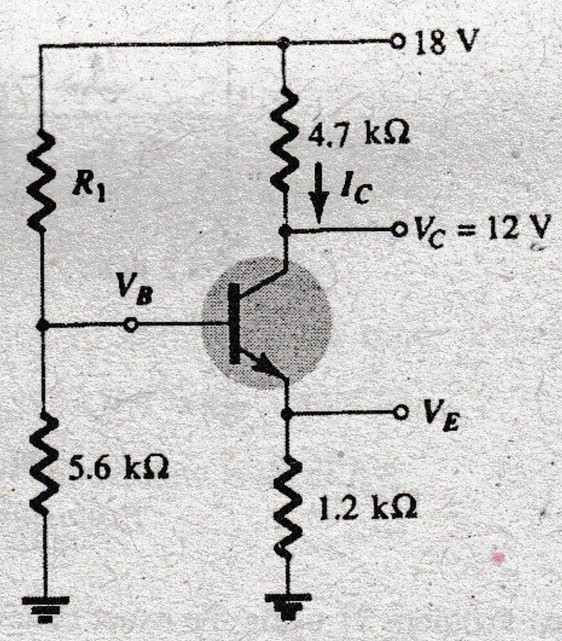


FIG. 4.126
Problems 17 and 19.

18. Given the information appearing in Fig. 4.127, determine:
a. I_C.
b. V_E.
c. V_{CC}.
d. V_{CE}.
e. V_B.
f. R_1.

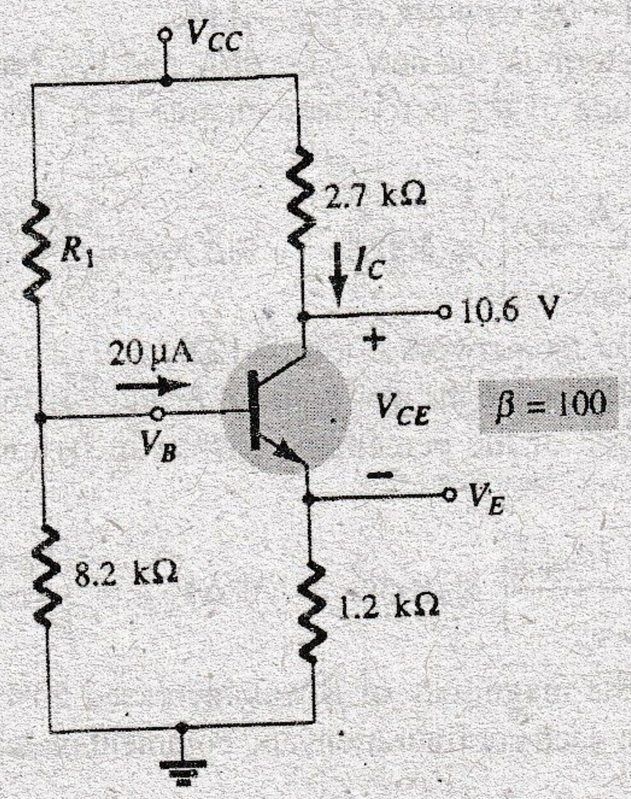


FIG. 4.127
Problem 18.

19. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.125.

20. **a.** Repeat problem 16 with $\beta = 140$ using the approximate approach and compare results.
    b. Is the approximate approach valid?

*21. Determine the following for the voltage-divider configuration of Fig. 4.128 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
    a. I_C.
    b. V_{CE}.
    c. I_B.
    d. V_E.
    e. V_B.

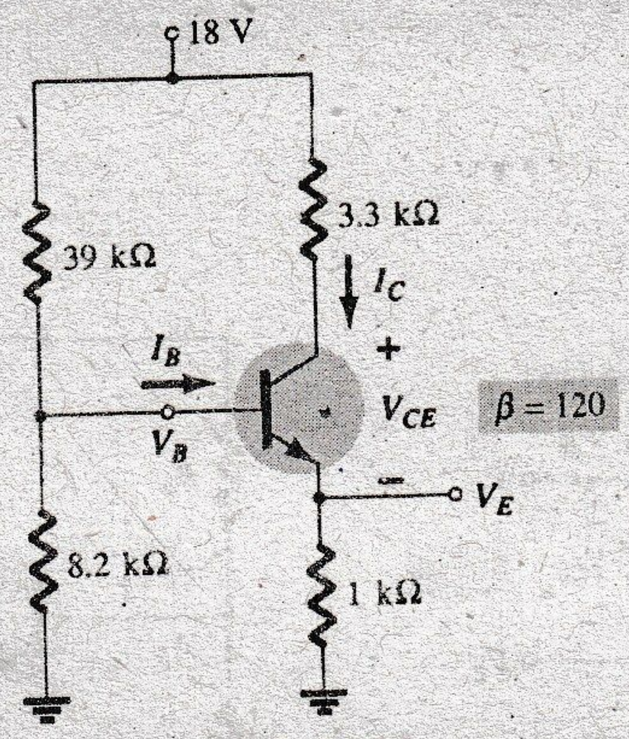


FIG. 4.128
Problems 21, 22, and 26.

*22. Repeat Problem 21 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?

23. **a.** Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} for the network of Problem 15 (Fig. 4.125) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.
    b. Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} using the exact approach.
    c. Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.

*24. **a.** Using the characteristics of Fig. 4.121, determine R_C and R_E for a voltage-divider network having a Q-point of $I_{C_Q} = 5$ mA and $V_{CE_Q} = 8$ V. Use $V_{CC} = 24$ V and $R_C = 3R_E$.
    b. Find V_E.
    c. Determine V_B.
    d. Find R_2 if $R_1 = 24\ \text{k}\Omega$ assuming that $\beta R_E > 10R_2$.
    e. Calculate β at the Q-point.
    f. Test Eq. (4.33), and note whether the assumption of part (d) is correct.

*25. a. Determine I_C and V_{CE} for the network of Fig. 4.125.
b. Change β to 120 (50% increase), and determine the new values of I_C and V_{CE} for the network of Fig. 4.125.
c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}}\right| \times 100\%, \quad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}}\right| \times 100\%$$

d. Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 14.
e. Based on the results of part (d), which configuration is least sensitive to variations in β?

*26. a. Repeat parts (a) through (e) of Problem 25 for the network of Fig. 4.128. Change β to 180 in part (b).
b. What general conclusions can be made about networks in which the condition $\beta R_E > 10R_2$ is satisfied and the quantities I_C and V_{CE} are to be determined in response to a change in β?

4.6 Collector-Feedback Configuration

27. For the collector-feedback configuration of Fig. 4.129, determine:
a. I_B.
b. I_C.
c. V_C.

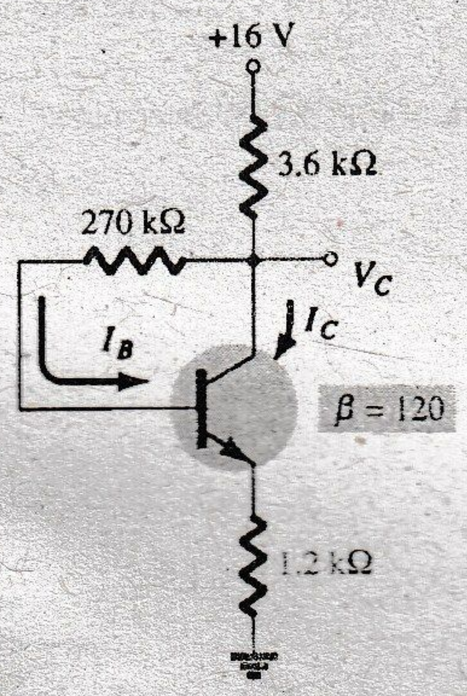


FIG. 4.129
Problems 27, 28, 74, and 78.

28. For the network of problem 27
a. Determine I_{C_Q} using the equation $I_{C_Q} \cong \frac{V'}{R'} = \frac{V_{CC} - V_{BE}}{R_C + R_E}$
b. Compare with the results of problem 27 for I_{C_Q}.
c. Compare R' to $R_{F/\beta}$.
d. Is the statement valid that the larger R′ is compared with $R_{F/\beta}$, the more accurate the equation $I_{C_Q} \cong \frac{V'}{R'}$? Prove using a short derivation for the exact current I_{C_Q}.
e. Repeat parts (a) and (b) for $\beta = 240$ and comment on the new level of I_{C_Q}.

29. For the voltage feedback network of Fig. 4.130, determine:
a. I_C.
b. V_C.
c. V_E.
d. V_{CE}.

30. a. Compare levels of $R' = R_C + R_E$ to $R_{F/\beta}$ for the network of Fig. 4.131.
b. Is the approximation $I_{C_Q} \cong V'/R'$ valid?

*31. a. Determine the levels of I_C and V_{CE} for the network of Fig. 4.131.
b. Change β to 135 (50% increase), and calculate the new levels of I_C and V_{CE}.
c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_C - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}}\right| \times 100\%, \quad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}}\right| \times 100\%$$

d. Compare the results of part (c) with those of Problems 14(c), 14(f), and 25(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in β?

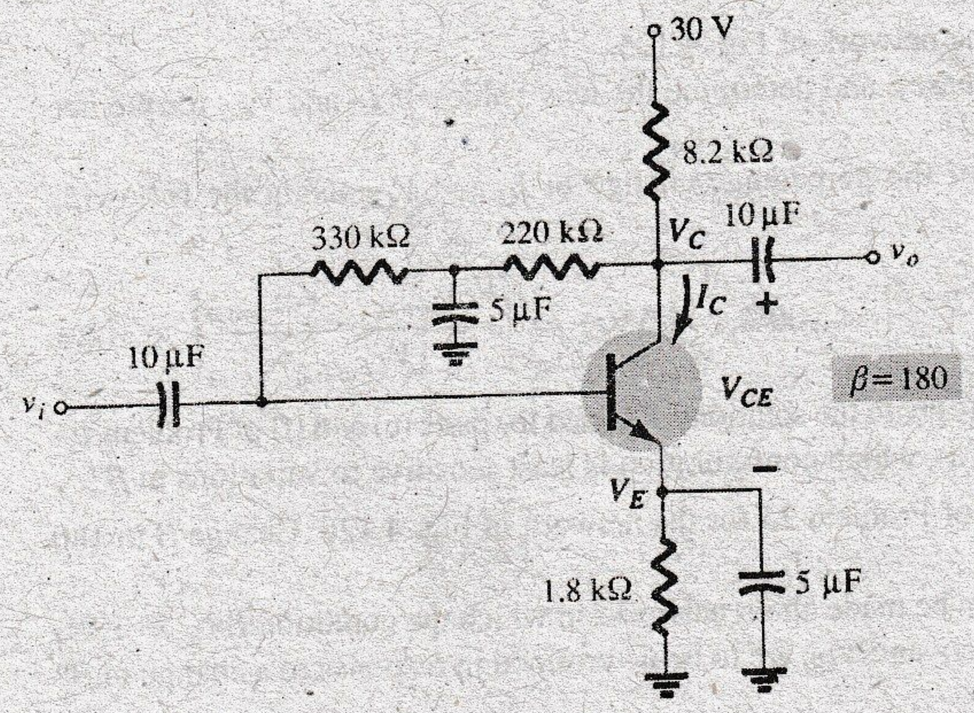


FIG. 4.130
Problems 29 and 30.

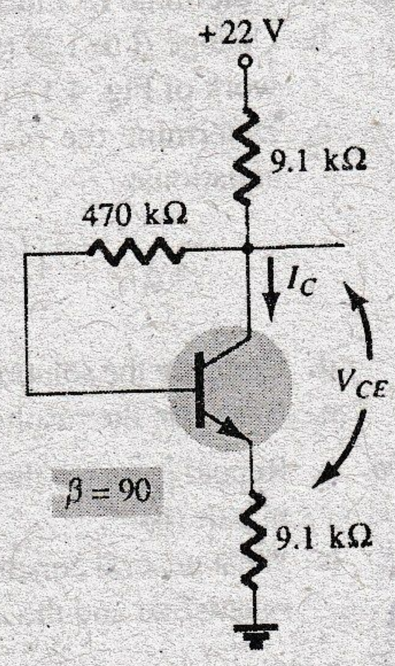


FIG. 4.131
Problems 30 and 31.

32. Determine the range of possible values for V_C for the network of Fig. 4.132 using the 1-MΩ potentiometer.

***33.** Given $V_B = 4$ V for the network of Fig. 4.133, determine:

a. V_E.
b. I_C.
c. V_C.
d. V_{CE}.
e. I_B.
f. β.

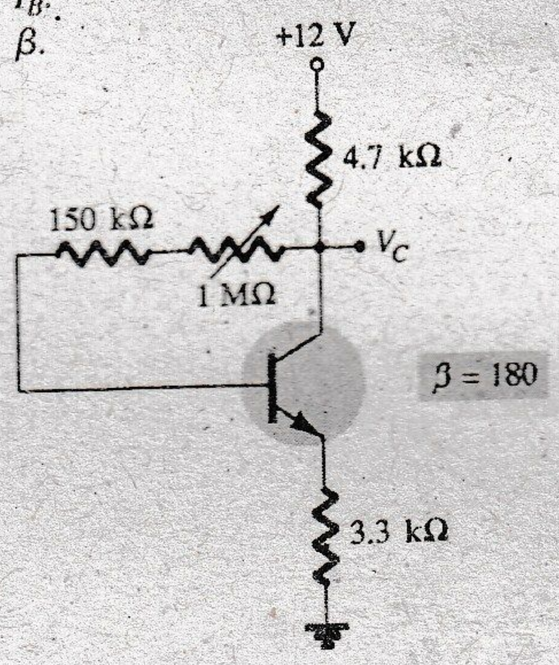


FIG. 4.132
Problem 32.

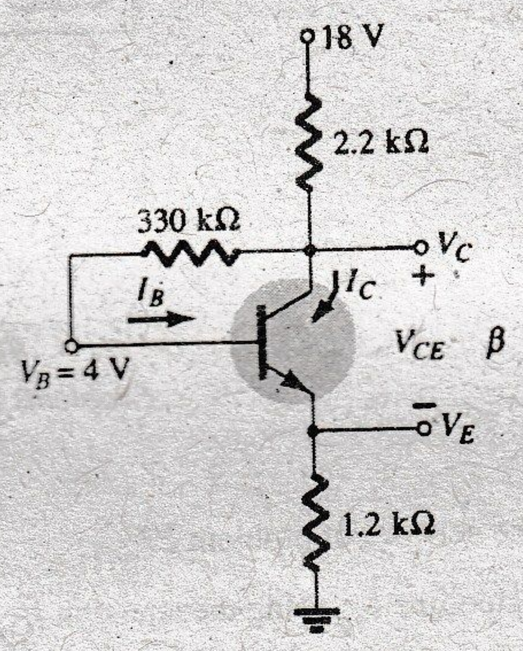


FIG. 4.133
Problem 33.

4.7 Emitter-Follower Configuration

***34.** Determine the level of V_E and I_E for the network of Fig. 4.134.

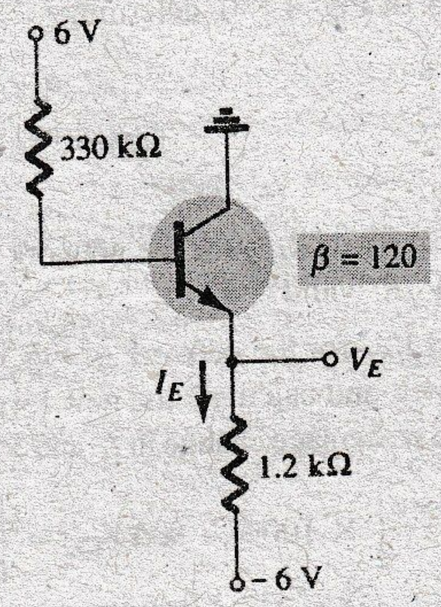


FIG. 4.134
Problem 34.

35. For the emitter follower network of Fig. 4.135
    a. Find I_B, I_C, and I_E.
    b. Determine V_B, V_C, and V_E.
    c. Calculate V_{BC} and V_{CE}.

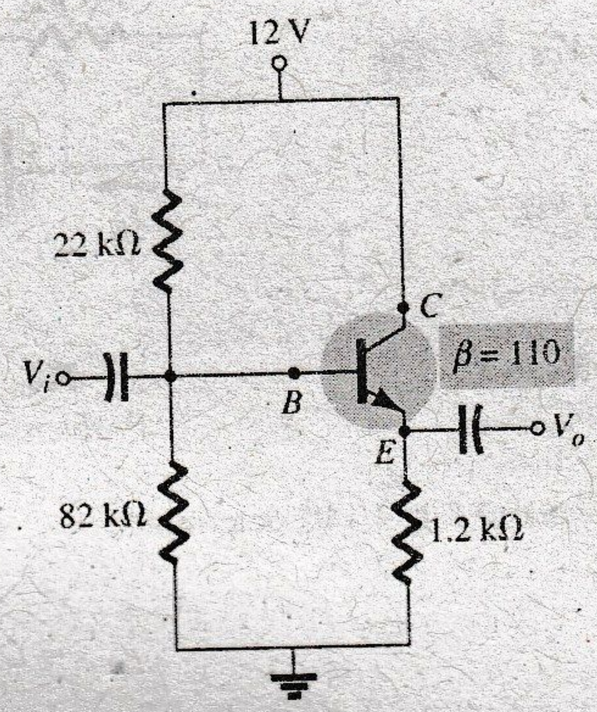


FIG. 4.135
Problem 35.

4.8 Common-Base Configuration

*36. For the network of Fig. 4.136, determine:
    a. I_B.
    b. I_C.
    c. V_{CE}.
    d. V_C.

*37. For the network of Fig. 4.137, determine:
    a. I_E.
    b. V_C.
    c. V_{CE}.

38. For the common-base network of Fig. 4.138
    a. Using the information provided determine the value of R_C.
    b. Find the currents I_B and I_E.
    c. Determine the voltages V_{BC} and V_{CE}.

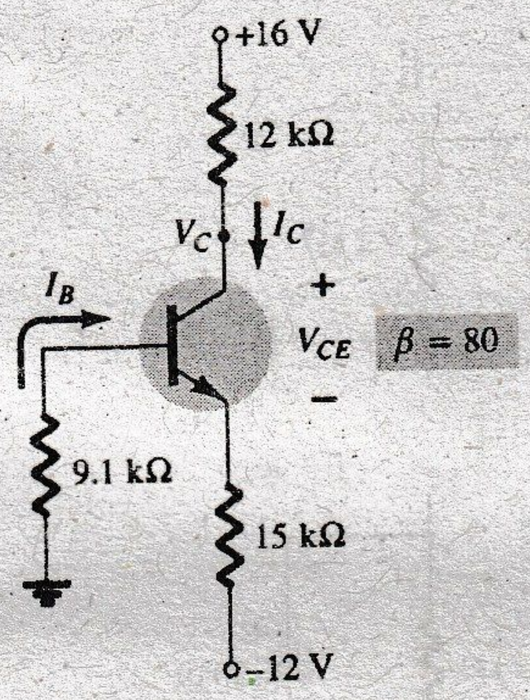


FIG. 4.136
Problem 36.

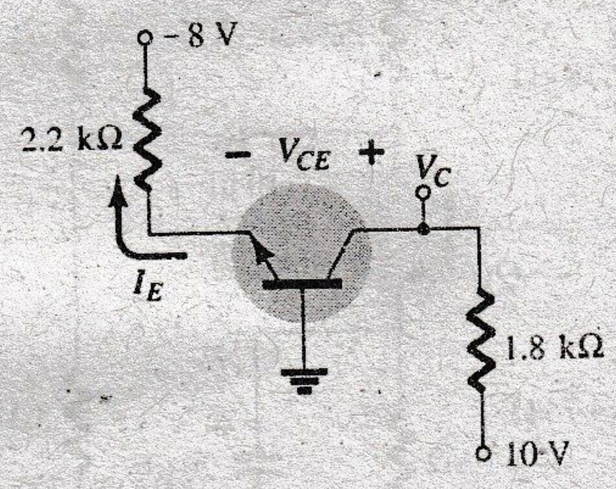


FIG. 4.137
Problem 37.

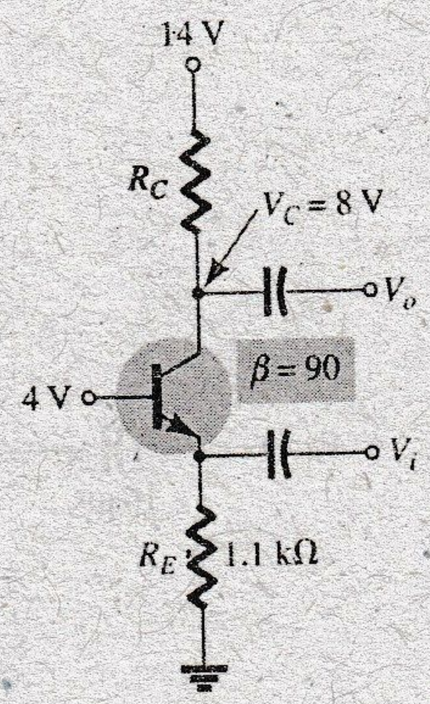


FIG. 4.138
Problem 38.

4.9 Miscellaneous Bias Configurations

*39. For the network of Fig. 4.139, determine:
    a. I_B.
    b. I_C.
    c. V_E.
    d. V_{CE}.

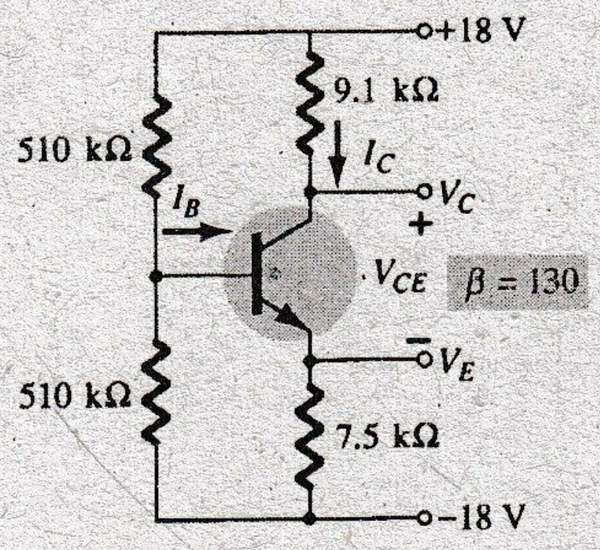


FIG. 4.139
Problem 39.

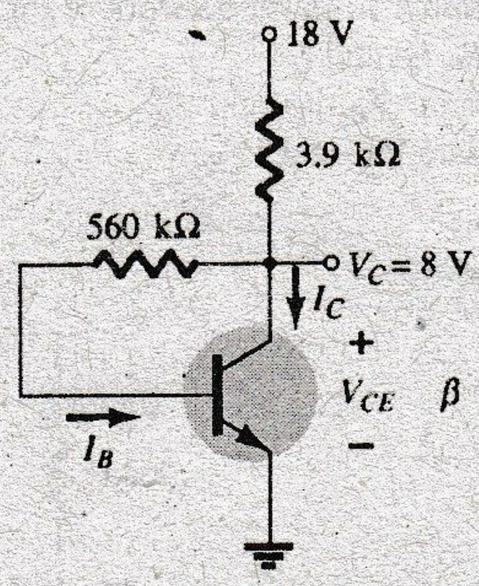


FIG. 4.140
Problems 40 and 68.

40. Given $V_C = 8$ V for the network of Fig. 4.140, determine:
- **a.** I_B.
- **b.** I_C.
- **c.** β.
- **d.** V_{CE}.

4.11 Design Operations

41. Determine R_C and R_B for a fixed-bias configuration if $V_{CC} = 12$ V, $\beta = 80$, and $I_{C_Q} = 2.5$ mA with $V_{CE_Q} = 6$ V. Use standard values.

42. Design an emitter-stabilized network at $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$ and $V_{CE_Q} = \frac{1}{2}V_{CC}$. Use $V_{CC} = 20$ V, $I_{C_{sat}} = 10$ mA, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

43. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of $I_{C_Q} = 4$ mA and $V_{CE_Q} = 8$ V. Choose $V_E = \frac{1}{8}V_{CC}$. Use standard values.

***44.** Using the characteristics of Fig. 4.121, design a voltage-divider configuration to have a saturation level of 10 mA and a Q-point one-half the distance between cutoff and saturation. The available supply is 28 V, and V_E is to be one-fifth of V_{CC}. The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

4.12 Multiple BJT Networks

45. For the R–C-coupled amplifier of Fig. 4.141 determine
- **a.** the voltages V_B, V_C, and V_E for each transistor.
- **b.** the currents I_B, I_C, and I_E for each transistor

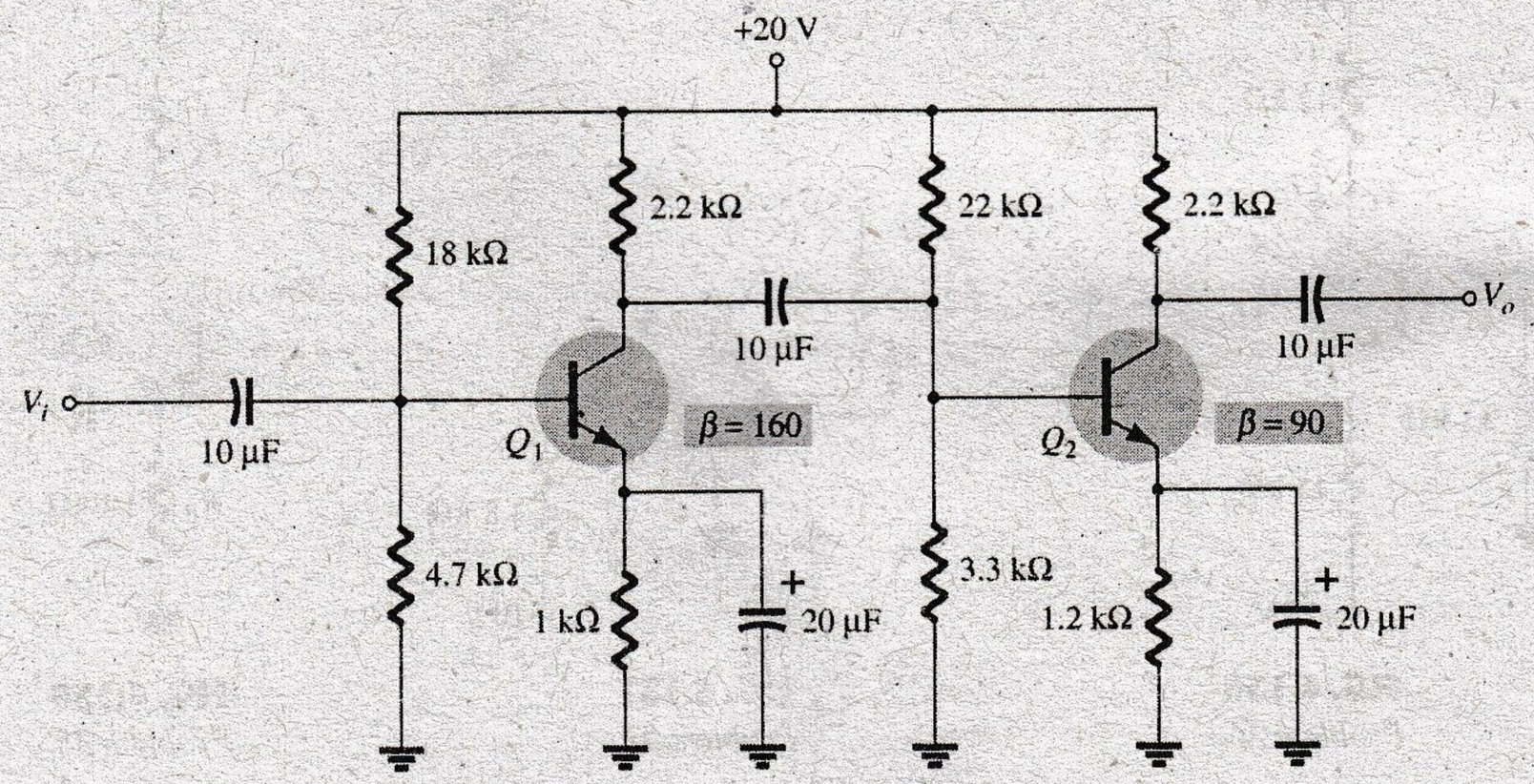


FIG. 4.141
Problem 45.

46. For the Darlington amplifier of Fig. 4.142 determine
- **a.** the level of β_D.
- **b.** the base current of each transistor.
- **c.** the collector current of each transistor.
- **d.** the voltages V_{C_1}, V_{C_2}, V_{E_1}, and V_{E_2}.

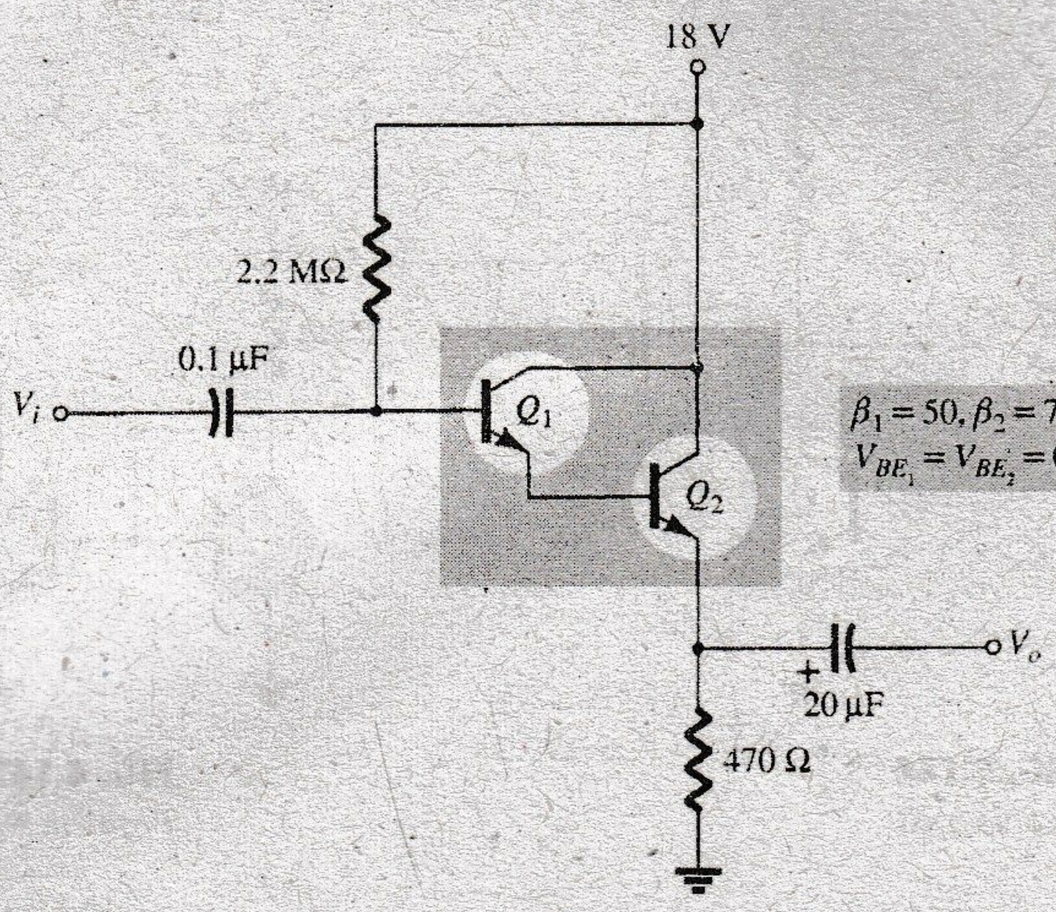


FIG. 4.142
Problem 46.

47. For the cascode amplifier of Fig. 4.143 determine
- **a.** the base and collector currents of each transistor.
- **b.** the voltages V_{B_1}, V_{B_2}, V_{E_1}, V_{C_1}, V_{E_2}, and V_{C_2}.

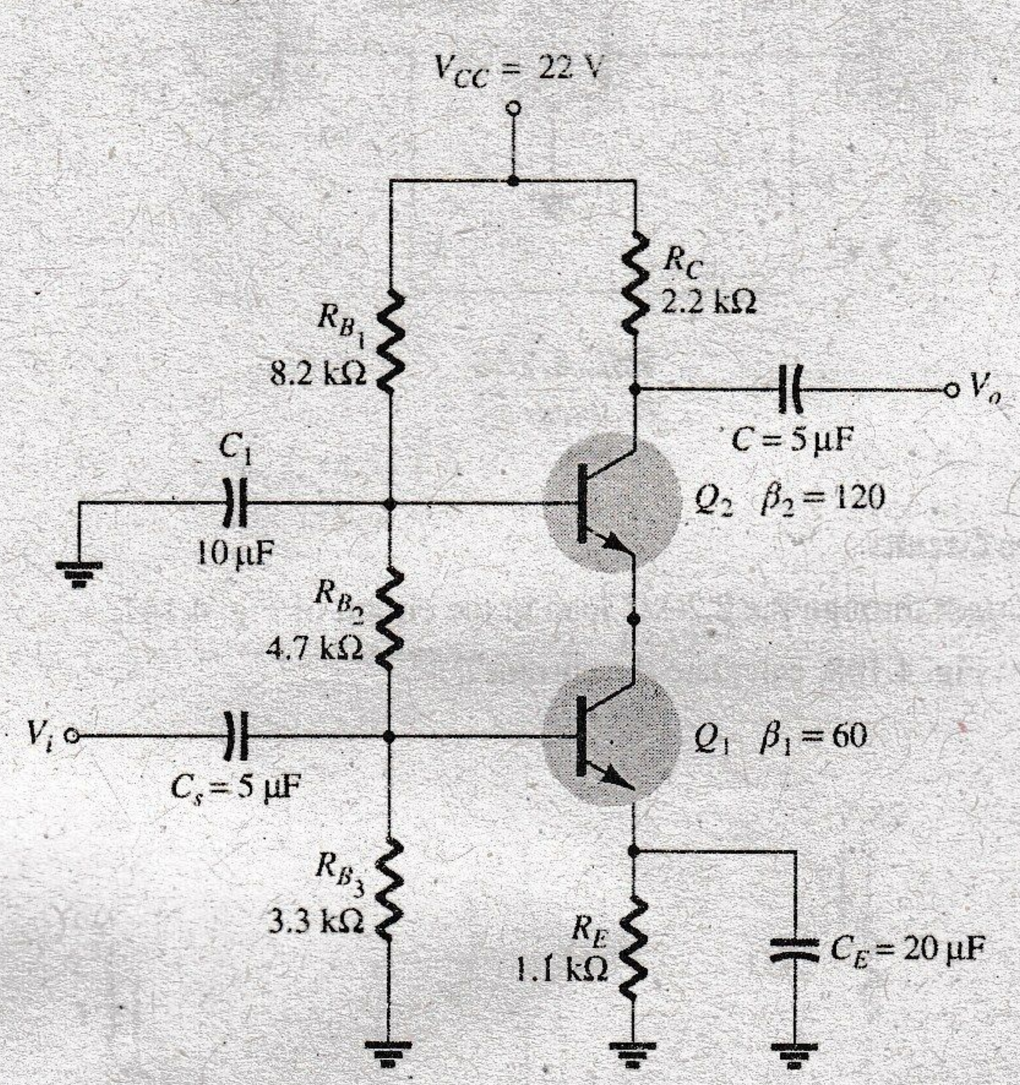


FIG. 4.143
Problem 47.

48. For the feedback amplifier of Fig. 4.144 determine
- **a.** the base and collector current of each transistor.
- **b.** the base, emitter, and collector voltages of each transistor.

4.13 Current Mirror Circuits

49. Calculate the mirrored current I in the circuit of Fig. 4.145.

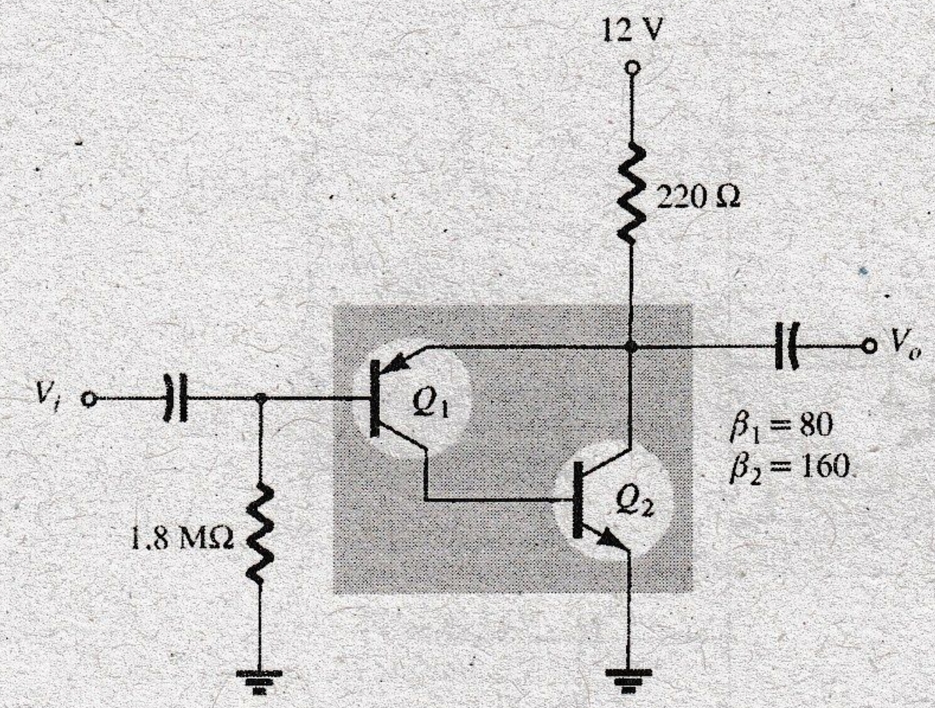


FIG. 4.144
Problem 48.

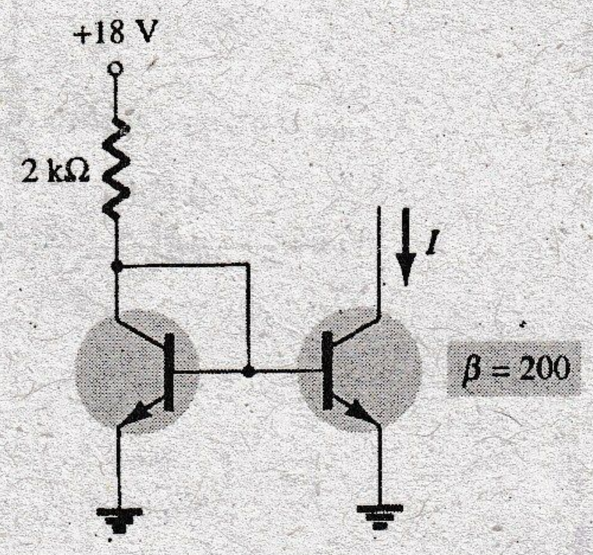


FIG. 4.145
Problem 49.

***50.** Calculate collector currents for Q_1 and Q_2 in Fig. 4.146.

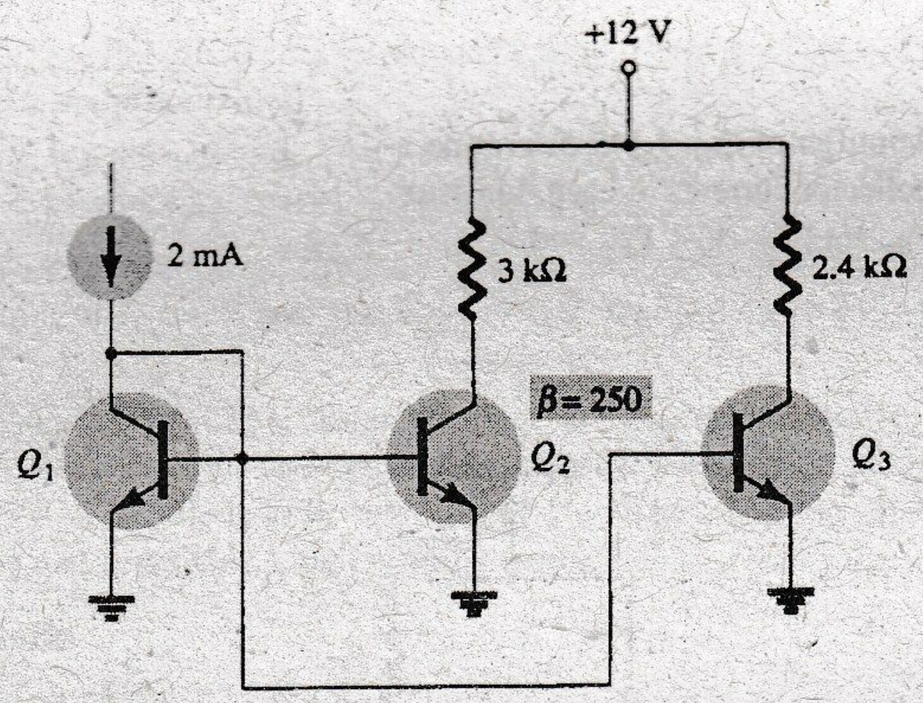


FIG. 4.146
Problem 50.

4.14 Current Source Circuits

51. Calculate the current through the 2.2-kΩ load in the circuit of Fig. 4.147.

52. For the circuit of Fig. 4.148, calculate the current I.

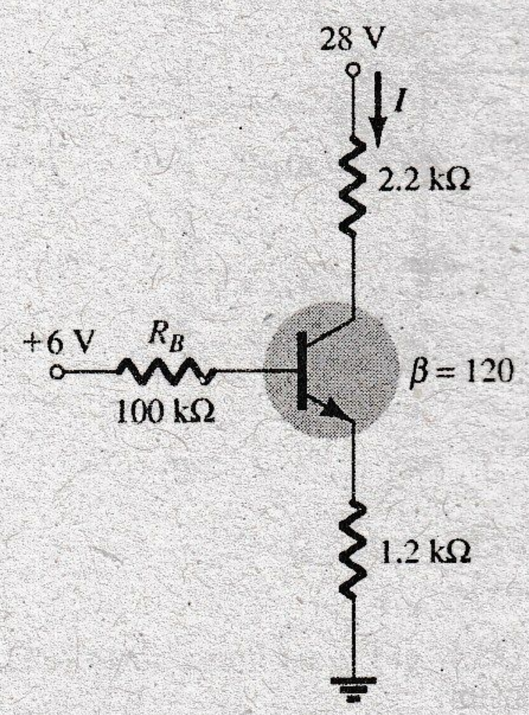


FIG. 4.147
Problem 51.

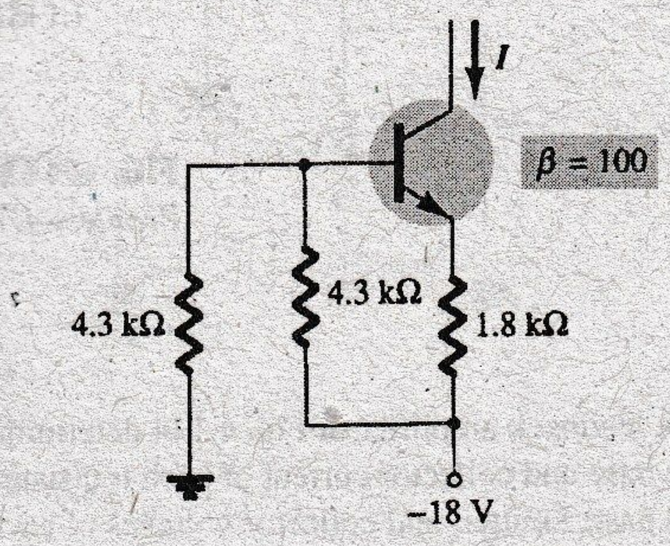


FIG. 4.148
Problem 52.

*53. Calculate the current I in the circuit of Fig. 4.149.

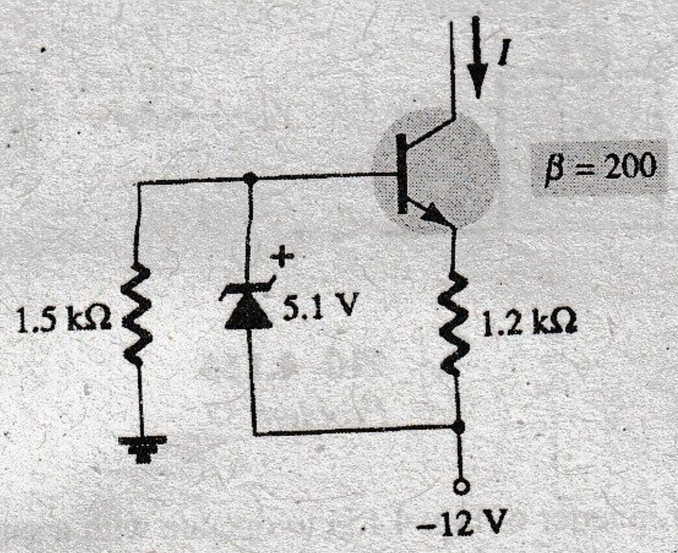


FIG. 4.149
Problem 53.

4.15 *pnp* Transistors

54. Determine V_C, V_{CE}, and I_C for the network of Fig. 4.150.

55. Determine V_C and I_B for the network of Fig. 4.151.

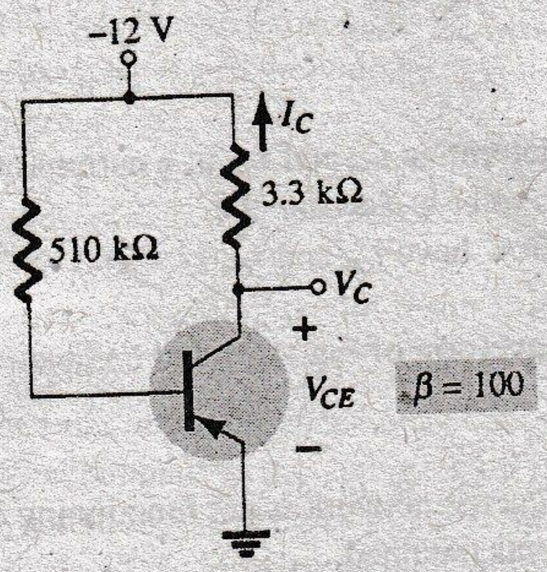


FIG. 4.150
Problem 54.

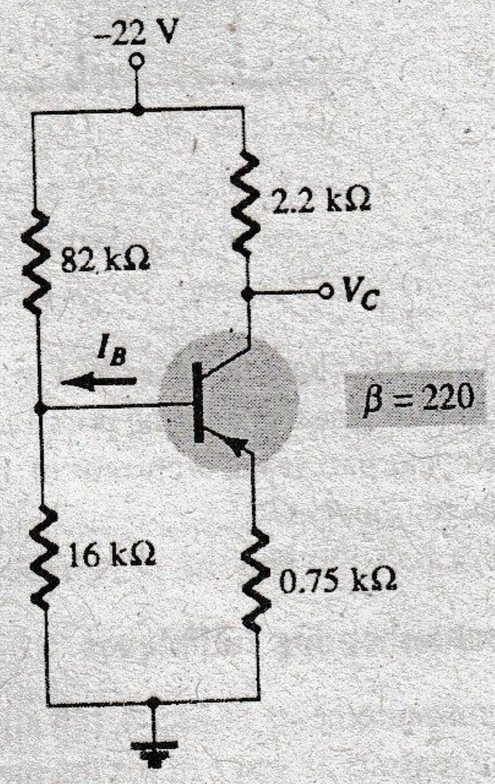


FIG. 4.151
Problem 55.

56. Determine I_E and V_C for the network of Fig. 4.152.

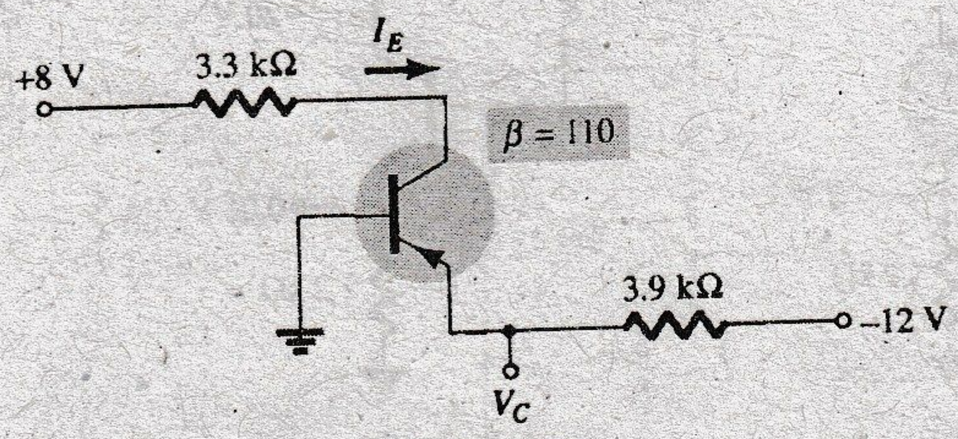


FIG. 4.152
Problem 56.

4.16 Transistor Switching Networks

*57. Using the characteristics of Fig. 4.121, determine the appearance of the output waveform for the network of Fig. 4.153. Include the effects of $V_{CE_{sat}}$, and determine I_B, $I_{B_{max}}$, and $I_{C_{sat}}$ when $V_i = 10$ V. Determine the collector-to-emitter resistance at saturation and cutoff.

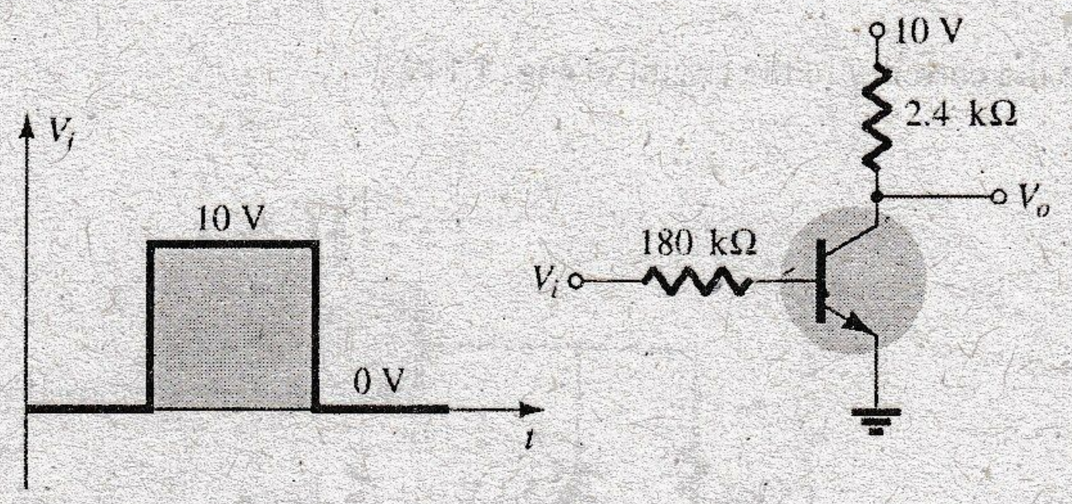


FIG. 4.153
Problem 57.

***58.** Design the transistor inverter of Fig. 4.154 to operate with a saturation current of 8 mA.using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B_{max}}$ and standard resistor values.

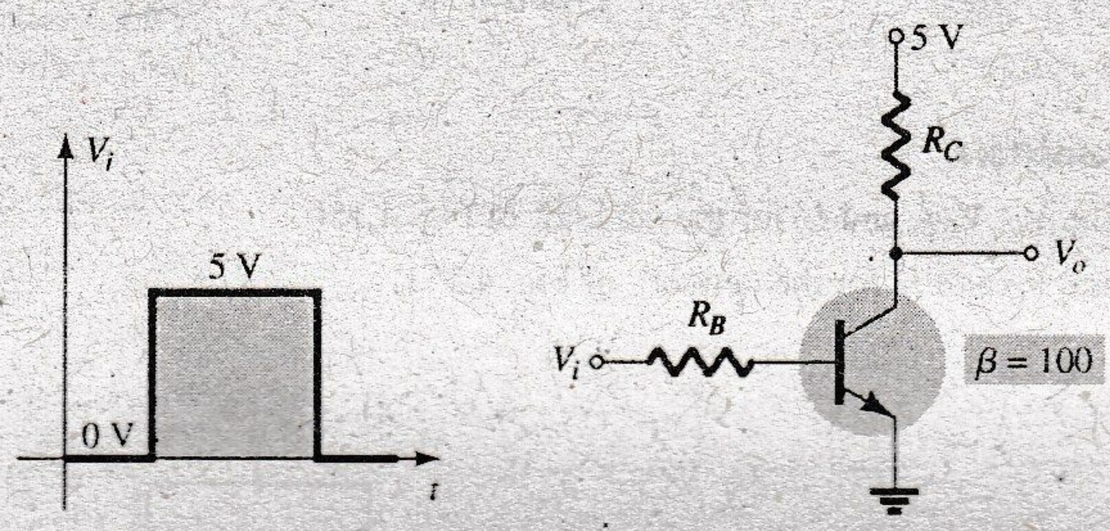


FIG. 4.154
Problem 58.

59. **a.** Using the characteristics of Fig. 3.23e, determine t_{on} and t_{off} at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 9.2.

b. Repeat part (a) at a current of 10 mA. How have t_{on} and t_{off} changed with increase in collector current?

c. For parts (a) and (b), sketch the pulse waveform of Fig. 4.91 and compare results.

4.17 Troubleshooting Techniques

***60.** The measurements of Fig. 4.155 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.

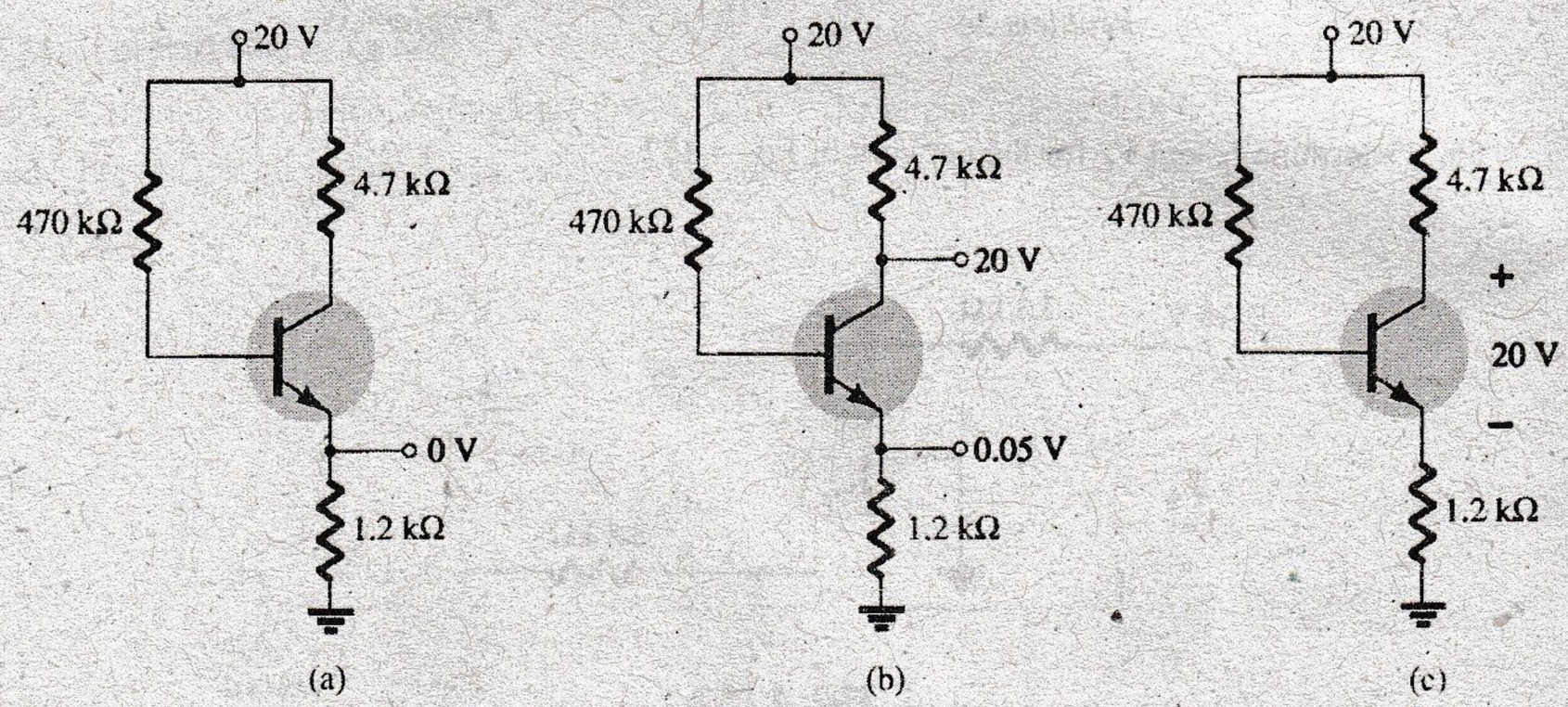


FIG. 4.155
Problem 60.

***61.** The measurements appearing in Fig. 4.156 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.

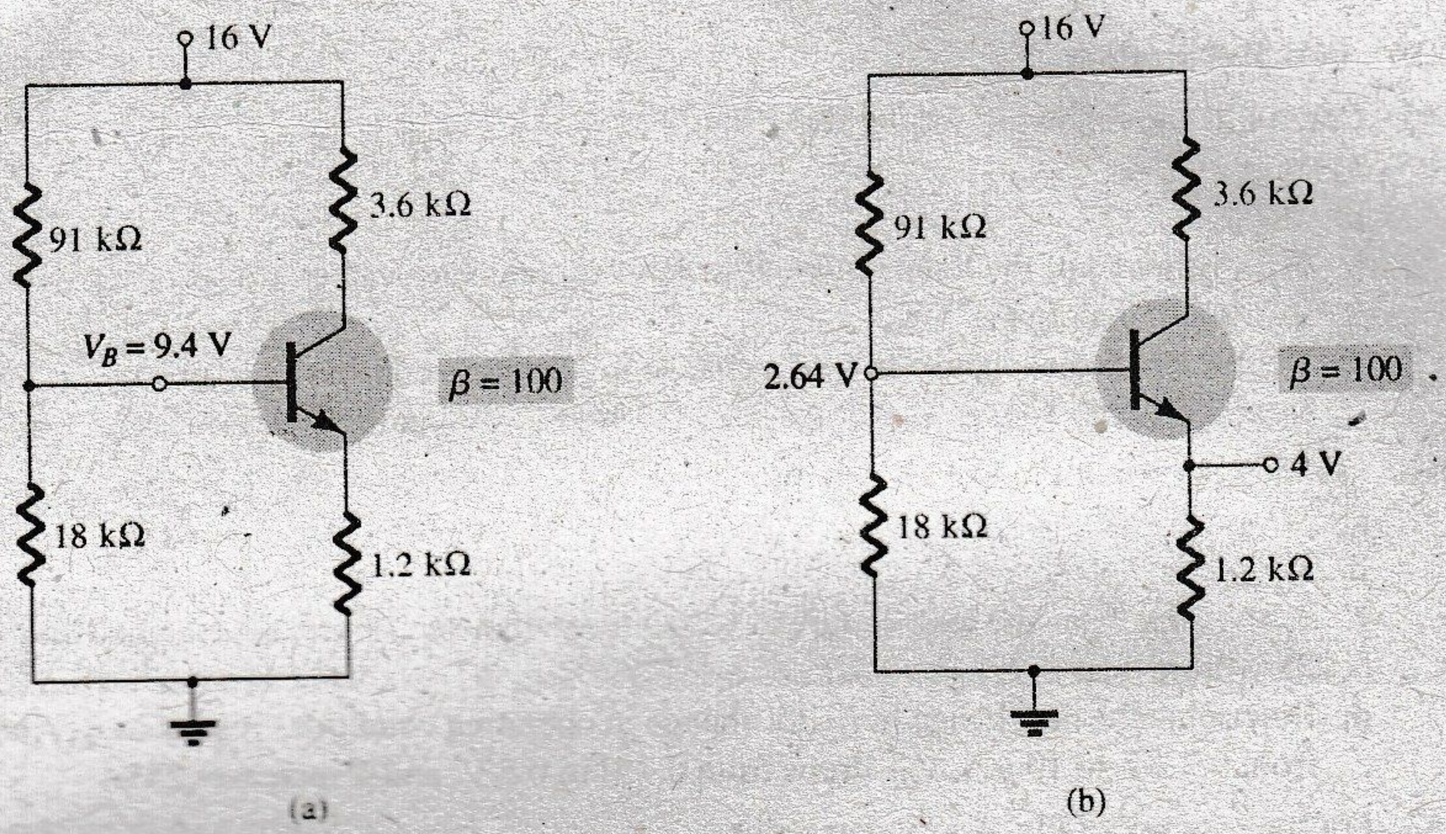


FIG. 4.156
Problem 61.

62. For the circuit of Fig. 4.157:

a. Does V_C increase or decrease if R_B is increased?

b. Does I_C increase or decrease if β is reduced?

c. What happens to the saturation current if β is increased?

d. Does the collector current increase or decrease if V_{CC} is reduced?

e. What happens to V_{CE} if the transistor is replaced by one with smaller β?

63 Answer the following questions about the circuit of Fig. 4.158:

a. What happens to the voltage V_C if the transistor is replaced by one having a larger value of β?

b. What happens to the voltage V_{CE} if the ground leg of resistor R_{B_2} opens (does not connect to ground)?

c. What happens to I_C if the supply voltage is low?

d. What voltage V_{CE} would occur if the transistor base–emitter junction fails by becoming open?

e. What voltage V_{CE} would result if the transistor base–emitter junction fails by becoming a short?

***64.** Answer the following questions about the circuit of Fig. 4.159:

a. What happens to the voltage V_C if the resistor R_B is open?

b. What should happen to V_{CE} if β increases due to temperature?

c. How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?

d. If the transistor collector connection becomes open, what will happen to V_E?

e. What might cause V_{CE} to become nearly 18 V?

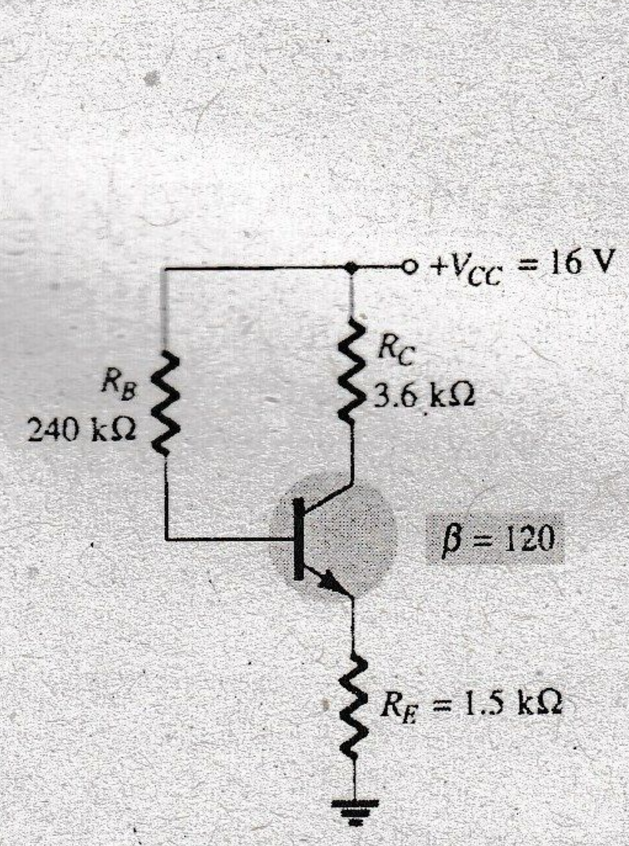


FIG. 4.157
Problem 62.

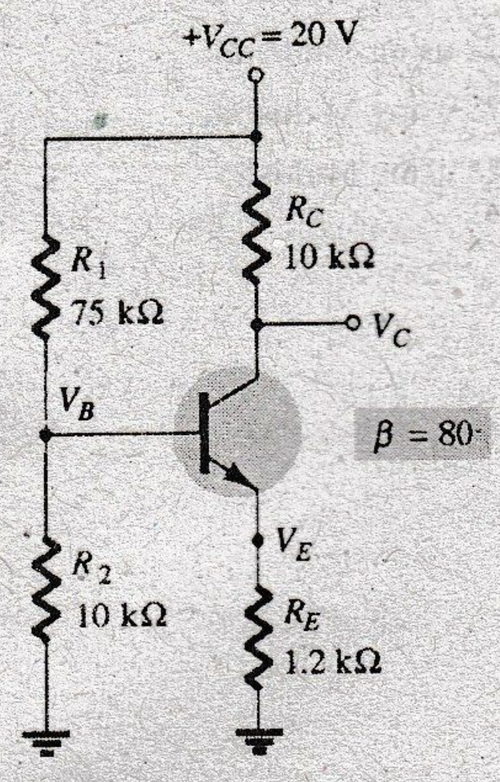


FIG. 4.158
Problem 63.

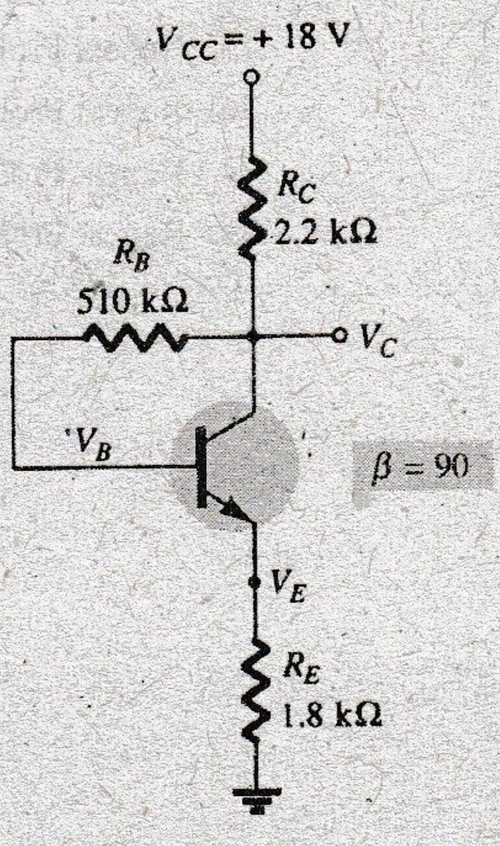


FIG. 4.159
Problem 64.

4.18 Bias Stabilization

65. Determine the following for the network of Fig. 4.118:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***66.** For the network of Fig. 4.122, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***67.** For the network of Fig. 4.125, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***68.** For the network of Fig. 4.140, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***69.** Compare the relative values of stability for Problems 65 through 68. The results for Exercises 65 and 67 can be found in Appendix E. Can any general conclusions be derived from the results?

***70.**
- **a.** Compare the levels of stability for the fixed-bias configuration of Problem 65.
- **b.** Compare the levels of stability for the voltage-divider configuration of Problem 67.
- **c.** Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

4.21 Computer Analysis

71. Perform a PSpice analysis of the network of Fig. 4.118. That is, determine I_C, V_{CE}, and I_B.

72. Repeat Problem 71 for the network of Fig. 4.122.

73. Repeat Problem 71 for the network of Fig. 4.125.

74. Repeat Problem 71 for the network of Fig. 4.129.

75. Repeat Problem 71 using Multisim.

76. Repeat Problem 72 using Multisim.

77. Repeat Problem 73 using Multisim.

78. Repeat Problem 74 using Multisim.