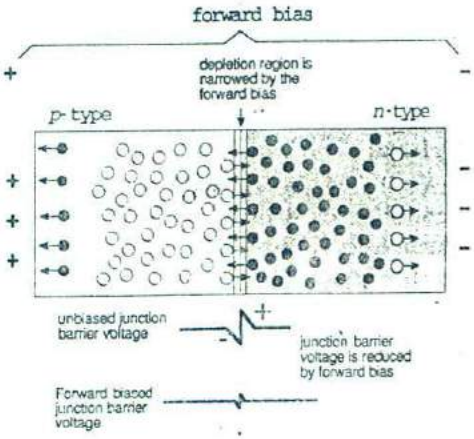
Chapter 1

Basic Semiconductor and pn-Junction Theory



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Objectives

You will be able to:

1. *Describe an atom, and sketch a diagram to show its components.*
2. *Explain energy levels and energy bands relating to electrons, and define valence band and conduction band.*
3. *Describe how electric current flow occurs by electron motion and by hole transfer.*
4. *Explain conventional current direction and direction of electron flow.*
5. *Sketch a diagram to show the relationship between covalently bonded atoms.*
6. *Discuss the differences between conductors, insulators, and semiconductors.*
7. *Explain how n-type and p-type semiconductor materials are created, and discuss the differences between the two types.*
8. *Sketch a pn-junction, and explain the origin of the junction depletion region.*
9. *Draw diagrams to show the effects of forward biasing and reverse biasing a pn-junction.*
10. *Sketch the current/voltage characteristics for forward biased and reverse biased pn-junctions.*
11. *Discuss temperature effects on conductors, insulators, semiconductors, and pn-junctions.*

Introduction

An electronic device controls the movement of electrons. The study of electronic devices requires a basic understanding of the relationship between electrons and the other components of an atom. The movement of electrons within a solid, and the bonding forces between atoms can then be investigated. This leads to a knowledge of the differences between conductors, insulators, and semiconductors, and to an understanding of *p*-type and *n*-type semiconductor material.

Junctions of *p*-type and *n*-type material (*pn*-junctions) are basic to all but a very few semiconductor devices. Forces act upon electrons that are adjacent to a *pn*-junction, and these forces are altered by the presence of an external bias voltage.

1-1 Atomic Theory

The Atom

The atom can be thought of as consisting of a central *nucleus* surrounded by orbiting *electrons* (see Fig. 1-1). Thus, it may be compared to a planet with orbiting satellites. Just as satellites are held in orbit by the attractive force of gravity due to the mass of the planet, so each electron is held in orbit by an *electrostatic force of attraction* between it and the nucleus.

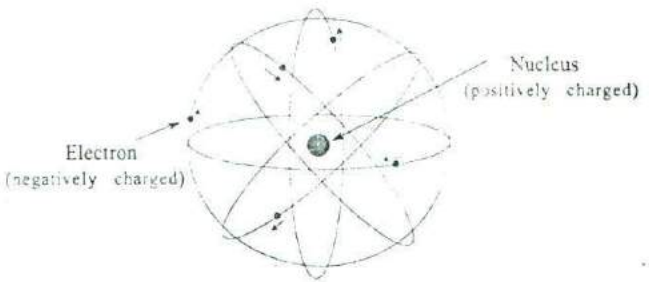


Figure 1-1
The atom consists of a central nucleus surrounded by orbiting electrons. The electrons have a negative charge, and the nucleus contains protons that are positively charged.

Each electron has a negative electrical charge of 1.602×10^{-19} coulombs (*C*), and some particles within the nucleus (*protons*) have a positive charge of the same magnitude. Since opposite charges attract, a force of attraction exists between the oppositely charged electron and nucleus. Compared to the mass of the nucleus, electrons are relatively tiny particles of almost negligible mass. In fact, they can be considered to be little particles of negative electricity having no mass at all.

The nucleus of an atom (Fig. 1-2) is largely a cluster of two types of particles, protons and *neutrons*. Protons have a positive electrical charge, equal in magnitude (but opposite in polarity) to the negative charge on an electron. A neutron has no charge at all. Protons and neutrons each have masses about 1800 times the mass of an electron. For a given atom, the number of protons in



Figure 1-2
The nucleus of an atom is largely a cluster of protons and neutrons.

the nucleus normally equals the number of orbiting electrons.

Since the protons and orbital electrons are equal in number and equal and opposite in charge, they neutralise each other electrically. For this reason, all atoms are normally electrically neutral. If an atom loses an electron, it has lost some negative charge. Thus, it becomes positively charged and is referred to as a *positive ion*. [see Fig 1-3(a)]. Similarly, if an atom gains an additional electron, it becomes negatively charged and is termed a *negative ion*. [Fig. 1-3(b)].

The differences among atoms consist largely of dissimilar numbers and arrangements of the three basic types of particles. However, all electrons are identical, as are all protons and all neutrons. An electron from one atom could replace an electron in any other atom. Different materials are made up of different types of atoms, or differing combinations of several types of atoms.

The number of protons in an atom is referred to as the *atomic number* of the atom. The *atomic weight* is approximately equal to the total number of protons and neutrons in the nucleus of the atom. The atom of the semiconductor material *silicon* has 14 protons and 14 neutrons in its nucleus, as well as 14 orbital electrons. Therefore, the atomic number for silicon is 14, and its atomic weight is approximately 28.

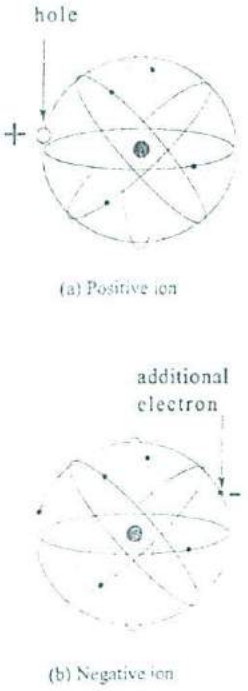


Figure 1-3
Positive and negative ions are created when an atom looses or gains an electron.

Electron Orbits and Energy Levels

Atoms may be conveniently represented by the two-dimensional diagrams shown in Figs. 1-4. It has been found that electrons can occupy only certain orbital rings or *shells* at fixed distances from the nucleus, and that each shell can contain only a particular number of electrons. The electrons in the outer shell determine the electrical (and chemical) characteristics of each particular type of atom. These electrons are usually referred to as *valence electrons*. An atom may have its outer shell, or *valence shell*, completely filled or only partially filled.

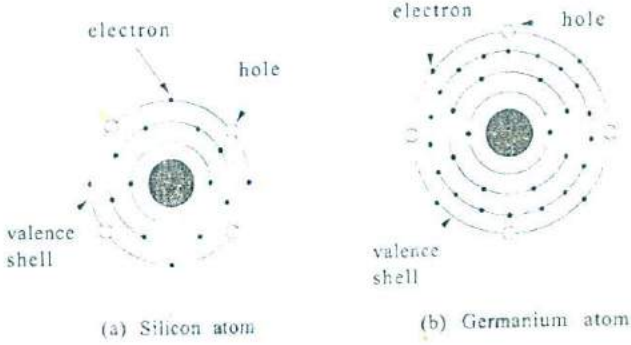


Figure 1-4
Two-dimensional representations of silicon and germanium atoms. The outer shells have four electrons and four holes.

The atoms represented in Fig. 1-4 are those of two important semiconductor materials, *silicon (Si)* and *germanium (Ge)*. It is seen that each of these atoms has four electrons in a valence shell that

can contain a maximum of eight. Thus, the valence shells have four electrons and four *holes*. A *hole* is defined as an absence of an electron in a shell where one could exist. Even though the valence shells of silicon and germanium have four holes, both types of atoms are electrically neutral because the total number of orbiting (negatively charged) electrons equals the total number of (positively charged) protons in the nucleus.

The closer an electron is to the nucleus, the stronger are the forces that bind it. Each shell has an *energy level* associated with it that represents the amount of energy required to extract an electron from the atom. Since the electrons in the valence shell are farthest from the nucleus, they require the least amount of energy to extract them. [see Fig 1-5(a)]. Conversely, those electrons closest to the nucleus require the greatest energy application to extract them from the atom.

The energy levels of the orbiting electrons are measured in *electron volts* (eV). An electron volt is defined as the amount of energy required to move one electron through a voltage difference of one volt.

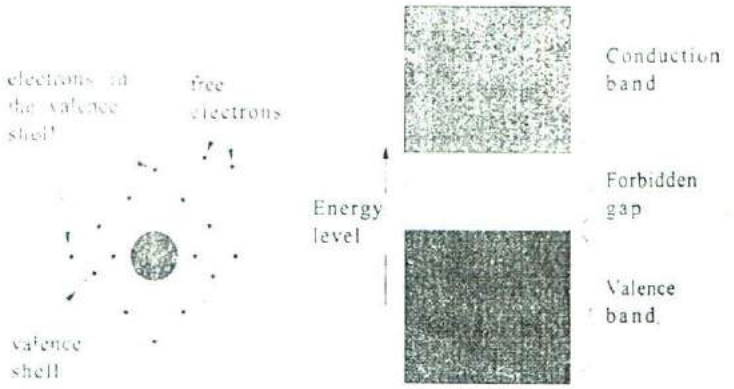


Figure 1-5
The energy level of electrons within a solid is shown by the energy band diagram. Electrons in orbit around a nucleus are in the valence band. Electrons which have broken away from an atom are in the conduction band.

Energy Bands

So far, the discussion has concerned a system of electrons in one isolated atom. The electrons of an isolated atom are acted upon only by the forces within that atom. However, when atoms are brought closer together, as in a solid, the electrons come under the influence of forces from other atoms. Under these circumstances, the energy levels that may be occupied by electrons merge into bands of energy levels. Within any given material there are two distinct energy bands in which electrons may exist: the *valence band* and the *conduction band*. Separating these two bands is an *energy gap*, termed the *forbidden gap*, in which no electrons can normally exist. The valence band, conduction band, and forbidden gap are shown diagrammatically in Fig. 1-5(b).

Electrons within the conduction band have become disconnected from atoms and are drifting around within the material. Conduction band electrons may be easily moved by the application of relatively small amounts of energy. Much larger amounts of energy must be applied to move an electron in the valence band. Electrons in the valence band are usually in orbit around a nucleus. For any given type of material, the forbidden gap may be large, small, or nonexistent. The distinction between conductors, insulators, and semiconductors is largely concerned with the relative widths of the forbidden gap.

It is important to note that *the energy band diagram is simply a graphic representation of the energy levels associated with electrons.* To repeat: those electrons in the valence band are actually in orbit around the nucleus of an atom; those in the conduction band are drifting in the spaces between atoms.

Section 1-1 Review

1-1.1 Define: nucleus, electron, electronic charge, proton, neutron, shell, positive ion, negative ion.

1-1.2 What is meant by atomic number and atomic weight? State the atomic number and atomic weight for silicon.

1-1.3 Define conduction band, valence band, and forbidden gap.

1-2 Conduction in Solids

Electron Motion and Hole Transfer

Conduction occurs in any given material when an applied voltage causes electrons within the material to move in a desired direction. This may be due to one or both of two processes: *electron motion* and *hole transfer.* In *electron motion,* free electrons in the conduction band are moved under the influence of the applied electric field, thus creating an electric current. (see Fig 1-6). Since electrons have a negative charge, they are repelled from the negative terminal of the applied voltage and attracted toward the positive terminal. Hole transfer involves electrons which are still attached to atoms, (those in the valence band).

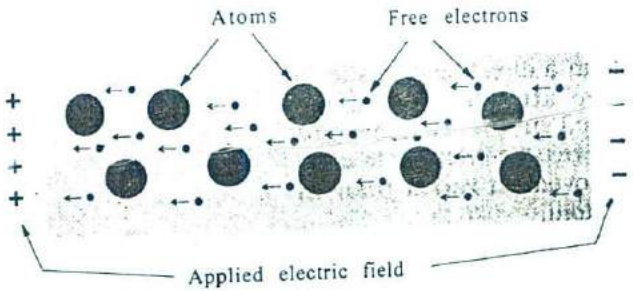


Figure 1-6
Free electrons are easily moved by an applied voltage to create an electric current.

If some of the electron positions in the valence shell of an atom are not occupied by electrons, there are holes where electrons could exist. When sufficient energy is applied, an electron may be made to jump from one atom to a hole in another atom. When it jumps, the electron leaves a hole behind it, and thus the hole has moved in a direction opposite to that of the electron.

Figure 1-7 illustrates a situation where there are no free electrons. However, those electrons in orbit around atoms experience a force of attraction to the positive terminal of the applied voltage, and repulsion from the negative terminal. This force can cause an electron to jump from one atom to another, moving toward the positive terminal.

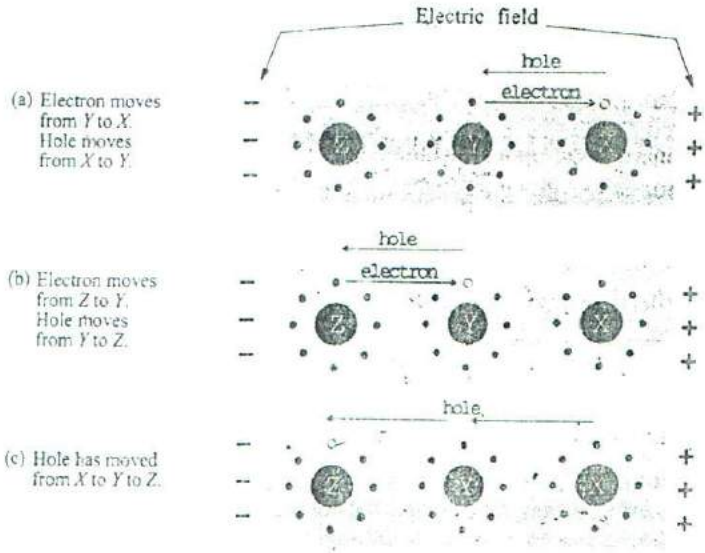


Figure 1-7
Conduction by hole transfer. An electron can be made to jump from one atom to another under the influence of an applied voltage, causing the hole to move in the opposite direction.

Figure 1-7(a) shows an electron jumping from atom *Y* to atom *X* (toward the positive terminal of the applied voltage). When this occurs, the hole in the valence shell of atom *X* is filled, and a hole is left in the valence shell of atom *Y*, [Fig. 1-7(b)]. If an electron now jumps from atom *Z* to fill the hole in *Y*, a hole is left in the valence shell of *Z*, [Fig. 1-7(c)]. Thus, the hole has moved from atom *X* to atom *Y* to atom *Z*. So, a flow of current (electron motion) has occurred, and this may be said to be due to *hole movement*, or *hole transfer*.

Holes may be thought of as *positively charged particles*, and as such, they move through an electric field in a direction opposite to that of electrons. (Positive particles are attracted toward the negative terminal of an applied voltage.) In the circumstance illustrated in Fig. 1-7 where there are few free electrons, it is more convenient to think in terms of hole movement rather than in terms of electrons jumping from atom to atom.

Since the flow of electric current is constituted by the movement of electrons and holes, electrons and holes are referred to as

charge carriers. Each time a hole moves, an electron must be supplied with sufficient energy, to enable it to escape from its atom. Free electrons require less application of energy than holes to move them, because they are already disconnected from their atoms. For this reason, electrons have *greater mobility* than holes.

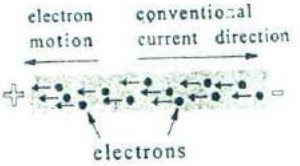


Figure 1-8
Conventional current direction is from positive to negative. Electron flow is from negative to positive.

Conventional Current and Electron Flow

In the early days of electrical experimentation it was believed that a positive charge represented an increased amount of electricity, and that a negative charge was a reduced quantity. Thus, it was assumed that current flowed from positive to negative. This is a convention that remains in use today even though current is now known to be a movement of electrons from negative to positive. (see Fig. 1-8).

Current flow from positive to negative is referred to as the ***conventional current direction.***

Electron flow from negative to positive is known as the ***direction of electron flow.***

It is important to understand both electron flow and conventional current direction. The operation of electronic devices is explained in terms of electron movement. However, *every graphic symbol used to represent an electronic device has an arrowhead which indicates conventional current direction.* (see the *diode* symbol in Fig. 1-9). Consequently, electronic circuits are most easily explained by using current flow from positive to negative.

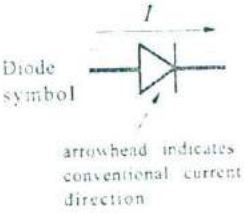


Figure 1-9
All electronic device graphic symbols have arrowheads that indicate conventional current direction.

Section 1-2 Review

1-2.1 Draw sketches to show the process of current flow by electron motion and by hole transfer.

1-2.2 Explain the difference between *conventional current direction* and *direction of electron flow*.

1-3 Conductors, Semiconductors, and Insulators

Bonding Forces Between Atoms

Whether a material is a conductor, semiconductor, or an insulator depends largely upon what happens to the outer-shell electrons when the atoms bond themselves together to form a solid. In the case of copper, the easily detached valence electrons are given up by the atoms. As illustrated in Fig. 1-10, this creates a great mass of free electrons (or electron gas) drifting about in the space between the copper atoms. The electrons are easily moved under the influence of an applied voltage to create a current flow. The bonding force that holds atoms together in a conductor is known as *metallic bonding*.

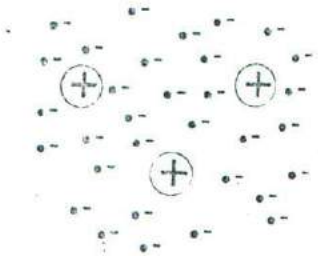


Figure 1-10
In metallic bonding there is a mass of free electrons drifting around in the spaces between atoms.

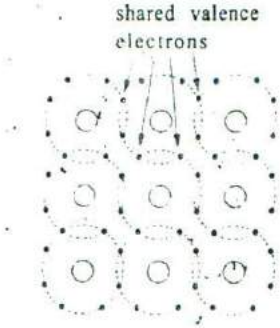


Figure 1-11
Covalent bonding in semiconductors produces very few free electrons and holes for current flow.

Semiconductor atoms normally have four outer-shell electrons and four holes, and are so close together that the outer-shell electrons behave as if they were orbiting in the valence shells of two atoms. In this way each valence-shell electron fills one of the holes in the valence shell of a neighbouring atom. This produces an atomic bonding force known as *covalent bonding*. As shown in Fig. 1-11, it would appear that there are no holes and no free electrons drifting about within the semiconductor material. In fact, some of the electrons are so weakly attached to their atoms that they can be made to break away to create a current flow when a voltage is applied.

In some insulating materials the atoms bond together in a similar way to semiconductor atoms *(covalent bonding)*. But the valence shell electrons are so strongly attached to their atoms in an insulator that no charge carriers are available for current flow. In other types of insulating materials, some atoms give up outer-shell electrons which are accepted into the orbit of neighbouring atoms. Because the atoms are *ionized*, this is termed *ionic bonding*, [Fig. 1-12]. Here again, all of the electrons are very strongly attached to the atoms, and the possibility of current flow is virtually zero.

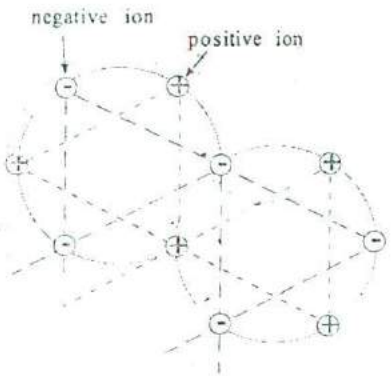


Figure 1-12
Ionic bonding occurs in some insulating materials. There are no holes or free electrons to facilitate current flow.

Energy Bands in Different Materials

The energy band diagrams in Fig. 1-13 show that insulators have a wide forbidden gap, semiconductors have a narrow forbidden gap, and conductors have no forbidden gap at all.

In the case of insulators, there are practically no electrons in the conduction band, and the valence band is filled. Also, the forbidden gap is so wide [Fig. 1-13(a)] that it would require the application of relatively large amounts of energy to cause an electron to cross from the valence band to the conduction band. Therefore, when a voltage is applied to an insulator, conduction cannot normally occur either by electron motion or hole transfer.

For semiconductors at absolute zero of temperature (-273°C) the valence band is usually full and there may be no electrons in the conduction band. As shown in Fig. 1-13(b), the forbidden gap in a semiconductor is very much narrower than that in an insulator, and the application of small amounts of energy can raise electrons from the valence band to the conduction band. Sufficient thermal energy for this purpose is available when the semiconductor is at normal room temperature. If a voltage is applied to the semiconductor, conduction can occur by both electron movement in the conduction band and by hole transfer in the valence band.

In the case of a conductor [Fig. 1-13(c)] there is no forbidden gap, and the valence and conduction energy bands overlap. For this reason, very large numbers of electrons are available for conduction, even at extremely low temperatures.

Typical resistance values for a 1-centimeter-cube sample are: Conductor $10^{-6}\ \Omega$, Semiconductor $10\ \Omega$, Insulator $10^{14}\ \Omega$.

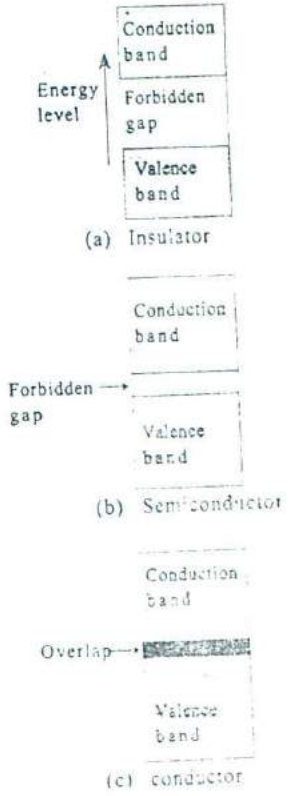


Figure 1-13
Energy band diagrams for insulators, semiconductors, and conductors.

Section 1-3 Review

1-3.1 Briefly describe the type of atomic bonding that occurs in (a) insulators, (b) conductors.

1-3.2 Draw a sketch to show the bonding of atoms in semiconductor material. Briefly explain.

1-3.3 Sketch and explain the energy band diagrams for conductors, insulators, and semiconductor.

1-4 n-Type and p-Type Semiconductor

Doping

Pure semiconductor material is known as *intrinsic* material. Before intrinsic material can be used for device manufacture, *impurity atoms* must be added to improve its conductivity. The process of adding the atoms is termed *doping*. Two different types of doping are possible; *donor doping*, and *acceptor doping*. Donor doping generates free electrons in the conduction band (i.e., electrons that are not tied to an atom). Acceptor doping produces valence band holes, or a shortage of valence electrons in the material. After doping, the semiconductor is known as *extrinsic* material.

n-Type Material

In donor doping, illustrated in Fig. 1-14, impurity atoms which have five electrons and three holes in their valence shells are added to the undoped material. The impurity atoms form covalent bonds with the silicon or germanium atoms. Because the semiconductor atoms have only four electrons and four holes in their valence shells, there is one extra valence-shell electron for each impurity atom added. Each additional electron produced in this way enters the conduction band as a free electron. As shown in Fig. 1-14, there is no hole for the fifth electron from the outer shell of the impurity atom; therefore, this electron becomes a free electron. Because the free electrons have *negative charges*, donor-doped semiconductor is known as *n-type material*.



Figure 1-14
In donor doping, impurity atoms with five valence shell electrons and three holes are added to the semiconductor material.

Free electrons in the conduction band are easily moved around under the influence of an electric field. Consequently, conduction occurs largely by electron motion in donor-doped semiconductor material. The doped material remains electrically neutral (it is neither positively charged nor negatively charged), because the total number of electrons (including the free electrons) is still equal to the total number of protons in the atomic nuclei.

The term *donor doping* comes from the fact that an electron is donated to the conduction band by each impurity atom. Typical donor materials are *antimony*, *phosphorus*, and *arsenic*. Since these atoms have five valence electrons, they are referred to as *pentavalent atoms*.

p-Type Material

The impurity atoms used for acceptor doping (Fig. 1-15) have outer shells containing three electrons and five holes. Suitable atoms with three valence electrons (*trivalent atoms*) are *boron*, *aluminum*, and *gallium*. These atoms form covalent bonds with the semiconductor atoms, but the bonds lack one electron for

complete outer shell of eight. In Fig. 1-15 the impurity atom illustrated has only three valence electrons; so, a hole exists in its bond with the surrounding atoms. Thus, in acceptor doping, holes are introduced into the valence band, so that conduction may occur by the process of hole transfer.

Since holes can be said to have a *positive charge*, acceptor-doped semi-conductor material is referred to as *p-type material*. As with *n*-type, the material remains electrically neutral, because the total number of orbital electrons in each impurity atom is equal to the total number of protons in its atomic nucleus. Holes can accept a free electron, hence the term *acceptor doping*.

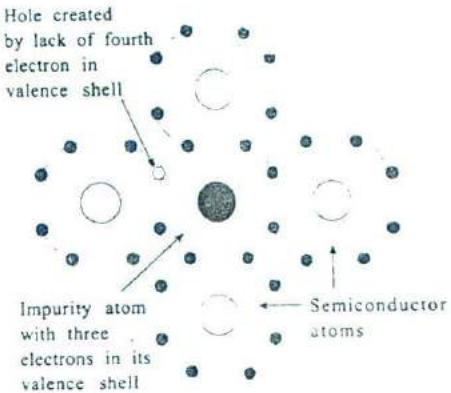


Figure 1-15
Acceptor doping requires the use of impurity atoms that have three electrons and five holes in the valence shells. This creates holes in the semiconductor material.

Majority and Minority Charge Carriers

In undoped semiconductor material at room temperature there are a number of free electrons and holes. These are due to thermal energy causing some electrons to break the bonds with their atoms and enter the conduction band. This process creates pairs of holes and electrons, and is appropriately termed *hole-electron pair generation*. The opposite effect, called *recombination*, occurs when an electron *falls into* a hole in the valence band. Because there are many more electrons than holes in *n*-type material, electrons are said to be the *majority charge carriers*, and holes are said to be *minority carriers* in *n*-type material. In *p*-type material, holes are the majority carriers and electrons are minority carriers.

Effects of Heat and Light

When a conductor is heated, the atoms (which are in fixed locations) tend to vibrate, and the vibration impedes the movement of the surrounding electron gas. This causes a reduction in the flow of the electrons that constitute the electric current. The reduced current flow means that the conductor resistance has increased. A conductor has a *positive temperature coefficient (PTC)* of resistance; a resistance which increases with

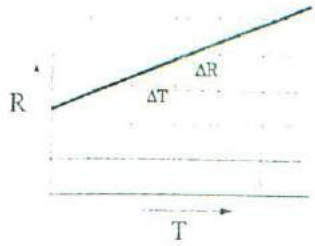
increasing temperature. This is illustrated in Fig. 1-16(a).

When undoped semiconductor material is at a temperature of absolute zero (-273°C), all electrons are in normal orbit around the atoms, and there are virtually no free electrons in the conduction band and no holes in the valence band. Consequently, at -273°C a semiconductor behaves as an insulator.

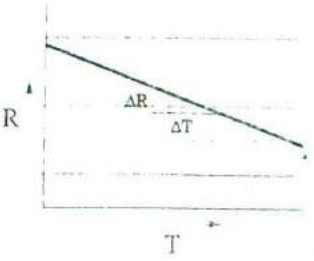
When the semiconductor temperature is raised, electrons break away from their atoms and move from the valence band to the conduction band. This produces holes in the valence band and free electrons in the conduction band, allowing conduction to occur by electron movement and by hole transfer. Increasing application of thermal energy generates an increasing number of hole-electron pairs.

As in the case of a conductor, thermal vibration of atoms occurs in a semiconductor. However, there are very few electrons to be impeded in a semiconductor compared to the large quantities in a conductor. The thermal generation of electrons is the dominating factor, and the semiconductor current increases with increasing temperature. This represents a decrease in resistance with increasing temperature; a *negative temperature coefficient (NTC)*, [Fig. 1-16(b)]. Heavily doped semiconductor material is an exception, behaving more like a conductor than a semiconductor.

Just as thermal energy can cause electrons to break their atomic bonds, so hole-electron-pairs can be generated by energy applied to a semiconductor in the form of light. A material which has few free electrons available for conduction when not illuminated is said to have a high *dark resistance*. When the semiconductor material is illuminated, its resistance decreases and may become comparable to that of a conductor.



(a) A conductor has a positive temperature coefficient



(b) A semiconductor has a negative temperature coefficient

Figure 1-16
The resistances of conductors and semiconductors are differently affected by temperature cha.

Section 1-4 Review

1-4.1 Draw a sketch to illustrate donor doping.

1-4.2 Draw a sketch to illustrate acceptor doping.

1-4.3 Define: *n-type material, p-type material, minority charge carriers, majority charge carriers, positive temperature coefficient, negative temperature coefficient, dark resistance.*

1-5 The pn-Junction

Junction of p-Type and n-Type

Two blocks of semiconductor material are represented in Fig. 1-17; one block is *p*-type material, and the other is *n*-type. The small circles in the *p*-type material represent holes, which are the majority charge carriers in *p*-type. The dots in the *n*-type material represent the majority charge carrier free electrons within that material. Normally, the holes are uniformly distributed throughout the volume of the *p*-type semiconductor, and the electrons are uniformly distributed in the *n*-type.

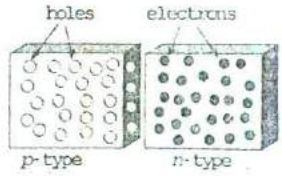


Figure 1-17.
P-type and n-type semiconductor materials.

In Figure 1-18, *p*-type and *n*-type semiconductor materials are shown side by side, representing a *pn-junction*. Holes and electrons are close together at the junction, so some free electrons from the *n*-side are attracted across the junction to fill adjacent holes on the *p*-side. They are said to *diffuse* across the junction from a region of high carrier concentration to one of low concentration. The free electrons crossing the junction create negative ions on the *p*-side by giving some atoms one more electron than their total number of protons. The electrons also leave positive ions (atoms with one fewer electron than the number of protons) behind them on the *n*-side.

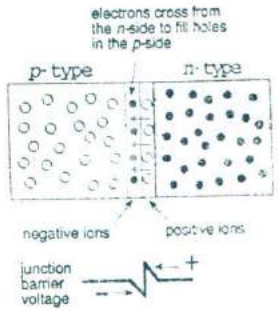


Figure 1-18
At a pn-junction, electrons cross from the n-side to fill holes in a layer of the p-side close to the junction.

Barrier Voltage

The *n*-type and *p*-type materials are both electrically neutral before the charge carriers diffuse across the junction. When negative ions are created on the *p*-side, the portion of the *p*-side close to the junction acquires a negative voltage, (see Fig. 1-18). Similarly, the positive ions created on the *n*-side gives the *n*-side a positive voltage close to the junction. The negative voltage on the *p*-side tends to repel additional electrons crossing from the *n*-side. Also, (thinking of the holes as positive particles) the positive voltage on the *n*-side tends to repel any hole movement from the *p*-side. Thus, the initial diffusion of charge carriers creates a *barrier voltage* at the junction, which is negative on the *p*-side and positive on the *n*-side. The transfer of charge carriers and the resultant creation of the barrier voltage occur when the *pn*-junctions are formed during the manufacturing process, (see Chapter 6).

The magnitude of the barrier voltage at a *pn*-junction can be calculated from a knowledge of the doping densities, electronic charge, and junction temperature. Typical barrier voltages at 25°C are 0.3 V for germanium junctions and 0.7 V for silicon.

It has been explained that the barrier voltage at the junction opposes both the flow of electrons from the *n*-side and the flow of holes from the *p*-side. Because electrons are the majority charge carriers in the *n*-type material, and holes are the majority charge carriers in the *p*-type, it is seen that *the barrier voltage opposes the flow of majority carriers* across the *pn*-junction, (see Fig. 1-19). Any free electrons generated by thermal energy on the *p*-side of the junction are attracted across the positive barrier to the *n*-side. Similarly, thermally generated holes on the *n*-side are attracted to the *p*-side through the negative barrier presented to them at the junction. Electrons on the *p*-side and holes on the *n*-side are minority charge carriers. Therefore, *the barrier voltage assists the flow of minority carriers* across the junction, (Fig. 1-19).

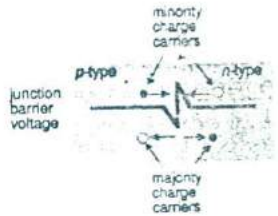


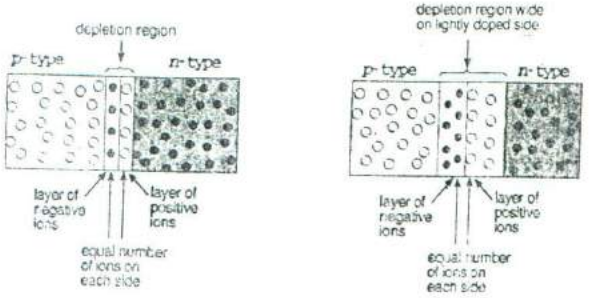
Figure 1-19
The barrier voltage at a pn-junction assists the flow of minority charge carriers and opposes the flow of majority carriers.

Depletion Region

The movement of charge carriers across the junction leaves a layer on each side which is depleted of charge carriers. This is the *depletion region* shown in Fig. 1-20(a). On the *n*-side, the depletion region consists of donor impurity atoms which, having lost the free electron associated with them, have become positively charged.

The depletion region on the *p*-side is made up of acceptor impurity atoms which have become negatively charged by losing the hole associated with them. (The hole has been filled by an electron.)

On each side of the junction, equal numbers of impurity atoms are involved in the depletion region. If the two blocks of semiconductor material have equal doping densities, the depletion layers on each side have equal widths, [Fig. 1-20(a)]. If the *p*-side is more heavily doped than the *n*-side, as illustrated in Fig. 1-20(b), the depletion region penetrates more deeply into the *n*-side in order to include an equal number of impurity atoms on each side of the junction. Conversely, when the *n*-side is most heavily doped, the depletion region penetrates deepest into the *p*-type material.



(a) Equal doping densities (b) Unequal doping densities

Figure 1-20
Charge carrier diffusion across a pn-junction creates a region depleted of charge carriers which penetrates deepest into the most lightly doped side.

Summarizing:

- A region depleted of charge carriers spreads across both sides of a *pn*-junction, penetrating furthest into the lowest doped side.
- The depletion region contains an equal number of ionized atoms on opposite sides of the junction.
- A barrier voltage is created by the charge carrier depletion effect, positive on the *n*-side and negative on the *p*-side.
- The barrier voltage opposes majority charge carrier flow and assists the flow of minority charge carriers across the junction.

Section 1-5 Review

1-5.1 Sketch a *pn*-junction showing the depletion region. Briefly explain how the depletion region is created.

1-5.2 Explain the origin of the barrier voltage at a *pn*-junction. Discuss the effect of the barrier voltage on minority and majority charge carriers.

1-6 Biased Junctions

Reverse Biased Junction

When an external bias voltage is applied to a *pn*-junction, positive to the *n*-side and negative to the *p*-side, electrons from the *n*-side are attracted to the positive terminal, and holes from the *p*-side are

attracted to the negative terminal. As shown in Fig. 1-21, holes on the *p*-side of the junction are attracted away from the junction, and electrons are attracted away from the junction on the *n*-side. This causes the depletion region to be widened and the barrier voltage to be increased, as illustrated. With the barrier voltage increase there is no possibility of majority charge carrier current flow across the junction, and the junction is said to be *reverse biased*. Because only a very small reverse current flows, a reverse-biased *pn*-junction can be said to have a high resistance.

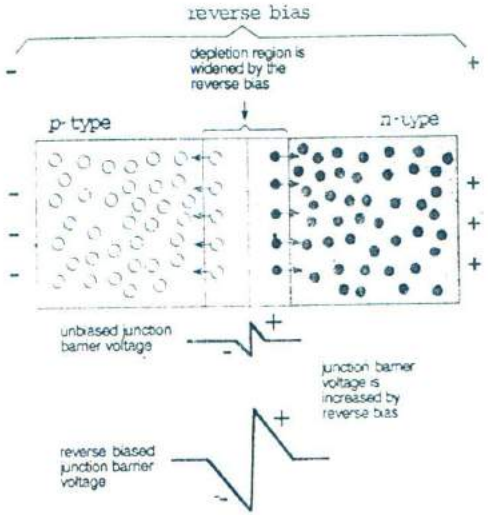


Figure 1-21
A reverse bias applied to a pn-junction (positive on the n-side, negative on the p-side) causes the depletion region to widen, and increases the barrier voltage. Only a very small reverse current flows across the junction.

Although there is no possibility of a majority charge carrier current flowing across a reverse-biased junction, minority carriers generated on each side can still cross the junction. Electrons in the *p*-side are attracted across the junction to the positive voltage on the *n*-side. Holes on the *n*-side may flow across to the negative voltage on the *p*-side. This is shown by the junction *reverse characteristic*, or the graph of reverse current (I_R) versus reverse voltage (V_R). (Fig. 1-22). Only a very small reverse bias voltage is necessary to direct all available minority carriers across the junction, and further increases in bias voltage do not increase the current. This current is referred to as a *reverse saturation current*.

The reverse saturation current is normally a very small quantity, ranging from nanoamps to microamps, depending on the junction area, temperature, and semiconductor material.

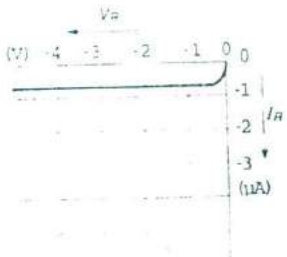


Figure 1-22
Current versus voltage characteristic for a reverse biased pn-junction.

Forward Biased Junction

Consider the effect of an external bias voltage applied with the polarity shown in Fig. 1-23; positive on the *p*-side, negative on the *n*-side. The holes on the *p*-side, being positively charged particles, are repelled from the positive terminal and driven toward the junction. Similarly, the electrons on the *n*-side are repelled from the negative terminal toward the junction. The result is that the

depletion region width and the barrier potential are both reduced.

When the applied bias voltage is progressively increased from zero, the barrier voltage gets smaller until it effectively disappears and charge carriers easily flow across the junction. Electrons from the *n*-side are now attracted across to the positive bias terminal on the *p*-side, and holes from the *p*-side flow across to the negative terminal on the n-side, (thinking of holes as positively-charged particles). Thus, a majority carrier current flows, and the junction is said to be *forward biased.*

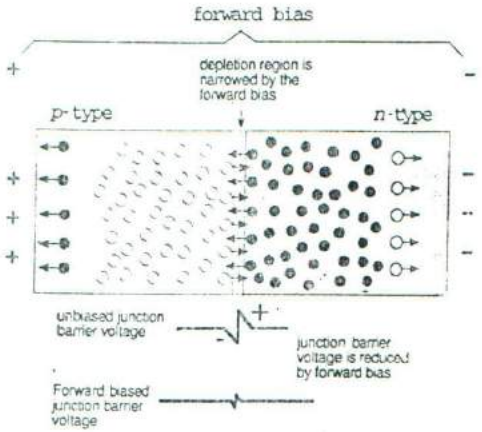


Figure 1-23
Forward biasing a pn-junction (positive on the p-side, negative on the n-side) narrows the depletion region, reduces the barrier voltage, and causes a relatively large current to flow across the junction.

The graph in Fig. 1-24 shows the forward current (I_F) plotted against forward voltage (V_F) for typical germanium and silicon *pn*-junctions. In each case, the graph is known as the *forward characteristic* of the junction. It is seen that very little forward current flows until V_F exceeds the junction barrier voltage (0.3 V for germanium, 0.7 V for silicon). When V_F is increased from zero toward the knee of the characteristic, the barrier voltage is progressively overcome, allowing more majority charge carriers to flow across the junction. Above the knee of the characteristic I_F increases almost linearly with increase in V_F. The level of current that can be made to flow across a forward-biased *pn*-junction largely depends on the junction area.

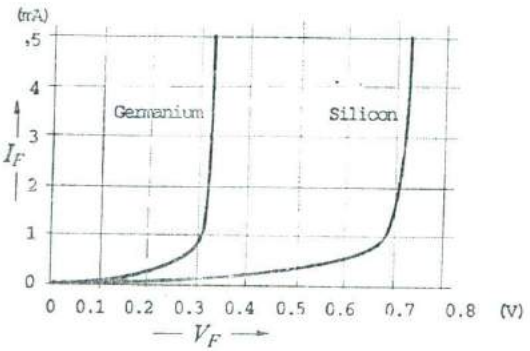
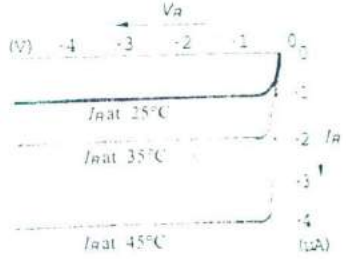


Figure 1-24
pn-junction forward characteristics. Germanium junctions are forward biased at approximately 0.3 V. A silicon junction requires approximately 0.7 V for forward bias.

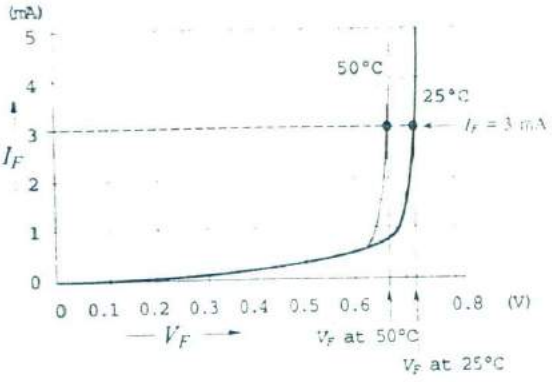
Junction Temperature Effects

As already discussed, the reverse saturation current (I_R) at a *pn*-junction consists of minority charge carriers. When the temperature of semiconductor material is increased, increasing numbers of electrons break away from their atoms. This generates additional minority charge carriers, causing I_R to increase as the junction temperature rises. It can be shown that the reverse current level approximately doubles with each 10°C increase in temperature, and that for a given junction, there is a definite I_R level for each temperature level, see Fig. 1-25(a).

The junction forward voltage drop (V_F) is also affected by temperature. The horizontal line (at 3 mA) on Fig. 1-25(b) shows that, if I_F is held constant while the junction temperature is changing, the forward voltage decreases with increasing junction temperature. This means that V_F has a negative temperature coefficient. It is found that the temperature coefficient for the forward voltage of a *pn*-junction is approximately -1.8 mV/°C for a silicon junction, and -2.02 mV/°C for germanium.



(a) Reverse current approximately doubles with each 10°C temperature increase



(b) Forward voltage drop changes by approximately -2 mV/°C

Figure 1-25
Junction reverse current and forward voltage drop are affected by temperature change.

Section 1-6 Review

1-6.1 Sketch typical voltage/current characteristics for a forward biased silicon *pn*-junction. Briefly explain.

1-6.2 Sketch typical voltage/current characteristics for a reverse biased *pn*-junction. Briefly explain.

1-6.3 Discuss the effects of temperature change on forward and reverse biased *pn*-junctions.

Chapter-1 Review Questions

Section 1-1

1-1 Describe the atom and draw a two-dimensional diagram to illustrate your description. Compare the atom to a planet with orbiting satellites.

1-2 Define: nucleus, electron, electronic charge, proton, neutron, shell, positive ion, negative ion.

1-3 Sketch two-dimensional diagrams of silicon and germanium atoms. Describe the valence shell of each atom.

1-4 Explain atomic number and atomic weight. State the atomic number and atomic weight for silicon.

1-5 Explain what is meant by energy levels and energy bands. Sketch an energy band diagram, and define conduction band, valence band, and forbidden gap.

Section 1-2

1-6 Draw a sketch to show the process of current flow by electron motion. Briefly explain.

1-7 Draw sketches to show the process of current flow by hole transfer. Which have greater mobility, electrons or holes? Explain why.

1-8 Define *conventional current direction* and *direction of electron flow*. State why each is important.

Section 1-3

1-9 Name the three kinds of bonds that hold atoms together in a solid. What kind of bonding might be found in: (a) conductors, (b) insulators, (c) semiconductors?

1-10 Draw sketches to illustrate *metallic bonding* and *ionic bonding*. Explain what occurs in each case.

1-11 Draw a sketch to illustrate *covalent bonding*. Explain the bonding process.

1-12 Draw energy band diagrams for conductors, insulators, and semiconductors. Explain the reasons for the differences between the diagrams.

Section 1-4

1-13 Define *acceptor doping*, and draw a sketch to illustrate the process. Explain.

1-14 Define *donor doping*, and draw a sketch to illustrate the process. Explain.

1-15 State the names given to acceptor-doped material and donor-doped material. Explain.

1-16 What is meant by *majority charge carriers* and *minority charge carriers*? Which are majority carriers and why in: (a)

donor-doped material, (b) acceptor-doped material?

1-17 Explain what happens to resistance with increasing temperature in the case of: (a) a conductor, (b) a semiconductor, (c) a heavily doped semiconductor. What do you think would happen to the resistance of an insulator with increasing temperature? Why?

1-18 Explain *hole-electron pair generation* and *recombination*.

1-19 Discuss the effects that illumination can produce on semiconductor materials.

1-20 Define: *n-type material, p-type material, majority charge carriers, minority charge carriers, positive temperature coefficient, negative temperature coefficient, dark resistance.*

Section 1-5

1-21 Using illustrations, explain how the *depletion region* and *barrier voltage* are produced at a *pn*-junction. List the characteristics of the depletion region.

1-22 Draw a sketch to show the depletion region and barrier voltage at a *pn*-junction, with unequal doping of each side. Briefly explain.

Section 1-6

1-23 A bias is applied to a *pn*-junction, positive to the *p*-side, negative to the *n*-side. Show, by a series of sketches, the effect of this bias on depletion region width, barrier voltage, minority carriers, and majority carriers. Briefly explain the effect in each case.

1-24 Repeat Question 1-23 for a bias applied negative to the *p*-side and positive to the *n*-side.

1-25 Sketch the voltage-current characteristics for a *pn*-junction: (a) with forward bias, and (b) with reverse bias. Show how temperature change affects the characteristics.

1-26 State typical values of barrier voltage for silicon and germanium junctions. Discuss the resistances of forward-biased and reverse-biased *pn*-junctions.

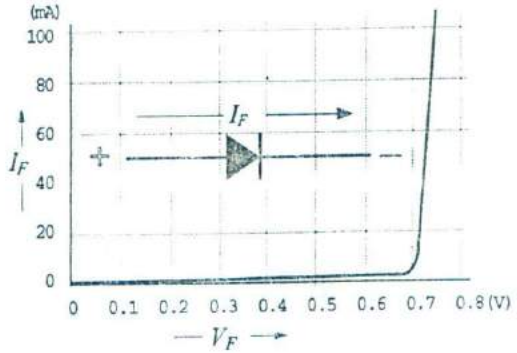
1-27 State typical *reverse saturation current* levels for *pn*-junctions. Explain the origin of reverse saturation current.

Chapter 2

Semiconductor Diodes

Chapter Contents

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2-1 pn-Junction Diode 22
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2-5 Temperature Effects 32
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Objectives

You will be able to:

1. Sketch a diode circuit symbol, identify the terminals, and discuss diode circuit behaviour.
2. Explain diode forward and reverse characteristics.
3. List important diode parameters, and determine parameter values from the characteristics.
4. Sketch approximate diode characteristics and dc equivalent circuits, and apply them to circuit analysis.
5. Draw dc load lines on diode characteristics to precisely analyse diode circuits.
6. Determine maximum diode power dissipations and forward voltages at various temperatures.
7. Sketch diode ac equivalent circuits and calculate switching times.
8. Determine diode parameter values from device data sheets.
9. Test diodes and plot the characteristics.
10. Sketch a Zener diode circuit symbol, identify the terminals, and explain the characteristics.
11. Determine Zener diode parameter values from device characteristics and from data sheets
12. Analyse basic Zener diode circuits.

Introduction

The term *diode* identifies a two-electrode, or two-terminal, device. A semiconductor diode is simply a *pn*-junction with a connecting lead on each side. A diode is a one-way device, offering a low resistance when forward biased, and behaving almost as an open switch when reverse biased. An approximately constant voltage drop across occurs across a forward-biased diode, and this simplifies diode circuit analysis. Diode (forward and reverse) characteristics are graphs of corresponding current and voltage levels. For precise circuit analysis, dc load lines are drawn on the diode forward characteristic.

Some diodes are low-current devices for use in switching circuits. High-current diodes are most often used as rectifiers for *ac* to *dc* conversion. Zener diodes are operated in reverse breakdown, because they have a very stable breakdown voltage. There are many other types of diodes designed for specialised applications.

2-1 pn-Junction Diode

As discussed in Sections 1-5 and 1-6, a *pn*-junction has the ability to permit substantial current flow when forward-biased, and to block current when reverse-biased. Thus, it can be used as a switch: *on* when forward-biased, and *off* when biased in reverse. A *pn*-junction provided with copper wire connecting leads becomes an electronic device known as a *diode*, (see Fig. 2-1).

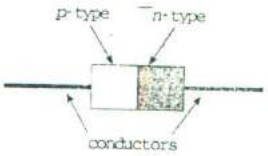


Figure 2-1
A semiconductor diode is a pn-junction with conductors for connecting the device to a circuit.

The circuit symbol (or *graphic symbol*) for a diode is an arrowhead and bar, (Fig. 2-2). The arrowhead indicates the conventional direction of current flow when the diode is forward biased, (from the positive terminal through the device to the negative terminal). The *p*-side of the diode is always the positive terminal for forward bias and is termed the *anode*. The *n*-side, called the *cathode*, is the negative terminal when the device is forward biased.

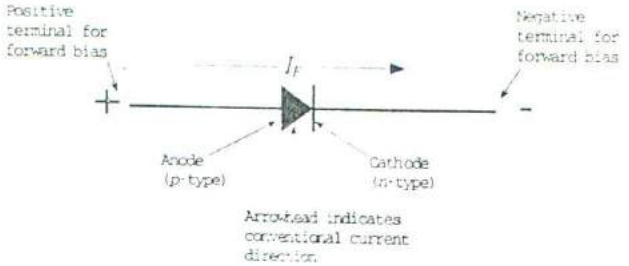


Figure 2-2
Diode circuit symbol. Current flows when the diode is forward biased: + on the anode, - on the cathode.

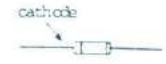
A *pn*-junction diode can be destroyed by a high level of forward current overheating the device. It can also be destroyed by a large reverse voltage causing the junction to breakdown. The maximum level of forward current and reverse voltage for diodes are specified

on the manufacturer's data sheets, (see Section 2-6). In general physically large diodes pass the largest currents and survive the largest reverse voltages. Small diodes are limited to low current levels and low reverse voltages.

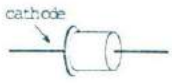
Figure 2-3 shows the appearance of low-, medium-, and high-current diodes. The body of the low-current device in Fig. 2-3(a) may be only 0.3 cm long, so the cathode is usually denoted by a coloured band. This type of diode is typically capable of passing a maximum forward current of approximately 100 mA. It can also survive about a 75 V reverse bias without breaking down, and its reverse current at 25°C is usually less than 1 μA.

The medium-current diode shown in Fig. 2-3(b) can typically pass a forward current of about 400 mA and survive over 200 V of reverse bias. The anode and cathode terminals may be indicated by a diode symbol on the side of the device.

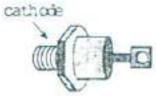
Low-current and medium-current diodes are usually mounted by soldering the connecting leads to terminals. Power dissipated in the device is then carried away by air convection and by heat conduction along the connecting leads. High-current diodes, or *power diodes* [Fig. 2-3(c)], generate a lot of heat. So, air convection would be completely inadequate. Such devices are designed for mechanically connecting to a metal heat sink. Power diodes can pass forward currents of many amperes and can survive several hundred volts of reverse bias.



(a) Low-current diode



(b) Medium-current diode



(c) High-current diode

Figure 2-3
The size and appearance of a diode depends upon the level of forward current that the device is required to pass.

2-2 *Characteristics and Parameters*

Forward and Reverse Characteristics

The semiconductor diode is essentially a *pn*-junction, and its characteristics are those discussed in Chapter 1. Figures 2-4 and 2-5 show typical forward and reverse characteristics for low-current silicon and germanium diodes. From the silicon diode characteristics in Fig. 2-4, it is seen that the forward current (I_F) remains very low (less than microamps) until the diode forward-bias voltage (V_F) exceeds approximately 0.7 V. Above 0.7 V, I_F increases almost linearly with increase in V_F.

Because the diode reverse current (I_R) is very much smaller than its forward current, the reverse characteristics are plotted with expanded current scales. For a silicon diode, I_R is normally less than 100 nA, and it is almost completely independent of the reverse-bias voltage. As already explained in Chapter 1, I_R is largely a minority charge carrier *reverse saturation current*. A small increase in I_R can occur with increasing reverse-bias voltage, due to some minority charge carriers leaking along the junction surface. For a diode with the characteristics in Fig. 2-4, the reverse current is typically less than 1/10,000 of the lowest normal forward current level. Therefore, I_R is quite negligible when compared to I_F, and a reverse-biased diode may be treated almost as an open switch. This is further investigated in Example 2-1

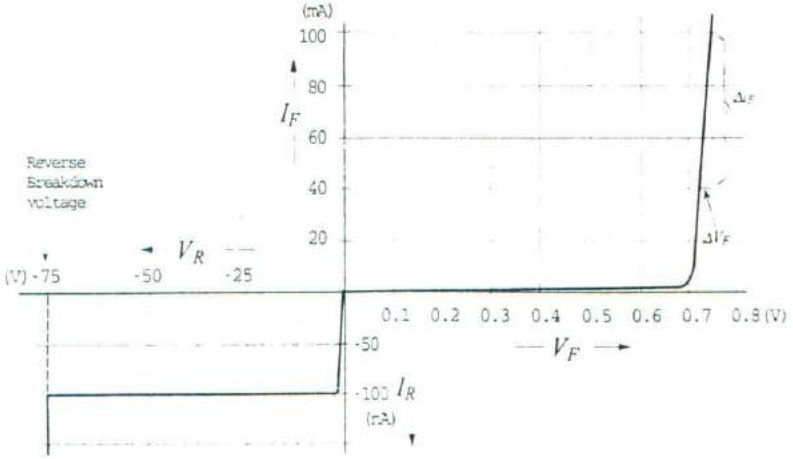


Figure 2-4
Typical forward and reverse characteristics for a silicon diode

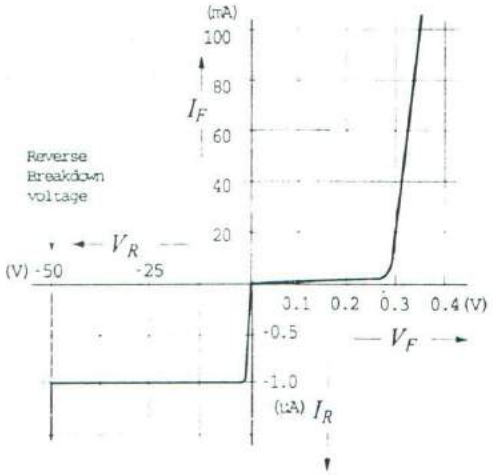


Figure 2-5
Typical forward and reverse characteristics for a germanium diode.

Example 2-1

Calculate the forward and reverse resistances offered by a silicon diode with the characteristics in Fig. 2.4, at I_F = 100 mA, and at V_R = 50 V.

Solution

at I_F = 100 mA, $V_F \approx 0.75$ V

$$R_F = \frac{V_F}{I_F} = \frac{0.75\text{ V}}{100\text{ mA}} \quad \text{[see Fig. 2-6(a)]}$$

$$= 7.5\ \Omega$$

at V_R = 50 V, I_R = 100 nA

$$R_R = \frac{V_R}{I_R} = \frac{50\text{ V}}{100\text{ nA}} \quad \text{[see Fig. 2-6(b)]}$$

$$= 500\ \text{M}\Omega$$



(a) Forward resistance



(b) Reverse resistance

Figure 2-6
Diode forward and reverse resistance determination.

When the diode reverse voltage (V_R) is sufficiently increased, the device goes into *reverse breakdown*. For the characteristics shown in Fig. 2-4, reverse breakdown occurs at 75 V. Reverse breakdown can destroy a diode unless the current is limited by a suitable series-connected resistor. Reverse breakdown is usefully applied in *Zener diodes* which are discussed in Section 2-9.

The characteristics of a germanium diode are similar to those of a silicon diode, with some important differences, (see Fig. 2-5). The forward voltage drop of a germanium diode is typically 0.3 V, compared to 0.7 V for silicon. For a germanium device, the reverse saturation current at 25°C may be around 1 μA, which is much larger than the reverse current for a silicon diode. Finally, the reverse breakdown voltage for germanium devices is likely to be substantially lower than that for silicon devices.

The lower forward voltage drop for germanium diodes can be a distinct advantage. However, the lower reverse current and higher reverse breakdown voltage of silicon diodes make them preferable to germanium devices for most applications.

Diode Parameters

The diode parameters of greatest interest are:

V_F	*forward voltage drop*
I_R	*reverse saturation current*
V_{BR}	*reverse breakdown voltage*
r_d	*dynamic resistance*
I_{Fmax}	*maximum forward current*

The values of these quantities are normally listed on the diode data sheet provided by device manufacturers (see Section 2-7). Some of the parameters can be determined directly from the diode characteristics. For the silicon diode characteristics in Fig. 2-4, V_F = 0.7 V, I_R = 100 nA, and V_{BR} = 75 V.

The forward resistance calculated in Example 2-1 is a *static quantity*; it is a constant resistance of the diode at a particular constant forward current. The *dynamic resistance* of the diode is the resistance offered to changing levels of forward voltage. The dynamic resistance, also known as the *incremental resistance* or *ac resistance*, is the reciprocal of the slope of the forward characteristics beyond the knee. Referring to Fig. 2-4, and Fig. 2-7,

$$r_d = \frac{\Delta V_F}{\Delta I_F} \qquad \textbf{(2-1)}$$

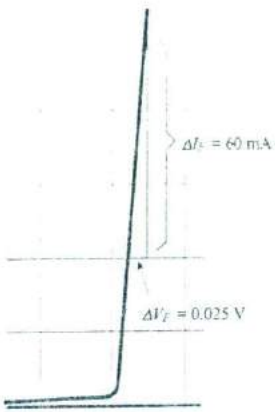


Figure 2-7
Determination of diode dynamic resistance from the forward characteristic.

The dynamic resistance can also be calculate from the equation,

$$r'_d = \frac{26\ \text{mV}}{I_F} \qquad \textbf{(2-2)}$$

where I_F is the *dc* forward current at the junction. Thus, for example, the dynamic resistance for a diode passing a 10 mA forward current is, r'_d = 26 mV/10 mA = 26 Ω.

Equation 2-2 shows that the diode dynamic resistance changes with the level of *dc* forward current. This is not shown in Figs. 2-4 and 2-5, so, the characteristics are approximations of the actual device characteristics. It should also be noted that Eq. 2-2 gives the *ac* resistance only for the junction. It does not include the *dc* resistance of the semiconductor material, which might be as large as 2 Ω depending on the design of the device. The resistance derived from the slope of the device characteristic does include the semiconductor *dc* resistance. So, r_d (from the characteristic) should be slightly larger than r'_d calculated from Eq. 2-2.

Example 2-2

Determine the dynamic resistance at a forward current of 70 mA for the diode characteristics given in Fig. 2-4. Also, use Eq. 2-2 to estimate the diode dynamic resistance.

Solution

at $I_F = 70$ mA, for $\Delta I_F = 60$ mA, $\Delta V_F \approx 0.025$ V

Eq. 2-1, $$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{0.025\text{ V}}{60\text{ mA}} \text{ (see Fig. 2-7)}$$

$$= 0.42\ \Omega$$

Eq. 2-2, $$r'_d = \frac{26\text{ mV}}{I_F} = \frac{26\text{ mV}}{70\text{ mA}}$$

$$= 0.37\ \Omega$$

Practise Problems

2-2.1 Calculate the resistances offered by a diode with the characteristics in Fig. 2.5, when the forward current is 60 mA, and when the reverse voltage is 30 V.

2-2.2 Determine the dynamic resistance at a 50 mA forward current for a diode with the characteristics in Fig. 2-5. Also, use Eq. 2-2 to estimate the diode dynamic resistance.

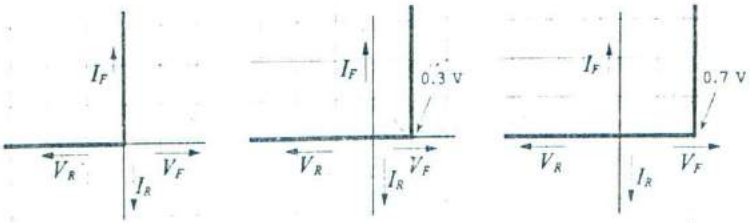
2-3 Diode Approximations

Ideal Diode Characteristics

As already discussed, a diode is essentially a one-way device, offering a low resistance when forward biased, and a high resistance when biased in reverse. An *ideal diode* (or perfect diode) would have zero forward resistance and zero forward voltage drop. It would also have an infinitely high reverse resistance, which would result in zero reverse current. Figure 2-8(a) shows the current/voltage characteristics of an ideal diode.

Although an ideal diode does not exist, there are many applications where diodes can be assumed to be near-ideal devices.

In circuits with supply voltages much larger than the diode forward voltage drop, V_F can be assumed constant without introducing any serious error. Also, the diode reverse current is normally so much smaller than the forward current that the reverse current can be ignored. These assumptions lead to the near-ideal, or approximate, characteristics for silicon and germanium diodes shown in Fig. 2-8(b) and (c). Example 2-3 investigates a situation where the diode V_F is assumed constant



(a) Ideal diode characteristics

(b) Approximate characteristics for a germanium diode

(c) Approximate characteristics for a silicon diode

Figure 2-8
An ideal diode has $V_F = 0$ and $I_R = 0$. Practical diodes can be treated as near-ideal devices if the forward voltage drop is taken into account.

Example 2-3

A silicon diode is used in the circuit shown in Fig. 2-9. Calculate the diode current.

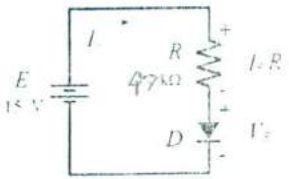


Figure 2-9
Circuit for Example 2-3.

Solution

$$E = I_F R_1 + V_F$$

or,

$$I_F = \frac{E - V_F}{R_1} = \frac{15\ \text{V} - 0.7\ \text{V}}{4.7\ \text{k}\Omega}$$

$$= 3.04\ \text{mA}$$

Piecewise Linear Characteristic

When the forward characteristic of a diode is not available, a straight-line approximation, called the *piecewise linear characteristic*, may be employed. To construct the piecewise linear characteristic, V_F is first marked on the horizontal axis, as shown in Fig. 2-10. Then, starting at V_F, a straight line is drawn with a slope equal to the diode dynamic resistance. Example 2-4 demonstrates the process.

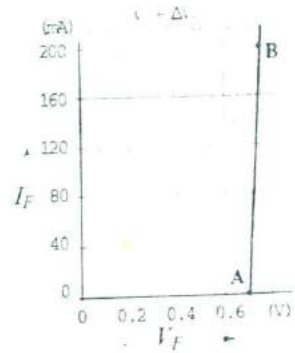


Figure 2-10
Diode piecewise linear characteristic, or straight-line approximation of the diode forward characteristic.

Example 2-4

Construct the piecewise-linear characteristic for a silicon diode that has a 0.25 Ω dynamic resistance and a 200 mA maximum forward current.

Solution

Plot point A on the horizontal axis at:

$V_f = 0.7$ V (see Fig. 2-10)

$$\Delta V_f = \Delta I_f \times r_d = 200 \text{ mA} \times 0.25\ \Omega$$
$$= 0.05 \text{ V}$$

Plot point B (on Fig. 2-10) at:

$$I_f = 200 \text{ mA and } V_f = (0.7 \text{ V} + 0.05 \text{ V})$$

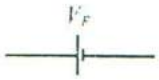
Draw the characteristic through points A and B.

dc Equivalent Circuits

An *equivalent circuit* for a device is a circuit that represents the device behaviour. Usually, the equivalent circuit is made up of a number of components, such as resistors and voltage cells. A diode equivalent circuit may be substituted in place of the device when investigating a circuit containing the diode. Equivalent circuits may also be used as device *models* in computer analysis of circuits.

In Example 2-3 a forward-biased diode is assumed to have a constant forward voltage drop (V_F) and negligible series resistance. In this case the *dc* equivalent circuit is assumed to be a voltage cell with a voltage V_F, [see Fig. 2-11(a)]. This simple *dc* equivalent circuit is quite suitable for a great many diode applications.

A more accurate equivalent circuit includes the diode dynamic resistance (r_d) in series with the voltage cell, as shown in Fig. 2-11(b). This takes account of the small variations in V_F that occur with change in forward current. An ideal diode is also included to show that curent flows only in one direction. The equivalent circuit without r_d assumes that the diode has the approximate characteristics illustrated in Fig. 2-8(b) or (c). With r_d included, the equivalent circuit represents a diode with the type of piecewise linear characteristic in Fig. 2-10. Consequently, the circuit in Fig. 2-11(b) is known as the *piecewise linear equivalent circuit.*



(a) Basic dc equivalent circuit



(b) Complete dc equivalent circuit

Figure 2-11
Dc equivalent circuits for a junction diode.

Example 2-5

Calculate I_f for the diode circuit in Fig. 2-12(a) assuming that the diode has $V_f = 0.7$ V and $r_d = 0$. Then, recalculate the current taking $r_d = 0.25\ \Omega$.

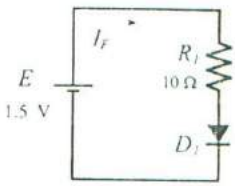
Solution

Substituting V_f as the diode equivalent circuit, [Fig 2-12(b)]:

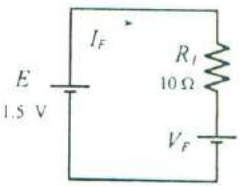
$$I_f = \frac{E - V_f}{R_1} = \frac{1.5 \text{ V} - 0.7 \text{ V}}{10\ \Omega}$$
$$= 80 \text{ mA}$$

Substituting V_f and r_d as the diode equivalent circuit, [Fig 2-12(c)]:

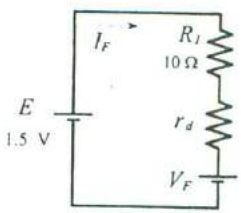
$$I_F = \frac{E - V_f}{R_1 + r_d} = \frac{1.5 \text{ V} - 0.7 \text{ V}}{10\ \Omega + 0.25\ \Omega}$$
$$= 78 \text{ mA}$$



(a) Diode circuit



(b) Diode replaced with voltage cell



(c) Diode replaced with r_d and V_F

Figure 2-12
Diode circuits for Example 2-5.

Practise Problems

2-3.1 Calculate the new level of diode current in the circuit in Fig. 2-9 when D_1 is replaced with two series-connected silicon diodes.

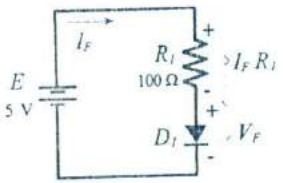
2-3.2 A germanium diode has a maximum forward current of 100 mA, and a 0.5 Ω dynamic resistance Construct the piecewise linear characteristics for this diode on Fig. 2-10.

2-3.3 Calculate the circuit current when the diode in Problem 2-3.2 is connected in series with a 15 Ω resistor and a 3 V battery which forward biased the diode.

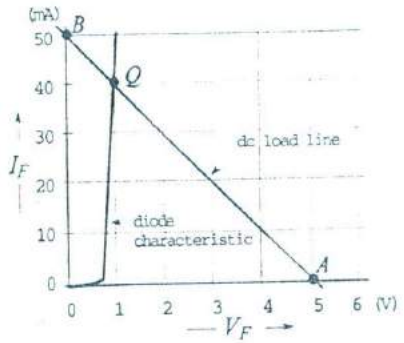
2-4 DC Load Line Analysis

DC Load line

Figure 2-13(a) shows a diode in series with a 100 Ω resistance (R_1) and a supply voltage (E). The polarity of E is such that the diode is forward biased, so a diode forward current (I_F) flows. As already discussed, the circuit current can be determined approximately by assuming a constant diode forward voltage drop (V_F). When the precise levels of the diode current and voltage must be calculated, *graphical analysis* (also termed *dc load line analysis*) is employed.



(a) Diode-resistor series circuit



(b) Plotting the dc load line on the diode characteristics

Figure 2-13
Drawing a dc load line on tl diode characteristic.

For graphical analysis, a *dc load line* is drawn on the diode forward characteristics, [Fig. 2-13(b)]. This is a straight line that illustrates all dc conditions that could exist within the circuit. Because the load line is always straight, it can be constructed by plotting any two corresponding current and voltage points and then drawing a straight line through them. To determine two points on the load line, an equation relating voltage, current,and resistance is first derived for the circuit. From Fig. 2-13(a),

$$E = (I_F R_1) + V_F \qquad (2\text{-}3)$$

Any convenient two levels of I_F can be substituted into Eq. 2-3 to calculate corresponding V_F levels, or vice versa. As demonstrated in Example 2-6, it is convenient to calculate V_F with $I_F = 0$, and to determine I_F when $V_F = 0$.

Example 2-6

Draw the dc load line for the circuit in Fig. 2-13(a). The diode forward characteristic is given in Fig. 2-13(b).

Solution

Substitute $I_f = 0$ into Eq. 2-3,

$$E = (I_f R_l) + V_f = 0 + V_f$$

or,

$$V_f = E = 5 \text{ V}$$

Plot point A on the diode characteristic at,

$$I_f = 0, \text{ and } V_f = 5 \text{ V}$$

Now substitute $V_f = 0$ into Eq. 2-3,

$$E = (I_f R_l) + 0$$

giving,

$$I_f = \frac{E}{R_l} = \frac{5 \text{ V}}{100 \ \Omega}$$

$$= 50 \text{ mA}$$

Plot point B on the diode characteristic at,

$$I_f = 50 \text{ mA, and } V_f = 0$$

Draw the dc load line through points A and B.

Q Point

The relationship between the diode forward voltage and current in the circuit in Fig. 2-13(a) is defined by the device characteristic. Consequently, there is only one point on the *dc* load line where the diode voltage and current are compatible with the circuit conditions. That is *point Q*, termed the *quiescent point* or *dc bias point*, where the load line intersects the characteristic. This may be checked by substituting the levels of I_F and V_F at point *Q* into Eq. 2-3. From the *Q* point on Fig. 2-13(b), $I_F = 40$ mA and $V_F = 1$ V. Equation 2-3 states that $E = (I_F R_l) + V_F$. Therefore,

$$E = (40 \text{ mA} \times 100 \ \Omega) + 1 \text{ V} = 5 \text{ V}$$

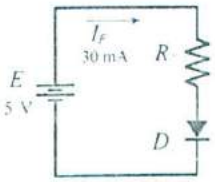
So, with $E = 5$ V and $R_l = 100 \ \Omega$, the only levels of I_F and V_F that can satisfy Eq. 2-3 on the diode characteristics in Fig. 2-13(b) are $I_F = 40$ mA and $V_F = 1$ V.

Note that, although $V_F = 0$ and $V_F = 5$ V were used when drawing the dc load line in Ex. 2-6, no functioning semiconductor diode would have such forward voltage drops. These are simply convenient theoretical levels for constructing the *dc* load line.

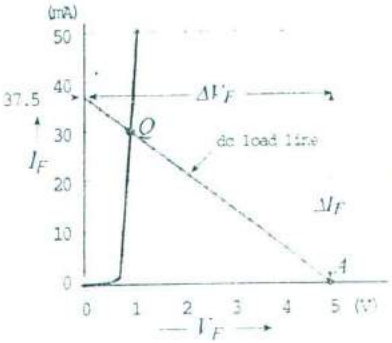
Calculating Load Resistance and Supply Voltage

In a diode series circuit [see Fig. 2-14(a)], resistor R_l dictates the slope of the *dc* load line, and supply voltage E determines point A on the load line. So, the circuit conditions can be altered by changing either R_l or E.

When designing a diode circuit, it may be required to use a given supply voltage and set up a specified forward current. In this case, points A and Q are first plotted and the load line is drawn. R_l is then calculated from the slope of the load line. The problem could also occur in another way. For example, R_l and the required I_F are known, and the required supply voltage is to be determined. This problem is solved by plotting point Q and drawing the load line with slope $1/R_l$. The supply voltage is then read at point A.



(a) Diode-resistor circuit



(b) Resistor determination

Figure 2-14
Determination of the series resistance from the slope of the dc load line.

Example 2-7

Determine the required load resistance for the circuit in Fig. 2-14(a) using the device characteristics in Fig. 2-14(b).

Solution

From Eq. 2-3, $V_l = E - (I_l R_l)$

Substituting $I_l = 0$, $V_l = E - 0 = 5$ V

Plot point A on the diode characteristic in Fig. 2-14(b) at,

$I_l = 0$, and $V_l = 5$ V

Now plot point Q in Fig. 2-14(b) at,

$I_l = 30$ mA

Draw the new dc load line through points A and Q.

From the load line,

$$R_l = \frac{\Delta V_l}{\Delta I_l} = \frac{5 \text{ V}}{37.5 \text{ mA}}$$

$$= 133\ \Omega$$

Example 2-8

Determine a new supply voltage for the circuit in Fig. 2-14(a) to give a 50 mA diode forward current when $R_l = 100\ \Omega$.

Solution

Plot point Q on the diode characteristic in Fig. 2-15 at,

$I_l = 50$ mA

and from the characteristic read,

$V_F = 1.1$ V

From Eq. 2-3, $V_F = E - (I_l R_l)$

When I_l *changes from 50 mA to 0,*

$\Delta I_l = 50$ mA (see Fig. 2-15)

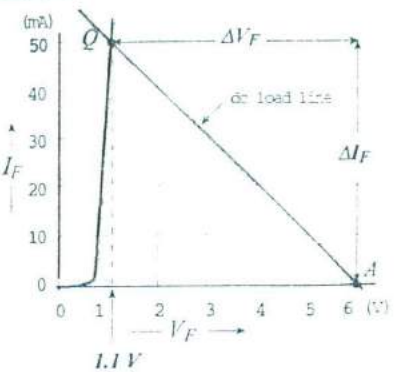


Figure 2-15
Determination of the supply voltage for a diode-resistor circuit.

and, $\Delta V_F = I_f R_1 = 50 \text{ mA} \times 100\ \Omega$ (see Fig. 2-15)
$= 5 \text{ V}$

The new level of E is, $E = V_f + \Delta V_F = 1.1 \text{ V} + 5 \text{ V}$
$= 6.1 \text{ V}$

Point A may now be plotted (on Fig. 2-15) at $I_f = 0$, and $E = 6.1$ V, and the new dc load line may be drawn through points A and Q.

Practise Problems

2-4.1 A diode with the characteristics in Fig. 2-15 is connected in series with a 3 V supply and a 100 Ω resistor. Draw the dc load line for the circuit, and determine the forward current level.

2-4.2 Calculate a new load resistance for the circuit in Problem 2-4.1 to produce a 40 mA diode forward current.

2-4.3 A diode with the characteristics in Fig. 2-15 is to have a 35 mA forward current when connected in series with a 70 Ω resistor. Determine the required supply voltage.

2-5 *Temperature Effects*

Diode Power Dissipation

The power dissipation in a diode is simply calculated as the device terminal voltage multiplied by the current level.

$$P = V_F I_F \qquad \textbf{(2-4)}$$

Device manufacturers specify a maximum power dissipation for each type of diode. If the specified level is exceeded, the device will overheat and it may short-circuit or open-circuit.

The maximum power that may be dissipated in a diode (or any other electronic device) is normally specified for an ambient temperature of 25°C, or sometimes for a 25°C case temperature. When the temperature exceeds the specified level, the device maximum power dissipation must be derated.

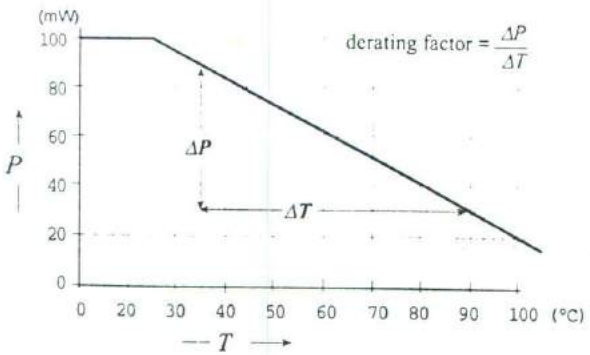


Figure 2-16
A power versus temperature graph shows how a device maximum power dissipation must be derated with increasing temperature.

Figure 2-16 shows the type of power-versus-temperature graph provided on some device data sheets. The maximum power dissipation for any given temperature can simply be read from the graph. Then, the maximum level of forward current is calculated from Eq. 2-4. Instead of a power-versus-temperature graph, the rectifier diode data sheet in Appendix 1-2 has a current-versus-temperature graph. This allows the maximum forward current at a desired temperature to be determined directly.

As an alternative to a power or current graph, a *derating factor* is sometimes listed on a device data sheet. As illustrated in Fig. 2-16, the derating factor defines the slope of the power-versus-temperature graph. It can be used to draw the graph, or employed directly without reference to the graph. The equation for the new maximum power dissipation when the temperature changes involves the specified power at the specified temperature (P_1 at T_1), the temperature change (ΔT), and the derating factor.

$$P_2 = (P_1 \text{ at } T_1) - [\Delta T \times (\textit{derating factor})] \qquad (2\text{-}5)$$

Example 2-9

A diode with a 700 mW maximum power dissipation at 25°C has a 5 mW/°C derating factor. If the forward voltage drop remains constant at 0.7 V, calculate the maximum forward current at 25°C and at 65°C temperatures.

Solution

At 25°C:

From Eq. 2-4,
$$I_f = \frac{P}{V_f} = \frac{700 \text{ mW}}{0.7 \text{ V}}$$
$$= 1 \text{ A}$$

At 65°C:

Eq. 2-5,
$$P_2 = (P_1 \text{ at } T_1) - [\Delta T \times (\textit{derating factor})]$$
$$= 700 \text{ mW} - [(65°\text{C} - 25°\text{C}) \times 5 \text{ mW/°C}]$$
$$= 500 \text{ mW}$$

From Eq. 2-4,
$$I_F = \frac{P_2}{V_f} = \frac{500 \text{ mW}}{0.7 \text{ V}}$$
$$= 714 \text{ mA}$$

Forward Voltage Drop

There are circumstances in which it is important to know the precise level of a diode forward voltage drop. In these cases, the graphical analysis techniques discussed in Section 2-4 may be appropriate. However, as explained in Section 1-6 and illustrated in Fig. 2-17, the voltage drop across a forward-biased *pn*-junction changes with temperature by approximately -1.8 mV/°C for a silicon device, and by -2.02 mV/°C for germanium. A diode V_F at any temperature can be calculated from a knowledge of V_F at the starting temperature (V_{F1} at T_1), the temperature change (ΔT), and the voltage/temperature coefficient (ΔV_F/°C).

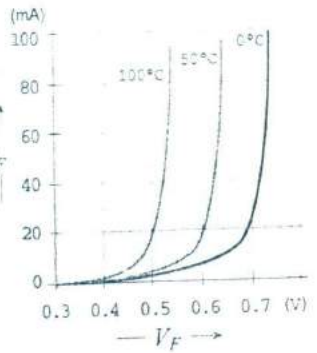


Figure 2-17
The forward voltage drop across a diode decreases as the device temperature increases.

$$V_{F2} = (V_{F1} \text{ at } T_1) + [\Delta T \times (\Delta V_F/^\circ C)] \qquad (2\text{-}6)$$

Dynamic Resistance

Equation 2-2 for calculating the dynamic resistance of a forward biased diode is correct only for 25°C junction temperatures. For higher or lower temperatures, the equation must be modified to,

$$r'_d = \frac{26 \text{ mV}}{I_F}\left[\frac{T + 273^\circ C}{298^\circ C}\right] \qquad (2\text{-}7)$$

where T is the junction temperature in degrees Celsius.

Example 2-10

A silicon diode with a 0.7 V forward voltage drop at 25°C is to be operated with a constant forward current up to a temperature of 100°C. Calculate the diode V_F at 100°C. Also, determine the junction dynamic resistance at 25°C and at 100 °C if the forward current is 26 mA.

Solution

Eq. 2-6, $V_{F2} = (V_{F1} \text{ at } T_1) + [\Delta T \times (\Delta V_F/^\circ C)]$

$= 0.7 \text{ V} + [(100^\circ C - 25^\circ C) \times (-1.8 \text{ mV}/^\circ C)]$

$= 0.565 \text{ V}$

at 25°C,

Eq. 2-7, $r'_d = \frac{26 \text{ mV}}{I_F}\left[\frac{T + 273^\circ C}{298^\circ C}\right]$

$= \frac{26 \text{ mV}}{26 \text{ mA}}\left[\frac{25^\circ C + 273^\circ C}{298^\circ C}\right]$

$= 1 \ \Omega$

at 100°C,

$r'_d = \frac{26 \text{ mV}}{26 \text{ mA}}\left[\frac{100^\circ C + 273^\circ C}{298^\circ C}\right]$

$= 1.25 \ \Omega$

Practise Problems

2-5.1 A diode with a constant 0.65 V forward drop has the power-versus-temperature graph in Fig. 2-16. Calculate the maximum forward current that may be passed at 25°C and at 80°C.

2-5.2 Calculate the maximum and minimum levels of V_F for a germanium diode with $V_F = 0.3$ V at 25°C when operated over a temperature range of 10°C to 80°C. Also, determine the junction dynamic resistances at the temperature extremes if I_F is 20 mA.

2-5.3 A diode with a 1 W maximum power dissipation at 25°C has a 4 mW/°C derating factor. Calculate the maximum power that may be dissipated in the diode when its temperature is 80°C.

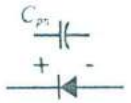
2-6 AC Equivalent Circuits

Junction Capacitances

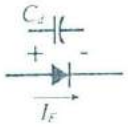
The depletion region of a *pn*-junction (see Section 1-5) is a layer depleted of charge carriers situated between two blocks of low resistance material. Because this is the description of a capacitor, the depletion region clearly has a capacitance. The *depletion layer capacitance* (C_{pn}) may be calculated from the equation for a parallel-plate capacitor if the junction dimensions are known. Typically, C_{pn} is 4 pF for a low-current diode.

The depletion layer capacitance is essentially the capacitance of a reverse-biased *pn*-junction. [Fig. 2-18(a)]. Consider the forward-biased junction in Fig. 2-18(b). If the applied voltage is suddenly reversed, forward current I_F ceases immediately leaving some majority charge carriers in the depletion region. These charge carriers must flow back out of the depletion region, which is widened when the junction is reverse biased. The result is that, when a forward-biased junction is suddenly reversed, a reverse current flows which is large initially and slowly decreases to the level of the reverse saturation current. The effect may be likened to the discharging of a capacitor, and so it is represented by a capacitance known as the *diffusion capacitance* (C_d).

It can be shown that C_d is proportional to the forward current I_F. This is to be expected, since the number of charge carriers in the depletion region must be directly proportional to I_F. For a low-current diode with a 10 mA forward current, a typical value of diffusion capacitance is around 1 nF.



(a) A depletion layer capacitance occurs at a reverse-biased diode

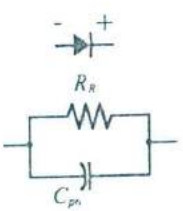


(b) A diffusion capacitance is present at a forward-biased diode

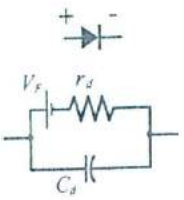
Figure 2-18
The capacitance of a diode depends upon the polarity of the applied voltage, and on the current level.

ac Equivalent Circuits (Reverse- and Forward-Biased)

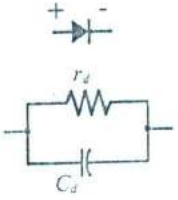
A reverse-biased diode can be simply represented by the (high non-constant) reverse resistance R_R in parallel with the depletion layer capacitance C_{pn}. [Fig. 2-19(a)]. The equivalent circuit for a forward-biased diode consists of the dynamic resistance r_d in series with a voltage cell representing V_F, as discussed in Section 2-3. To allow for the effect of the diffusion capacitance, C_d is included in parallel. This gives the complete equivalent circuit shown in Fig. 2-19(b).



(a) Equivalent circuit for a reverse-biased diode



(b) Equivalent circuit for a forward-biase diode



(c) AC equivalent circuit for a forward-biased diode

Figure 2-19
Equivalent circuits for reverse-biased and forward biased diodes.

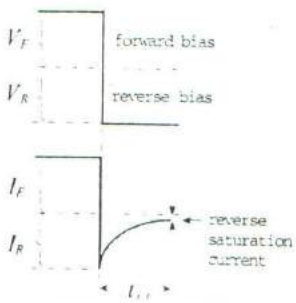
The equivalent circuit for the forward-biased diode may be modified to form an *ac equivalent circuit*. This applies to diodes that are maintained in a forward-biased condition while subjected to small variations in I_F and V_F. The ac equivalent circuit is created simply by removing the voltage cell representing V_F from the complete equivalent circuit. [see Fig. 2-19(c)].

Reverse Recovery Time

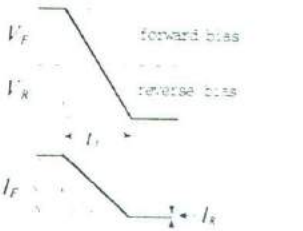
In many applications, diodes must switch rapidly between forward and reverse bias. Most diodes switch very quickly into the forward-biased condition, however, there is a longer *turn-off* time due to the junction diffusion capacitance.

Figure 2-20 illustrates the effect of a voltage pulse on the diode forward current. When the pulse switches from positive to negative, the diode conducts in reverse instead of switching *off* sharply. [Fig. 2-20(a)]. The reverse current (I_R) initially equals the forward current (I_F). then it gradually decreases toward zero. The high level of reverse current occurs because at the instant of reverse bias there are charge carriers crossing the junction depletion region, and these must be removed. (The same effect that produces diffusion capacitance.) The *reverse recovery time* (t_{rr}) is the time required for the current to decrease to the reverse saturation current level. Typical values of t_{rr} for switching diodes range from 4 ns to 50 ns. Figure 2-20(b) shows that, to keep the diode reverse current to a minimum, the *fall time* (t_f) of the applied voltage pulse must be much larger than the diode t_{rr}. Typically,

$$t_{f(min)} = 10\ t_{rr} \qquad (2\text{-}8)$$



(a) Effect of instantaneous reverse bias



(b) Effect of $t_f >> t_{rr}$

Figure 2-20
The minimum on-off switching time of a diode is limited by the reverse recovery time.

Example 2-11

Calculate the minimum fall time for voltage pulses applied to *1N915* and *1N917* diodes.

Solution

From the diode data sheet in Appendix 1-1,

t_{rr} = 10 ns *for the 1N915, and* t_{rr} = 3 ns *for the 1N917*

For the 1N915,
Eq. 2-8,
$$t_{f(min)} = 10\ t_{rr} = 10 \times 10 \text{ ns} = 100 \text{ ns}$$

For the 1N917,
Eq. 2-8,
$$t_{f(min)} = 10\ t_{rr} = 10 \times 3 \text{ ns} = 30 \text{ ns}$$

Practise Problems

2-6.1 Determine the maximum reverse recovery time for a diode with an applied voltage pulse that has a 0.5 μs fall-time.

2-6.2 Estimate a suitable minimum fall time for switching a diode from *on* to *off* if the diode has t_{rr} = 15 ns.

2-7 *Diode Specifications*

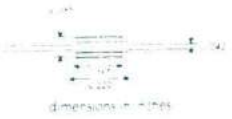
Diode Data Sheets

To select a suitable diode for a particular application, the *data sheets*, or *specifications*, provided by device manufacturers must be consulted. Portions of typical diode data sheets are shown in Fig. 2-21 and in Appendices 1-1 through 1-3.

Most data sheets start off with the device type number at the top of the page, such as *1N914 through 1N917*, or *1N5391 through 1N5399*. The *1 (one)* in the type number signifies a one-junction device; a diode. A short descriptive title follows the type number; for example, *silicon switching diode*, or *silicon rectifier*. *Mechanical data* is also given, usually in the form of an illustration showing the package shape and dimensions. The *maximum ratings* at 25°C are then listed, (see Fig. 2-21).

Type 1N914 Through 1N917 Silicon Switching Diodes

mechanical data



absolute maximum ratings at 25°C ambient temperature

	1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
V_R Reverse Voltage	75	75	75	50	75	75	75	30	V
I_O Average Rectified Forward Current	75	75	75	75	75	75	75	50	mA
I_{FRM} Repetitive Peak Forward Current	225	225	225	225	225	225	225	150	mA
P Power Dissipation	250	250	250	250	250	250	250	250	mW

Figure 2-21
Portion of data sheet for 1N914 through 1N917 diodes.

The maximum ratings are the maximum voltages, currents, etc., that can be applied without destroying the device. It is very important that these ratings not be exceeded, otherwise failure of the diode is quite likely. *For reliability, the maximum ratings should not even be approached.* If a diode is to survive a 50 V reverse bias, one that has a 75 V peak reverse voltage should be selected. If the diode peak forward current is to be 100 mA, use a device that can handle 150 mA. It also is important to note that the maximum ratings must be adjusted downward for operation at temperatures greater than 25°C, (see Section 2-5).

A list of other electrical characteristics for the device normally follows the maximum ratings. An understanding of all the parameters specified on a data sheet will not be achieved until the data sheets have been consulted frequently. However, some of the most important parameters are considered below:

V_R or V_{RRM} *Peak reverse voltage*, (also termed *peak inverse voltage*, and *DC blocking voltage*). This is the maximum reverse voltage that may be applied across the diode.

I_o or $I_{F(AV)}$ — *Steady-state forward current.* The maximum current that may be passed continuously through the diode.

I_{FSM} — *Non-repetitive peak surge current.* This current may be passed for a specified time period. The surge current is very much higher than the normal maximum forward current. It is a current that may be allowed flow briefly when a circuit is first switched *on*.

I_{FRM} — *Repetitive peak surge current.* Peak current that may be repeated over and over again: for example, during each cycle of a rectified waveform.

V_F — Static forward voltage drop. The maximum forward volt drop for a given forward current and device temperature.

P — Continuous power dissipation at 25°C. The maximum power that the device can safely dissipate continuously in free air. This rating must be downgraded at higher temperatures (see Section 2-5).

Low-Power Diodes

The data sheet portion in Fig. 2-21 identifies the *1N914* to *1N917* devices as *switching diodes*. The average rectified forward current is listed as 75 mA (except for the *1N917*). Maximum reverse voltage ranges from 30 V to 75 V. Thus, these diodes are intended for relatively low-current, low-voltage applications, in which they may be required to switch rapidly between the *on* and *off* states.

Rectifier Diodes

Appendices 1-2 and 1-3 shows data sheets for low-power rectifiers. It is seen that the *1N4000* range of rectifiers can pass an average forward current of 1 A, and that the *1N5390* range can pass 1.5 A. Both types have maximum reverse voltages ranging from 50 V to 1000 V. Unlike the case of the switching diodes specified in Appendix 1-1, the reverse recovery time is not listed on the rectifier data sheet. Rectifier diodes are generally intended for low-frequency applications (60 Hz to perhaps 400 Hz) in which switching time is not important, (see Sections 3-1 and 3-2).

Example 2-12

Referring to Fig. 2-21, determine the following quantities for a *1N915* diode: peak reverse voltage, steady-stage forward current, peak repetitive forward current, power dissipation.

Solution

For the 1N915,

$$PIV = V_R = 50\text{ V}$$
$$I_o = 75\text{ mA}$$
$$I_{FRM} = 225\text{ mA}$$
$$P = 250\text{ mW}$$

Practise Problems

2-7.1 Referring to Appendix 1-3, determine the following quantities for a *1N5397* diode: peak reverse voltage, steady-stage forward current, nonrepetitive forward current.

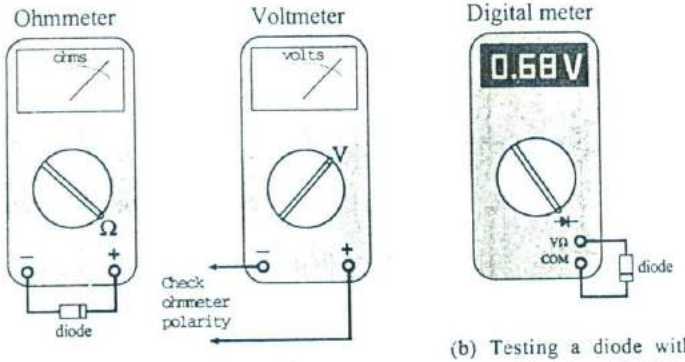
2-7.2 A rectifier has to pass an average current of 600 mA, and survive a repetitive reverse voltage of 75 V. Select a suitable diode from Appendices 1-1 and 1-3.

2-8 Diode Testing

Ohmmeter Tests

Several methods are available for testing diodes. One of the simplest and quickest tests can be made using an ohmmeter to measure the forward and reverse resistance of a diode, [see Fig. 2-22(a)]. The diode should offer a low resistance when forward biased, and a high resistance when reverse biased. A diode is short-circuited when it displays a low resistance for both forward and reverse bias. If a high resistance is measured with both bias polarities, the device is open-circuited. Usually, the actual indicated high resistance is approximately half the selected ohmmeter range.

Obviously, the ohmmeter test will identify the anode and cathode of a diode, if there is doubt about the diode terminals. However, it is very important to note that *when some multifunction instruments are used as ohmmeters, the voltage polarity at the terminals may* **not** *be the same as the polarity marked on the instrument.* A voltmeter should be used, as illustrated in Fig. 2-22(a), to check the ohmmeter terminal polarity.



(a) Testing a diode with an ohmmeter

(b) Testing a diode with a digital multimeter

Figure 2-22
Analog or digital multimeters may be used for diode testing.

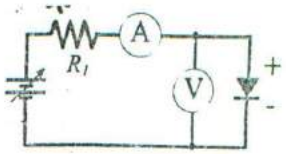
Use of a Digital Meter

Many portable multifunction digital instruments have a diode testing facility which displays the diode forward voltage when the terminals are connected *positive* to the anode, *negative* to the

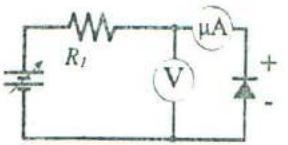
cathode [Fig. 2-22(b)]. When reverse connected, a functioning diode produces an *OL* display. If an *OL* display occurs with both forward and reverse connections, the diode is open-circuited. When the display is *000*, the device is short-circuited.

Diode Characteristics Plotting

The forward characteristics of a diode can be obtained by use of the circuit illustrated in Fig. 2-23(a). The diode voltage is set at a series of convenient levels, and the corresponding current levels are measured and recorded. The characteristics are then plotted from the table of quantities obtained in this way. The reverse characteristics can be obtained in the same way, except that a very sensitive microammeter is required to measure the diode reverse current, [Fig. 2-23(b)]. The microammeter must be connected directly in series with the diode, as shown; otherwise the voltmeter current may introduce a serious error.



(a) Circuit for obtaining diode forward charactertistics



(b) Circuit for obtaining diode reverse charactertistics

Figure 2-23
Diode characteristics can be plotted from a table of corresponding current and voltage measurements

Figure 2-24 shows a method of using an *XY recorder* for drawing the forward characteristics of a diode. The resistor voltage (V_{R1}) is directly proportional to the diode forward current (I_F). So, V_{R1} is applied to the vertical input terminals of the *XY* recorder, as illustrated. The diode forward voltage (V_F) goes to the horizontal input terminals. When the power supply voltage is slowly increased from zero, the diode forward characteristic is traced out by the pen on the *XY* recorder.

If R_1 in Fig. 2-24 is a 1 kΩ resistor, there is a 1 V drop across R_1 for every 1 mA of diode current. Therefore, with the vertical scale of the *XY* recorder set to 1 V/cm, the (vertical) current co-ordinate of the graph is 1 mA/cm. A convenient scale for the (horizontal) voltage co-ordinate is 0.1 V/cm. Diodes can also be investigated by means of a *curve tracer* which displays the device characteristics on oscilloscope-type screen.

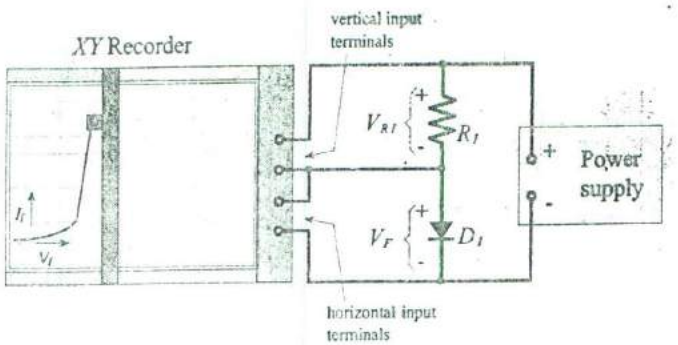


Figure 2-24
An XY-recorder can be used for directly plotting diode characteristics.

Example 2-13

The arrangement shown in Fig. 2-24 is to be used to plot the characteristics of a 1N914 diode. Select resistor R_1, and determine appropriate V/cm scales for the *XY* recorder.

Solution

From Fig. 2-21, $I_o = 75$ mA *(for the 1N914)*

Select a vertical scale of 5 mA/cm for the characteristic to give,

$$\text{vertical scale length (for } I_F) = \frac{75 \text{ mA}}{5 \text{ mA/cm}} = 15 \text{ cm}$$

Select a vertical scale of 1 V/cm for the XY recorder, so that 15 cm represents 15 V, as well as 75 mA.

$$R_1 = \frac{15 \text{ V}}{75 \text{ mA}} = 200 \ \Omega$$

and,

$$P_{R1(max)} = [I_{F(max)}]^2 R_1 = (75 \text{ mA})^2 \times 200 \ \Omega = 1.1 \text{ W}$$

V_F might be as large as 0.8 V, so select a horizontal scale of 0.1 V/cm to give,

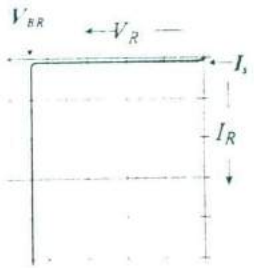
$$\text{horizontal scale length (for } V_f) = \frac{0.8 \text{ V}}{0.1 \text{ V/cm}} = 8 \text{ cm}$$

Practise Problems

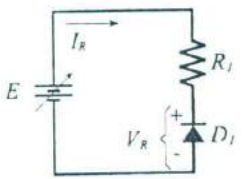
2-8.1 Plot the forward characteristics for a silicon diode from the following experimental data:

V_F (V)	0.6	0.62	0.64	0.66	0.68	0.7	0.72	0.74	0.76
I_F (mA)	1	1.4	1.8	2.5	10	50	90	130	170

2-8.2 An XY recorder is used, as in Fig. 2-24, to plot silicon diode forward characteristics to approximately fill a 10 cm by 10 cm square. If the maximum forward current is to be 100 mA, select suitable V/cm scales for the recorder, and a suitable resistance for R_1.



(a) Diode reverse characteristic



(b) Diode-resistor circuit

Figure 2-25
A diode can be operated in reverse breakdown if the current is limited by means of a series-connected resistor.

2-9 Zener Diodes

Junction Breakdown

When a junction diode is reverse biased, normally only a very small reverse saturation current flows; I_S on the reverse characteristic in Fig. 2-25(a). When the reverse voltage is sufficiently increased, the junction *breaks down* and a large reverse current flows. If the reverse current is limited by means of a suitable series resistor, [R_1 in the circuit in Fig. 2-25(b)], the power dissipation in the junction can be kept to a level that will not destroy the device. In this case, the diode may be operated continuously in reverse breakdown. The reverse current returns to its normal level when the voltage is reduced below the reverse breakdown level.

Diodes designed for operation in reverse breakdown are found to have a breakdown voltage that remains extremely stable over a

wide range of current levels. This property gives the *breakdown diode* many useful applications as a voltage reference source.

There are two mechanisms that cause breakdown in a reverse biased *pn*-junction. With a very narrow depletion region, the electric field strength (volts/width) produced by a reverse bias voltage can be very high. The high intensity electric field causes electrons to break away from their atoms, thus converting the depletion region from an insulating material into a conductor. This is *ionization by electric field*, also called *Zener breakdown*, and it usually occurs with reverse bias voltages less than 5 V.

In cases where the depletion region is too wide for Zener breakdown, the electrons in the reverse saturation current can be given sufficient energy to cause other electrons to break free when they strike atoms within the depletion region. This is termed *ionization by collision*. The electrons released in this way collide with other atoms to produce more free electrons in an *avalanche* effect. *Avalanche breakdown* is normally produced by reverse voltage levels above 5 V. Although *Zener* and *avalanche* are two different types of breakdown, the name *Zener diode* is commonly applied to all breakdown diodes.

Circuit Symbol and Package

The circuit symbol for a Zener diode in Fig. 2-26(a) is the same as that for an ordinary diode, but with the cathode bar approximately in the shape of a letter *Z*. The arrowhead on the symbol still points in the (conventional) direction of forward current when the device is forward biased. As illustrated, for operation in reverse bias, the voltage drop (V_Z) is + on the cathode, - on the anode.

Low-power Zener diodes are available in a variety of packages. For the device package shown in Fig. 2-26(b), the colored band identifies the cathode terminal, as in the case of an ordinary low-current diode. High-current Zener diodes are also available in the type of package that allows for mounting on a heat sink.

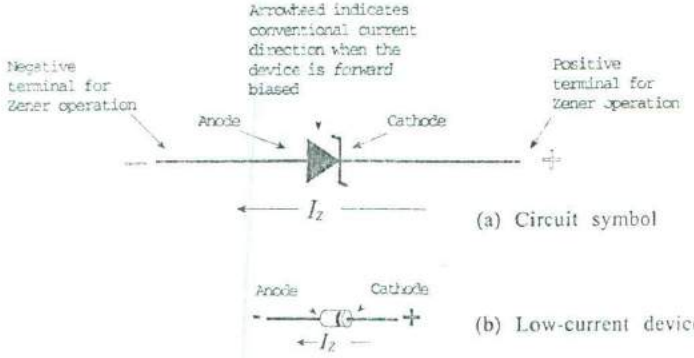


Figure 2-26
Zener diode circuit symbol and low-current zener diode package.

Characteristics and Parameters

The typical characteristics of a Zener diode are shown in detail in Fig. 2-27. Note that the forward characteristic is simply that of an

ordinary forward-biased diode. Some important points on the reverse characteristic are:

- V_Z — *Zener breakdown voltage*
- I_{ZT} — *Test current* for measuring V_Z
- I_{ZK} — Reverse current near the *knee* of the characteristic; the *minimum reverse current* to sustain breakdown
- I_{ZM} — *Maximum Zener current:* limited by the maximum power dissipation.

The *dynamic impedance* (Z_Z) is another important parameter that may be derived from the characteristics. As illustrated in Fig. 2-27, Z_Z defines how V_Z changes with variations in diode reverse current. When measured at I_{ZT}, the dynamic impedance is designated (Z_{ZT}). The dynamic impedance measured at the knee of the characteristic (Z_{ZK}) is substantially larger than Z_{ZT}.

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} \qquad \textbf{(2-9)}$$

The Zener diode current may be any level between I_{ZK} and I_{ZM}. For greatest voltage stability, the diode is normally operated at the test current. Many low-power Zener diodes have a test current specified as 20 mA, however, some devices have lower test currents.

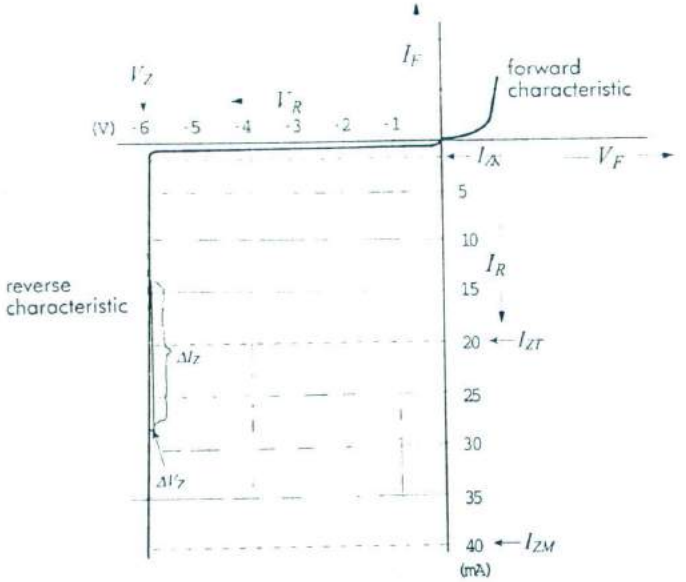


Figure 2-27
Typical characteristics for a Zener diode. The most important parameters are: the Zener voltage V_Z, the knee current I_{ZK}, the test current I_{ZT}, and the maximum current I_{ZM}.

Data Sheet

Portions of a data sheet for low-power Zener diodes with voltages ranging from 3.3 V to 12 V is shown in Fig. 2-28. (A data sheet for 2.4 V to 110 V Zener diodes is presented in Appendix 1-4.) Note in Fig. 2-28 that the V_Z tolerance is ±5% or ±10%. This means, for example, that for a *1N753* with a ±10% tolerance the actual V_Z level is 6.3 V ±10%, or 5.67 V to 6.93 V. The Zener voltage remains

stable at whatever it happens to be within this range.

The data sheet also lists the dynamic impedance, reverse leakage current, and the temperature coefficient for the V_Z of each device. The Zener voltages at any temperature can be calculated from,

$$V_{Z2} = (V_{Z1} \text{ at } T_1) + [\Delta T\, \alpha_Z\, V_Z/100)] \qquad \textbf{(2-10)}$$

Temperature compensated Zener diodes are also available with extremely low temperature coefficients.

Type 1N746 Through 1N759 Silicon Zener Diodes

3.3 V to 12 V (±5% or ±10%)
P_D = 400 mW (derate linearly above 50°C at 3.2 mW/°C)

electrical characteristics at 25°C ambient temperature

Type number	Nominal Zener voltage V_Z (V)	Test current I_Z (mA)	Zener impedance Z_{ZT} (Ω)	leakage current i_R (μA)	Reverse Temperature coefficient α_Z (%/°C)
1N746	3.3	20	28	10	-0.062
1N747	3.6	20	24	10	-0.055
1N753	6.2	20	7	0.1	+0.022
1N755	7.5	20	6	0.1	+0.045
1N757	9.1	20	10	0.1	+0.056
1N759	12.0	20	30	0.1	+0.060

Figure 2-28
Portions of a data sheet for low-power Zener diodes.

Low-power Zener diodes are typically limited to a maximum power dissipation of 400 mW, (P_D in Fig. 2-28). Higher-power devices are available. All of the power dissipations must be derated with temperature increase, exactly as explained in Section 2-5. When the maximum Zener current is not listed on the device data sheet, it may be calculated from the power dissipation equation.

$$P_D = V_Z \times I_{ZM} \qquad \textbf{(2-11)}$$

Example 2-14

Calculate the maximum current that may be allowed to flow through a *1N755* Zener diode at device temperatures of 50°C and 100 °C.

Solution

From the data sheet in Fig. 2-28, the 1N755 Zener diode has,

V_Z = 7.5 V, P_D = 400 mW at 50°C, and the derating factor = 3.2 mW/°C

At 50°C:

From Eq. 2-11,
$$I_{ZM} = \frac{P_D}{V_Z} = \frac{400 \text{ mW}}{7.5 \text{ V}}$$
$$= 53.3 \text{ mA}$$

At 100°C:

Eq. 2-5,
$$P_2 = (P_1 \text{ at } T_1) - [\Delta T \times (\text{derating factor})]$$
$$= 400 \text{ mW} - [(100°C - 50°C) \times 3.2 \text{ mW/°C}]$$
$$= 240 \text{ mW}$$

From Eq. 2-11,

$$I_{ZM} = \frac{P_Z}{V_Z} = \frac{240\ \text{mW}}{7.5\ \text{V}}$$

$$= 32\ \text{mA}$$

Example 2-15

The Zener diode circuit in Fig. 2-29 has $E = 20$ V, $R_1 = 620\ \Omega$, and a *1N755* Zener diode. Calculate the diode current and power dissipation.

Solution

From the data sheet in Fig. 2-28, the 1N755 Zener diode has, $V_Z = 7.5$ V

$$V_{R1} = E - V_Z = 20\ \text{V} - 7.5\ \text{V}$$
$$= 12.5\ \text{V}$$

$$I_Z = I_{R1} = \frac{V_{R1}}{R_1} = \frac{12.5\ \text{V}}{620\ \Omega}$$

$$= 20.16\ \text{mA}$$

$$P_D = V_Z\ I_Z = 7.5\ \text{V} \times 20.16\ \text{mA}$$
$$= 151\ \text{mW}$$

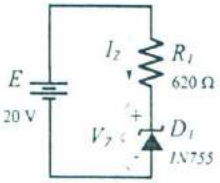


Figure 2-29
Circuit for Example 2-15

Equivalent Circuit

The *dc* equivalent circuit for a Zener diode is simply a voltage cell with a voltage V_Z, as in Fig. 2-30(a). This is the complete equivalent circuit for the device for all dc calculations. For the ac equivalent circuit [Fig. 2-30(b)], the dynamic impedance is included in series with the voltages cell. The *ac* equivalent circuit is used in situations where the Zener current is varied by small amounts. It must be understood that *these equivalent circuits apply only when the Zener diode is maintained in reverse breakdown.* If the device becomes forward biased, then the equivalent circuit for a forward-biased diode must be used.



(a) *dc* eqivalent circuit



(b) *ac* eqivalent circuit

Figure 2-30
Equivalent circuits for a Zener diode.

Example 2-16

A Zener diode with $V_Z = 4.3$ V has $Z_Z = 22\ \Omega$ at $I_Z = 20$ mA. Calculate the upper and lower limits of V_Z when I_Z changes by ±5 mA.

Solution

$$\Delta V_Z = \pm(\Delta I_Z \times Z_Z) = \pm(5\ \text{mA} \times 22\ \Omega)$$
$$= \pm 110\ \text{mV}$$

$$V_{Z(max)} = V_Z + \Delta V_Z = 4.3\ \text{V} + 110\ \text{mV}$$
$$= 4.41\ \text{V}$$

$$V_{Z(min)} = V_Z - \Delta V_Z = 4.3\ \text{V} - 110\ \text{mV}$$
$$= 4.19\ \text{V}$$

Practise Problems

2-9.1 Calculate the maximum current for a 1N753 Zener diode at device temperatures of 50°C and 100 °C.

2-9.2 A 1N749 Zener diode is connected in series with a resistor $R_1 = 820$ Ω, and a supply voltage $E = 12$ V. Calculate the diode current and power dissipation.

Chapter-2 Review Questions

Section 2-1

2-1 Sketch the symbol for a semiconductor diode, labelling the anode and cathode, and showing the polarity and current direction for forward bias. Also, show the direction of movement of charge carriers when the device is (a) forward biased, (b) reverse biased.

2-2 Draw sketches to show the appearance of low-current and medium-current diodes, and show how the cathode is identified in each case.

Section 2-2

2-3 Sketch typical forward and reverse characteristics for a germanium diode and for a silicon diode. Discuss the characteristics, and compare silicon and germanium diodes.

2-4 For diodes, define: forward voltage drop, maximum forward current, dynamic resistance, reverse saturation current, and reverse breakdown voltage.

2-5 Show how the diode dynamic resistance can be determined from the forward characteristics. Also, write an equation for calculating the dynamic resistance from *dc* forward current.

Section 2-3

2-6 Sketch the characteristics for an ideal diode, and approximate characteristics for practical diodes. Briefly explain each characteristic.

2-7 Draw the *dc* equivalent circuit for a diode and the piecewise linear equivalent circuit. Discuss the application of each.

Section 2-4

2-8 Explain the purpose of a dc load line. Write the equation for drawing a dc load line for a series circuit consisting of a supply voltage (E), a resistor (R_1), and a diode (D_1).

2-9 Define the Q point in a diode circuit, and explain how it is related to the diode characteristics and the dc load line.

Section 2-5

2-10 Sketch and explain a power-versus-temperature graph for a diode. Define the power derating factor for a diode.

2-11 Discuss how temperature change affects diode forward voltage drop.

Section 2-6

2-12 Explain the origins of depletion layer capacitance and diffusion capacitance, and discuss the importance of each.

2-13 Sketch the complete equivalent circuits for forward-biased and reverse-biased diodes. Also, sketch the ac equivalent circuit for a forward-biased diode. Briefly explain each circuit.

2-14 Define reverse recovery time. Sketch waveforms to show the effect of reverse recovery time on a diode switched rapidly from *on* to *off*. Explain each waveform.

Section 2-7

2-15 Discuss the major differences between switching diodes and rectifier diodes.

2-16 Define the following diode quantities: peak reverse voltage, repetitive peak surge current, steady-state forward current.

Section 2-8

2-17 Describe how an ohmmeter may be used for diode testing.

2-18 Sketch circuits for obtaining diode forward and reverse characteristics by measuring corresponding current and voltage levels. Explain.

2-19 Draw a sketch to show how the forward characteristics of a diode may be plotted on an *XY* recorder.

Section 2-9

2-20 Discuss the different types of junction breakdown that can occur in a reverse-biased diode. Sketch the circuit symbol for a Zener diode, and briefly explain its operation.

2-21 Sketch typical characteristics for a Zener diode. Explain the shape of the characteristics, and identify the important points.

2-22 Sketch the equivalent circuit for a Zener diode. Briefly explain.

Chapter-2 Problems

Section 2-2

2-1 Calculate the static forward resistance for the characteristics in Fig. 2-31 at a 200 mA forward current. Also, determine the reverse resistance at a 75 V reverse voltage.

2-2 Determine the dynamic resistance at a 150 mA forward current for a diode with the characteristics Fig. 2-31.

2-3 Calculate the static forward resistance for the characteristics in Fig. 2-32 at a 25 mA forward current. Also, determine the dynamic resistance for the device at I_F = 25 mA, using the characteristic and using Eq. 2-2.

Section 2-3

2-4 Calculate the forward current in a circuit consisting of a germanium diode connected in series with a 9 V battery and a 3.3 kΩ resistor.

2-5 A silicon diode in series with a 2.7 kΩ resistor and a battery is to have I_F = 1.96 mA. Calculate the battery voltage.

2-6 Draw the piecewise linear characteristics for a silicon diode with a 0.6 Ω dynamic resistance and a 75 mA maximum forward current.

2-7 Draw a straight-line approximation of the forward characteristic for a silicon diode that has a 0.5 Ω dynamic resistance and a maximum forward current of 300 mA.

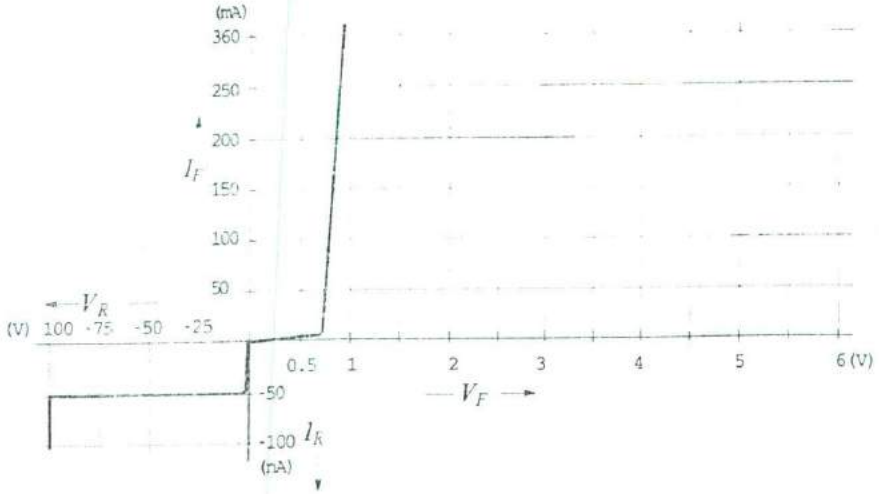


Figure 2-31

Section 2-4

2-8 A diode with the characteristics in Fig. 2-13(b) is to pass a 35 mA current from a 5.5 V supply. Draw the dc load line and calculate the required series resistance value. Determine the new current level when the supply is reduced to 3.5 V.

2-9 A diode with the forward characteristic in Fig. 2-31 is connected in series with a 30 Ω resistance and a 6 V supply. Determine the diode current, and find the new current when the resistance is changed to 20 Ω.

2-10 A diode which has the characteristics shown in Fig. 2-32 is to pass a 20 mA forward current when the supply is 12 V. Determine the value of resistance that must be connected in series with the diode.

2-11 Calculate the new level of supply voltage for the circuit in Problem 2-10 to give a 15 mA current level.

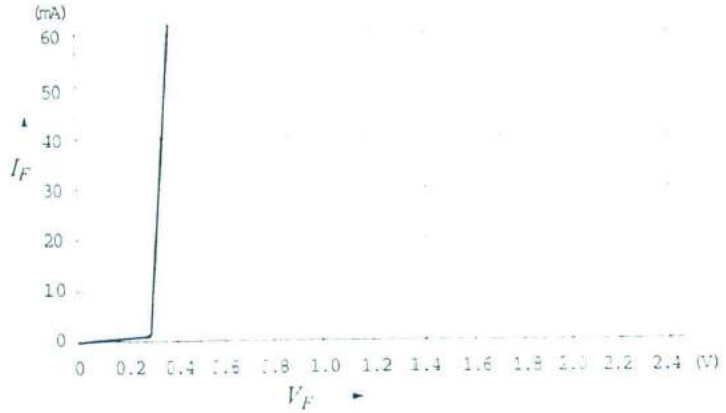


Figure 2-32

Section 2-5

2-12 A diode with a maximum power dissipation of 1000 mW at 25°C is to pass an average forward current of 500 mA. The forward voltage drop for the device is 0.8 V, and the power derating factor is 10 mW/°C. Calculate the maximum temperature at which the diode may be safely operated.

2-13 The diode specified in Problem 2-12 is to be operated at a temperature of 75°C. Calculate the maximum level of average forward current that the diode can safely pass.

2-14 Draw the power dissipation-versus-temperature graph for the diode specified in Problem 2-12.

2-15 A diode with a 0.9 V forward drop has a 1.5 W maximum power dissipation at 25°C. If the device derating factor is 7.5 mW/°C, calculate the maximum forward current level at 25°C and at 75°C. Assume that V_F remains constant.

2-16 Estimate the forward voltage drop at 75°C of the silicon diode in Problem 2-15. Determine the junction dynamic resistances at the temperature extremes if I_F is 20 mA.

2-17 A 5 V supply is applied via a 150 Ω resistor to a silicon diode and a germanium diode which are connected in series. Determine the diode current at 25°C and at 100°C.

Section 2-6

2-18 Calculate the minimum fall time for a voltage pulse applied to a diode with a reverse recovery time of (a) 6 ns, (b) 50 ns.

2-19 A diode has an applied voltage with a 200 ns fall time. Determine the maximum reverse recovery time for the diode.

2-20 Calculate a suitable minimum fall time for a switching waveform applied to a diode which has a 12 ns reverse recovery time.

2-21 Calculate the minimum fall time for a voltage pulse applied to a *1N914* diode.

Section 2-7

2-22 A diode connected in series with a 560 Ω resistor has a supply voltage that alternates between peak levels of +150 V and -150 V. Select a suitable device from the data sheets in Appendices 1-1 and 1-2.

2-23 Referring to Appendix 1-3, determine the peak reverse voltage and average rectified forward current for a *1N5398* diode.

2-24 A rectifier diode has to pass an average current of 55 mA and survive a 40 V peak reverse voltage. Select a suitable device from Appendices 1-1 through 1-3.

Section 2-8

2-25 The circuit shown in Fig. 2-24 is to be used to plot the forward characteristics of a *1N917* diode. Determine the resistance value for R_l, and select appropriate V/cm scales for the horizontal and vertical inputs of the *XY* recorder. The graph size should be approximately 20 cm x 20 cm.

2-26 Plot the forward characteristics of a diode from the following experimental data:

V_F (V)	0.24	0.26	0.28	0.29	0.30	0.31	0.32	0.33	0.34
I_F (mA)	0.05	0.07	0.09	0.5	0.9	20	40	60	80

Section 2-9

2-27 Determine the maximum current that may be used with a *1N757* Zener diode at temperatures of 25°C and 80°C.

2-28 A *1N750* Zener diode is connected in series with an 470 Ω resistor and a 10 V supply voltage. Calculate the diode current and power dissipation.

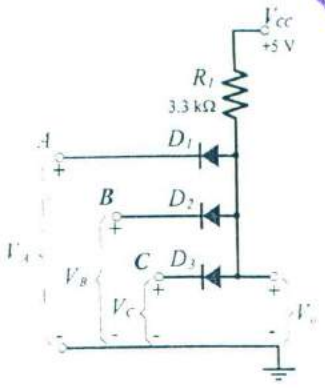
Practise Problem Answers

2-2.1 5.5 Ω, 30 MΩ
2-2.2 0.5 Ω, 0.5 Ω
2-3.1 2.89 mA
2-3.2 (Point *A:* 0 mA, 0.3 V),
(Point *B:* 100 mA, 0.35 V)
2-3.3 174 mA
2-4.1 20 mA
2-4.2 50 Ω
2-4.3 3.45 V
2-5.1 154 mA, 61.5 mA
2-5.2 267 mV, 421 mV, 1.23 Ω, 1.54 Ω
2-5.3 780 mV
2-6.1 50 ns
2-6.2 150 ns
2-7.1 600 V, 1.5 A, 50 A
2-7.2 *1N5392*
2-8.2 Vertical 1 V/cm, Horizontal 0.1 V/cm, 100 Ω
2-9.1 64.5 mA, 38.7 mA
2-9.2 40.4 mW

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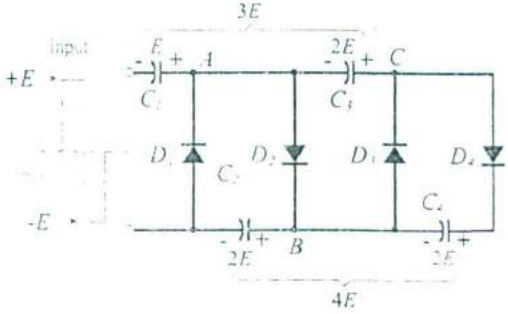
Chapter 3

Diode Applications



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Objectives

You will be able to:

1. *Sketch half-wave and full-wave rectifier circuits showing input and output waveforms, and explain the operation of each circuit.*
2. *Draw and explain circuit diagrams for basic dc power supplies using rectifiers and capacitor filters.*
3. *Determine capacitor values and diode current and voltage levels for basic dc power supplies.*
4. *Define line effect, load effect, line regulation, and load regulation for dc power supplies. Calculate these quantities for various power supplies.*
5. *Sketch Zener diode voltage regulator circuits, and explain their operation.*
6. *Design and analyze Zener diode regulator circuits.*
7. *Draw diagrams for series and shunt clipping circuits, clamping circuits, and dc voltage multipliers.*
8. *Sketch the input and output waveforms, and explain the operation of each of the circuit in objective 7.*
9. *Design and analyze the types of circuits listed in objective 7.*
10. *Sketch diode AND and OR gate circuits, and explain their operation.*

Introduction

One of the most important application of diodes is rectification; that is, conversion of a sinusoidal *ac* waveform into single-polarity half cycles. The rectified wave is smoothed by the use of capacitors to process it into direct voltage. A Zener diode may be applied to regulate the direct voltage.

Other important diode applications include clipping, clamping, *dc* voltage multiplication, and logic circuits. Diode clipping circuits are used for *clipping-off* an unwanted portion of a waveform. Clamping circuits change the *dc* voltage level of a waveform without affecting the wave shape. DC voltage multipliers are applied to change the level of a *dc* voltage source to a desired higher level. Logic circuits produce a *high* or *low* output voltage, depending upon the voltage levels at several input terminals.

3-1 *Half-Wave Rectification*

Half-Wave Rectifier Circuit

A basic diode *half-wave rectifier* circuit is shown in Fig. 3-1(a). An alternating input voltage is applied to a single diode connected in series with a load resistor R_L. The diode is forward biased during the positive half-cycles of the input waveform, and reverse biased during the negative half-cycles. Substantial current flows through R_L only during the positive half-cycles of the input. For the duration of the negative half-cycles, the diode behaves almost as an open switch. The output voltage waveform developed across R_L is a series of positive half-cycles of alternating voltage with intervening very small negative voltage levels produced by the diode reverse saturation current.

When the diode is forward biased [Fig. 3-1(a)], the voltage drop across it is V_F, and the output voltage is (input voltage) - V_F. So, the peak output voltage is,

$$V_{po} = V_{pi} - V_F \qquad \textbf{(3-1)}$$

Note that $V_{pi} = 1.414\ V_i$, where V_i is the *rms* level of the sinusoidal input voltage.

The diode peak forward current is,

$$I_p = \frac{V_{po}}{R_L} \qquad \textbf{(3-2)}$$

During the negative half-cycle of the input [Fig. 3-1(b)], the reverse-biased diode offers a very high resistance. So, only a very small reverse current (I_R) flows, giving an output voltage,

$$-V_o = -I_R \times R_L \qquad \textbf{(3-3)}$$

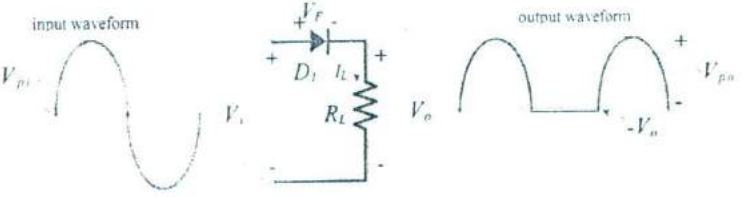
While the diode is reverse biased, the peak voltage of the negative half-cycle of the input is applied to its terminals. Thus, the *peak reverse voltage*, or *peak inverse voltage (PIV)*, applied to the diode is,

$$V_R = PIV = V_{pi} \qquad (3\text{-}4)$$

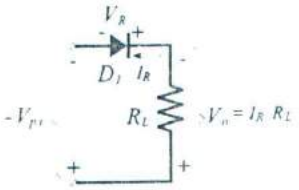
Most rectifier circuits use a *reservoir capacitor* at the output terminals to smooth the rectified voltage wave into direct voltage [see Fig. 3-1(c)]. It is important to note that

the presence of the reservoir capacitor substantially changes the rectified voltage waveform and affects the diode current and voltage requirements.

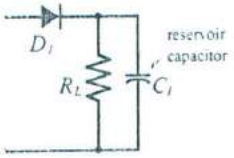
This is discussed in Section 3-3.



(a) Half-wave rectifier circuit with input and output waveforms



(b) Effect of negative input



(c) Use of a reservoir capacitor

Figure 3-1
Half-wave rectifier circuit. The diode is forward biased during one half-cycle of the applied waveform, and reverse-biased during the other half-cycle.

Example 3-1

A diode with $V_f = 0.7$ V is connected as a half-wave rectifier. The load resistance is 500 Ω, and the (*rms*) ac input is 22 V. Determine the peak output voltage, the peak load current, and the diode peak reverse voltage.

Solution

$$V_{pi} = 1.414\, V_i = 1.414 \times 22\ \text{V} = 31.1\ \text{V}$$

Eq. 3-1, $$V_{po} = V_{pi} - V_F = 31.1\ \text{V} - 0.7\ \text{V}$$
$$= 30.4\ \text{V}$$

Eq. 3-2, $$I_P = \frac{V_{po}}{R_l} = \frac{30.4\ \text{V}}{500\ \Omega}$$
$$= 60.8\ \text{mA}$$

Eq. 3-4, $$PIV = V_{pi} = 31.1\ \text{V}$$

Practise Problems

3-1.1 A half-wave rectifier circuit has a 15 V ac input and a 330 Ω load resistance. Calculate the peak output voltage, peak load current, and the diode maximum reverse voltage.

3-1.2 A half-wave rectifier (as in Fig. 3-1) produces a 40 mA peak load current through a 1.2 kΩ resistor. If the diode is silicon, calculate the *rms* input voltage and the diode PIV.

3-2 *Full-Wave Rectification*

Two-Diode Full-Wave Rectifier

The *full-wave rectifier* circuit in Fig. 3-2 uses two diodes, and its input voltage is supplied from a transformer (T_1) with a center-tapped secondary winding. The circuit is essentially a combination of two half-wave rectifier circuits, each supplied from half of the transformer secondary.

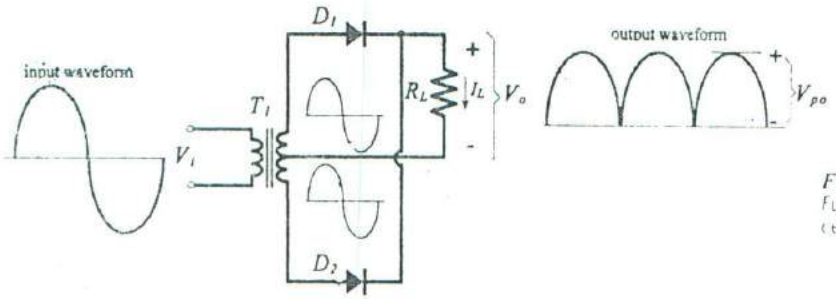
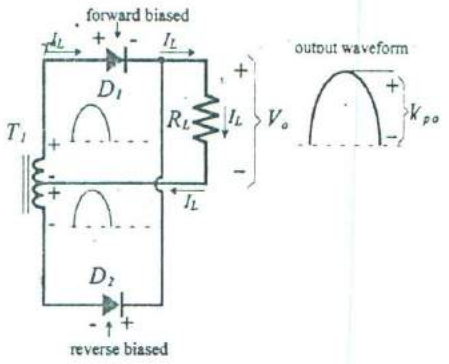
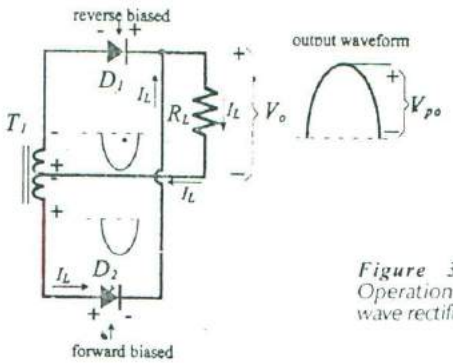


Figure 3-2
Full-wave rectifier circuit using a center-tapped transformer.



(a) D_1 forward biased, D_2 reverse biased



(b) D_1 reverse biased, D_2 forward biased

Figure 3-3
Operation of a two-diode full-wave rectifier circuit.

When the transformer output voltage is positive at the top, as illustrated in Fig. 3-3(a), the anode of D_1 is positive, and the center-tap of the transformer is connected to the cathode of D_1 via R_L. Consequently, D_1 is forward biased, and load current (I_L) flows

from the top of the transformer secondary through D_1, through R_L from top to bottom, and back to the transformer center-tap. During this time, the polarity of the voltage from the bottom half of the transformer secondary causes diode D_2 to be reverse biased.

For the duration of the negative half-cycle of the transformer output, the polarity of the transformer secondary voltage causes D_1 to be reverse biased and D_2 to be forward biased, [see Fig. 3-3(b)]. I_L flows from the bottom terminal of the transformer secondary through diode D_2, through R_L from top to bottom, and back to the transformer center-tap. The output waveform is the combination of the two half-cycles; that is, a continuous series of positive half-cycles of sinusoidal waveform. This is *full-wave rectification*.

Bridge Rectifier

The center-tapped transformer used in the circuit of Fig. 3-2 is usually more expensive and requires more space than additional diodes. So, a *bridge rectifier* is the circuit most frequently used for full-wave rectification.

The bridge rectifier circuit in Fig. 3-4 is seen to consist of four diodes connected with their arrowhead symbols all pointing toward the positive output terminal of the circuit. Diodes D_1 and D_2 are series-connected, as are D_3 and D_4. The *ac* input terminals are the junction of D_1 and D_2 and the junction of D_3 and D_4. The positive output terminal is at the cathodes of D_1 and D_3, and the negative output is at the anodes of D_2 and D_4.

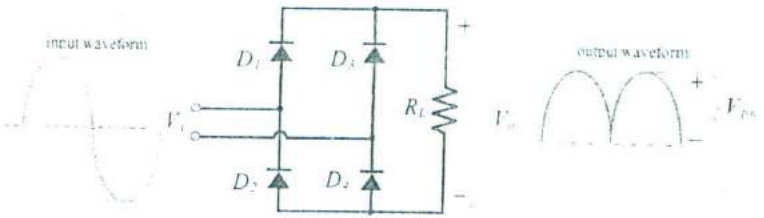


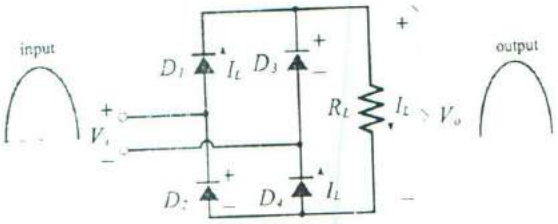
Figure 3-4
Full-wave bridge rectifier circuit.

During the positive half-cycle of input voltage, diodes D_1 and D_4 are in series with R_L, as illustrated in Figs. 3-5(a) and (b). Thus, load current (I_L) flows from the positive input terminal through D_1 to R_L, and then through R_L and D_4 back to the negative input terminal. Note that the direction of the load current through R_L is from top to bottom. During this time, the positive input terminal is applied to the cathode of D_2, and the negative output is at D_2 anode, [see Fig. 3-5(a)]. So, D_2 is reverse biased during the positive half-cycle of the input. Similarly, D_3 has the negative input at its anode and the positive output at its cathode during the positive input half-cycle, causing D_3 to be reverse biased.

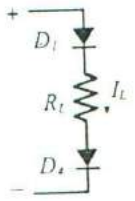
Figures 3-5(c) and (d) show that diodes D_2 and D_3 are forward biased during the negative half-cycle of the input waveform, while D_1 and D_4 are reverse biased. Although the circuit input terminal

polarity is reversed, I_L again flows through R_L from top to bottom, via D_3 and D_2.

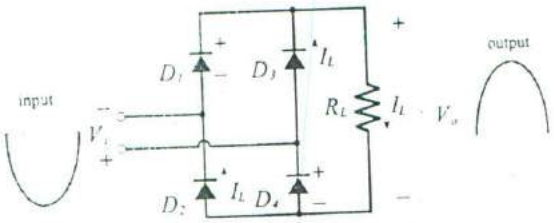
It is seen that during both half-cycles of the input, the output terminal polarity is always positive at the top of R_L, negative at the bottom. Both positive and negative half-cycles of the input are passed to the output. The negative half-cycles are inverted, so that the output is a continuous series of positive half-cycles of sinusoidal voltage.



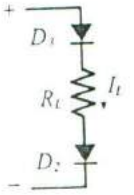
(a) Effect of positive half-cycle of input



(b) D_1 and D_4 forward biased



(c) Effect of negative half-cycle of input



(d) D_3 and D_2 forward biased

Figure 3-5 Operation of the bridge rectifier circuit.

The bridge rectifier has two forward-biased diodes in series with the supply voltage and the load. Because each diode has a forward voltage drop (V_F), the peak output voltage is,

$$V_{po} = V_{pi} - 2V_F \qquad \textbf{(3-5)}$$

As in the case of the half-wave rectifier,

a reservoir capacitor substantially changes the full-wave rectified output voltage waveform and affects the diode current and voltage requirements.

See the discussions in Sections 3-3 and 3-4.

Example 3-2

Determine the peak output voltage and current for the bridge rectifier circuit in Fig. 3-4 when $V_i = 30$ V, $R_L = 300\ \Omega$, and the diodes have $V_F = 0.7$ V.

Solution

$$V_{pi} = 1.414\,V_i = 1.414 \times 30\ \text{V}$$
$$= 42.42\ \text{V}$$

Eq. 3-5. $V_{po} = V_{pi} - 2V_f = 42.42\ V - (2 \times 0.7\ V)$
$= 41\ V$

Eq. 3-2. $I_p = \frac{V_{po}}{R_l} = \frac{41\ V}{300\ \Omega}$
$= 137\ mA$

Figure 3-6 shows two common methods of drawing a bridge rectifier circuit. Although they both look more complex than the circuit in Fig. 3-4, comparison shows that they are exactly the same circuit. The cathodes of D_1 and D_3 in all three circuits are connected to the positive output terminal, and the anodes of D_2 and D_4 are connected to the negative output terminal. Also, the *ac* input is applied to the junction of D_1 and D_2 and the junction of D_3 and D_4.

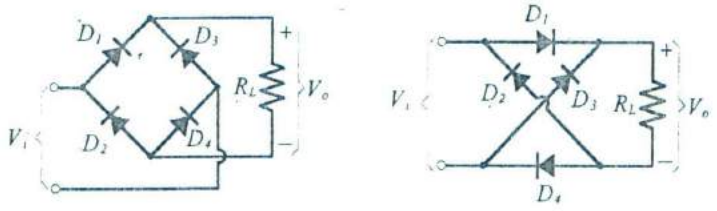


Figure 3-6
Two more ways of showing bridge rectifier circuits. These are exactly the same as the circuit in Fig. 3-4.

Practise Problems

3-2.1 Determine the peak load voltage, peak current, and the power dissipation in a 470 load resistor connected to a bridge rectifier circuit that has a 24 V ac input. The rectifier diodes are germanium.

3-2.2 A bridge rectifier with silicon diodes and a 680 Ω load resistor has an 18 V peak output. Calculate the power dissipated in the load resistor and the *rms* input voltage.

3-3 *Half-Wave Rectifier DC Power Supply*

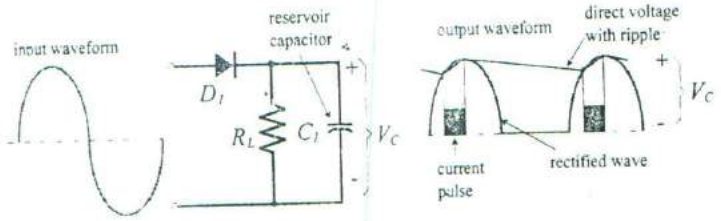
Capacitor Filter Circuit

When a sinusoidal alternating voltage is rectified, the resultant waveform is a series of positive (or negative) half-cycles of the input waveform; it is not direct voltage. To convert to direct voltage (*dc*), a *smoothing circuit* or *filter* must be employed.

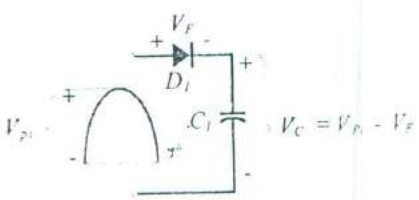
Figure 3-7(a) shows a half-wave rectifier circuit with a single capacitor filter (C_1) and a load resistor (R_L). The capacitor, termed a *reservoir capacitor*, is charged almost to the peak level of the circuit input voltage when the diode is forward biased. This occurs at V_{pi}, as shown in Fig. 3-7(b), giving a peak capacitor voltage,

$$V_C = V_{pi} - V_F \qquad (3\text{-}6)$$

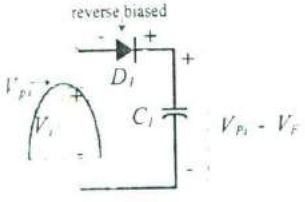
When the instantaneous level of input (at the diode anode) falls below V_{pi} the diode becomes reverse biased, because the capacitor voltage (V_C) (at the diode cathode) remains close to (V_{pi} - V_F). [see Fig. 3-7(c)]. With the diode reverse biased, the capacitor begins to discharge through the load resistor (R_L). So, V_C falls slowly, as shown by the capacitor voltage waveform in Fig. 3-7(a).



(a) Half-wave rectifier circuit with a reservoir capacitor



(b) C_1 is charged to $V_{pi} - V_F$



(c) D_1 is reverse biased when V_i falls below V_{pi}

Figure 3-7
A reservoir capacitor smoothes the output from a rectifier circuit by charging up to the peak output voltage and retaining most of its charge between voltage peaks.

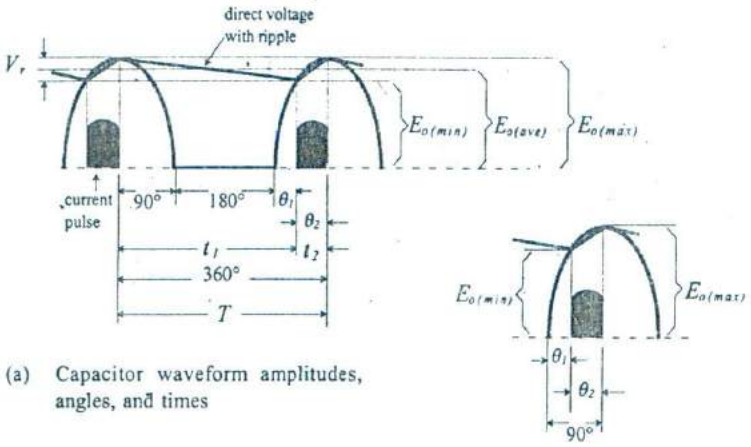
The diode remains reverse biased through the remainder of the input positive half-cycle, the negative half-cycle, and the first part of the positive half-cycle again until the instantaneous level of V_i becomes greater than V_C once more. At this point current flows through the diode to recharge the capacitor, causing the capacitor voltage to return to (V_{pi} - V_F). The charge and discharge of the capacitor causes the small increase and decrease in the capacitor voltage, which is also the circuit output voltage. It is seen that the circuit output is a direct voltage with a small *ripple voltage* waveform superimposed. [Fig. 3-7(a)].

Capacitance Calculation

The amplitude of the ripple voltage is affected by the load current, the reservoir capacitor value, and the capacitor discharge time. The discharge time depends upon the frequency of the ripple waveform, which is the same as the *ac* input frequency in the case of a half-wave rectifier. With a constant load current, the ripple amplitude is inversely proportional to the capacitance; the largest capacitance produces the smallest ripple.

The capacitance for the reservoir capacitor can be calculated from the load current, the acceptable ripple amplitude, and the capacitor discharge time. Consider the circuit output voltage waveform illustrated in Fig. 3-8(a). The waveform quantities are:

E_{ave}	average *dc* output voltage
$E_{o(max)}$	maximum output voltage level
$E_{o(min)}$	minimum output voltage
V_r	ripple voltage peak-to-peak amplitude
T	time period of the *ac* input waveform
t_1	capacitor discharge time
t_2	capacitor charge time
θ_1	phase angle of the input wave from zero to $E_{o(min)}$
θ_2	phase angle of the input wave from $E_{o(min)}$ to $E_{o(max)}$



(a) Capacitor waveform amplitudes, angles, and times

(b) Relationship between $E_{o(min)}$ and $E_{o(max)}$

Figure 3-8
The capacitance value for a reservoir capacitor can be calculated from a knowledge of the load current, ripple voltage, and input frequency.

Figure 3-8(b) shows that, because the input wave is sinusoidal,

$$E_{o(min)} = E_{o(max)} \sin \theta_1$$

which gives,

$$\theta_1 = \sin^{-1} \frac{E_{o(min)}}{E_{o(max)}} \qquad \textbf{(3-7)}$$

Also from Fig. 3-8(b),

$$\theta_2 = 90° - \theta_1 \qquad \textbf{(3-8)}$$

The time period is,

$$T = \frac{1}{f}$$

where f is the frequency of the *ac* input waveform.

During T, the input waveform goes through a 360° phase angle, which gives the time per degree as,

$$t/degree = \frac{T}{360°}$$

so, $$t_2 = \frac{\theta_2 T}{360^\circ} \quad \textbf{(3-9)}$$

and, $$t_1 = T - t_2 \quad \textbf{(3-10)}$$

Taking the current as a constant quantity.

$$C = \frac{I_L t_1}{V_r} \quad \textbf{(3-11)}$$

Capacitor Selection

When a capacitance value is calculated, an appropriate capacitor has to be selected from a manufacturer's list of available standard values. With a reservoir capacitor, the calculated capacitance is always the minimum value required to give a specified maximum ripple voltage amplitude. If a larger-than-calculated capacitance is used, the ripple voltage will be lower than the specified maximum. So, a larger standard value capacitor is always selected in the case of a reservoir capacitor.

The standard-value capacitors listed in Appendix 2-2 are typically available with ±20% tolerance. In the case of capacitors greater than 10 μF, the tolerance is often listed as -10% +50%. This means that a 100 μF capacitor might have a capacitance as low as 90 μF, or as high as 150 μF. In most circuit situations, a minimum capacitance value is calculated, and a larger value is quite acceptable.

The voltage that a capacitor will be subjected to must be taken into consideration. The maximum voltage that may be safely applied to a capacitor is stated in terms of its *dc working voltage*. The *dc* working voltages can be quite small for large-value capacitors. For example, some 10 μF capacitors have 6.3 V working voltages. The capacitor dielectric may break down if the specified voltage is exceeded.

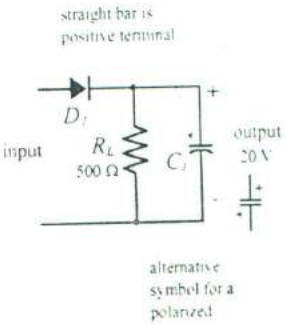


Figure 3-9
It is very important that polarized capacitors be connected with the correct polarity.

Capacitor Polarity

It is very important that polarized capacitors be correctly connected. Sometimes polarized capacitors ***explode*** when they are incorrectly connected, and this could have ***tragic consequences*** for the eyes of an experimenter. The positive terminal is represented by the straight bar on the component graphic symbol, or identified by the plus sign on the alternative symbol, (see Fig. 3-9). This should be connected to the most positive point in the circuit where the capacitor is to be installed. Non-polarized capacitors should be used in situations where the voltage polarity might be reversed.

Example 3-3

The half-wave rectifier *dc* power supply in Fig. 3-9 is to supply 20 V to a 500 Ω load. The peak-to-peak ripple voltage is not to exceed 10% of the average output voltage, and the ac input frequency is 60 Hz. Calculate the required reservoir capacitor value.

Solution

$$V_r = 10\% \text{ of } E_{o(ave)} = 10\% \text{ of } 20 \text{ V}$$
$$= 2 \text{ V}$$

$$E_{o(min)} = E_{o(ave)} - 0.5\, V_r = 20 \text{ V} - (0.5 \times 2 \text{ V})$$
$$= 19 \text{ V}$$

$$E_{o(max)} = E_{o(ave)} + 0.5\, V_r = 20 \text{ V} + (0.5 \times 2 \text{ V})$$
$$= 21 \text{ V}$$

Eq. 3-7,
$$\theta_1 = \sin^{-1} \frac{E_{o(min)}}{E_{o(max)}} = \sin^{-1} \frac{19 \text{ V}}{21 \text{ V}}$$
$$\approx 65°$$

Eq. 3-8,
$$\theta_2 = 90° - \theta_1 = 90° - 65°$$
$$= 25°$$

$$T = \frac{1}{f} = \frac{1}{60 \text{ Hz}}$$
$$= 16.7 \text{ ms}$$

Eq. 3-9,
$$t_2 = \frac{\theta_2\, T}{360°} = \frac{25° \times 16.7 \text{ ms}}{360°}$$
$$= 1.16 \text{ ms}$$

Eq. 3-10,
$$t_1 = T - t_2 = 16.7 \text{ ms} - 1.16 \text{ ms}$$
$$= 15.54 \text{ ms}$$

$$I_L = \frac{E_{o(ave)}}{R_L} = \frac{20 \text{ V}}{500\ \Omega}$$
$$= 40 \text{ mA}$$

Eq. 3-11,
$$C = \frac{I_L\, t_1}{V_r} = \frac{40 \text{ mA} \times 15.54 \text{ ms}}{2 \text{ V}}$$
$$= 310\ \mu\text{F (use 330 } \mu\text{F - see Appendix 2-2)}$$

Approximate Calculations

The capacitance calculation in Example 3-3 assumes that the load current is a constant quantity. This is an approximation, because the load current changes by a small amount as the output voltage increases and decreases. Normally, the load current change is so small that it has no significant effect on the calculation.

Another approximation that can be made to simplify the capacitance calculation is to take the discharge time (t_1) as equal to the input waveform time period (T), [see Fig. 3-8(a)].

$$t_1 \approx T \qquad \textbf{(3-12)}$$

Equation 3-12 assumes that the capacitor charging time (t_2) is so much smaller than t_1 that it can be neglected.This is a reasonable assumption where the ripple voltage is small. Also, use of Eq. 3-12

gives a larger capacitance value than the more precise calculation, and this is acceptable because a larger-than-calculated standard value capacitor is normally selected.

Example 3-4

Assuming that $t_2 << t_1$, recalculate the required reservoir capacitor value for the circuit in Example 3-3

Solution

$$V_r = 10\% \text{ of } E_{o(ave)} = 10\% \text{ of } 20 \text{ V}$$
$$= 2 \text{ V}$$

$$T = \frac{1}{f} = \frac{1}{60 \text{ Hz}}$$
$$= 16.7 \text{ ms}$$

Eq. 3-12, $$t_1 \approx T = 16.7 \text{ ms}$$

$$I_L = \frac{E_{o(ave)}}{R_L} = \frac{20 \text{ V}}{500 \Omega}$$
$$= 40 \text{ mA}$$

Eq. 3-11, $$C = \frac{I_L \, t_1}{V_r} = \frac{40 \text{ mA} \times 16.7 \text{ ms}}{2 \text{ V}}$$

$$= 334 \, \mu\text{F}$$

Diode Specification

Rectifier diodes must be specified in terms of the currents and voltages that they are subjected to. The calculated levels are normally minimum quantities, and the selected diodes must be able to survive higher levels.

Consider Fig. 3-10 which illustrates the situation when the *ac* input wave is at its negative peak voltage ($-V_p$). The capacitor has already been charged up to approximately the positive peak level of the input ($+V_p$). Consequently, the diode has $-V_p$ at its anode and $+V_p$ at its cathode, so the diode peak reverse voltage is,

$$V_R \approx 2 \, V_p \qquad \textbf{(3-13)}$$

The *average forward rectified current* ($I_{F(av)}$) that the diode must pass is equal to the *dc* output current.

$$I_{F(av)} = I_L \qquad \textbf{(3-14)}$$

The diode in a half-wave rectifier circuit with a reservoir capacitor does not conduct continuously, but repeatedly passes pulses of current to recharge the capacitor each time the diode becomes forward biased. This is illustrated in Fig. 3-8 and again in Fig. 3-11. The current pulse is known as the *repetitive surge current*, and is designated (I_{FRM}). The average input current to the rectifier circuit

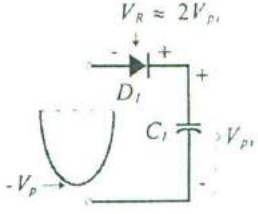


Figure 3-10
Diode reverse voltage in a half-wave rectifier.

must equal the average load current (I_L), so I_{FRM} averaged over time period T equals I_L. (see Fig. 3-11).

$$I_L = \frac{I_{FRM}\ t_2}{(t_1 + t_2)}$$

giving,

$$I_{FRM} = \frac{I_L (t_1 + t_2)}{t_2} \qquad \textbf{(3-15)}$$

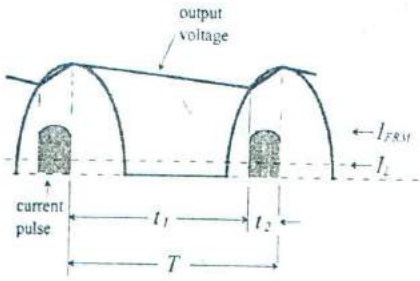


Figure 3-11
Diode average (load) current (I_L) and repetitive surge current (I_{FRM}) in a half-wave rectifier.

Figure 3-12 shows a half-wave rectifier circuit with a resistor (R_S) connected in series with the diode. This is a low-resistance component known as a *surge limiting resistor*. As its name suggests, the purpose of R_S is to limit the level of any surge current that might pass through the diode. The highest surge current occurs when the *ac* supply is first switched on to the rectifier circuit. Before switch-on, the reservoir capacitor normally contains no charge, so it behaves as a short-circuit at the instant of switch-on. If switch-on occurs when the *ac* input is at its peak level, the surge current is,

$$I_{F(surge)} = \frac{V_p}{R_S}$$

For a diode with a specified maximum *non-repetitive surge current* (I_{FSM}), the surge limiting resistor is calculated as,

$$R_S = \frac{V_p}{I_{FSM}} \qquad \textbf{(3-16)}$$

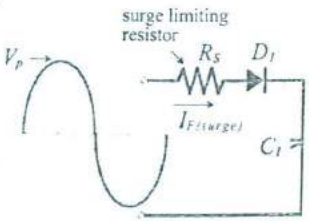


Figure 3-12
Surge limiting resistor in a half-wave rectifier.

Example 3-5

Specify the diode for the half-wave rectifier circuit in Example 3-3. Select a suitable device from Appendix 1, and calculate a suitable surge limiting resistance.

Solution

$$V_p = E_{o(max)} + V_F = 21\ \text{V} + 0.7\ \text{V}$$
$$= 21.7\ \text{V}$$

Eq. 3-13, $V_R \approx 2\,V_p = 2 \times 21.7\ \text{V}$
$= 43.4\ \text{V}$

Eq. 3-14, $I_{F(av)} = I_L = 40\ \text{mA}$

Eq. 3-15, $I_{FRM} = \dfrac{I_L(t_1 + t_2)}{t_2} = \dfrac{40\ \text{mA} \times 16.7\ \text{ms}}{1.16\ \text{ms}}$
$= 576\ \text{mA}$

In Appendix 1-2, the *1N4001* has $V_R = 50\ \text{V}$, and $I_{F(av)} = I_o = 1\ \text{A}$, and $I_{FRM} = I_{Fm(rep)} = 10\ \text{A}$. So, its specification is better than required for this application. Any of the *1N4002* through *1N4007* diodes could be used, but, those with higher reverse voltage are more expensive than the *1N4001*.

For the *1N4001*, $I_{F(surge)} = 30\ \text{A}$

Eq. 3-16, $R_S = \dfrac{V_p}{I_{FSM}} = \dfrac{21.7\ \text{V}}{30\ \text{A}}$
$\approx 0.7\ \Omega$

Practise Problems

3-3.1 A *dc* power supply consisting of a half-wave rectifier and a reservoir capacitor has to supply 120 V to a 200 Ω load. Determine the capacitance required if the maximum ripple voltage is to be ±5% of the average output, and the input frequency is 60 Hz.

3-3.2 For Problem 3-3.1, recalculate the capacitance approximately by assuming that the capacitor discharge time is very much larger than the charging time.

3-3.3 For the circuit in Problem 3-3.1, specify the diode, select a suitable device from the available data sheets, and determine the required surge limiting resistance.

3-4 *Full-Wave Rectifier DC Power Supply*

Like half-wave rectifiers, full-wave rectifiers require filter circuits to convert the output waveform to direct voltage. Figure 3-13 shows a full-wave rectifier circuit with a reservior capacitor and a surge limiting resistor. These components operate exactly as explained for the half-wave rectifier circuit, with a few important exceptions.

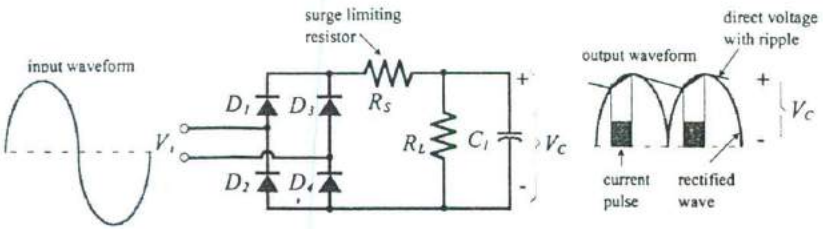


Figure 3-13
Bridge rectifier circuit with a reservior capacitor and a surge limiting resistor

The capacitor-smoothed full-wave rectifier waveforms are shown in detail in Fig. 3-14. Eqation 3-7, derived for the half-wave rectifier circuit, still applies for determining the angle θ_1.

Eq. 3-7, $$\theta_1 = \sin^{-1} \frac{E_{o(min)}}{E_{o(max)}}$$

Also, θ_2 can be determined from Eq.3-8,

Eq.3-8, $$\theta_2 = 90^\circ - \theta_1$$

and Eq. 3-9 can be used for time t_2,

Eq. 3-9, $$t_2 = \frac{\theta_2 T}{360^\circ}$$

Comparing Fig. 3-14 and Fig. 3-8, it is seen that the capacitor discharge time (t_1) for the half-wave circuit is approximately equal to the waveform time period (T), whereas for the full-wave circuit t_1 approximately equals $T/2$. More precisely,

$$t_1 = (T/2) - t_2 \qquad \textbf{(3-17)}$$

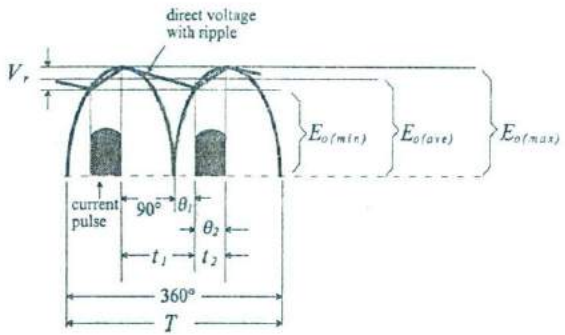


Figure 3-14
Ripple voltage, waveform angles and time periods for a full-wave rectifier with capacito smoothing.

Using the correct value of t_1, Eq. 3-11 can be used for calculating the reservior capacitance for a full-wave rectifier circuit.

Eq. 3-11, $$C = \frac{I_L t_1}{V_r}$$

Similarly, (using the correct value of t_1 in Fig. 3-14), the repetitive current (I_{FRM}) can be determined from Eq. 3-15,

Eq. 3-15, $$I_{FRM} = \frac{I_L (t_1 + t_2)}{t_2}$$

The average forward current passed by the bridge rectifier circuit is equal to the load current. But, each pair of diodes supplies

current for no more than a half cycle of the input wave. The other pair conducts during the other half cycle. So, as illustrated in Fig. 3-15, the diode average forward current is half of the load current.

$$I_{F(av)} = \frac{I_L}{2}$$

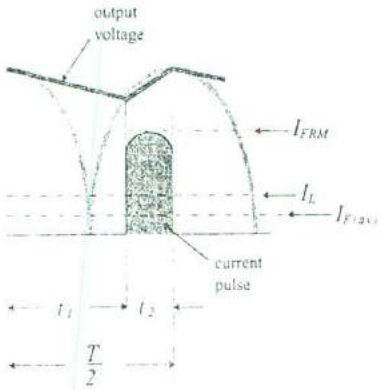


Figure 3-15
The diode average forward current in a bridge rectifier circuit is equal to half the load current.

Another difference between the half-wave and full-wave rectifier power supply circuits concerns the reverse voltage applied to the diodes. Consider Fig. 3-16. When the instantaneous input voltage is $+V_p$, as illustrated, V_p is applied across forward-biased diode D_1 in series with reverse-biased diode D_3. Therefore, the reverse voltage across D_3 is,

$$V_R = V_p - V_F$$

or,

$$V_R \approx V_p \qquad \textbf{(3-18)}$$

Examination of the circuit shows that Eq. 3-18 applies to each diode when reverse biased.

As in the case of the half-wave circuit, the capacitor calculation can be simplified by assuming that time t_2 is very much smaller than t_1. This gives the approximation that the capacitor discharge time is equal to half the input waveform time period.

$$t_1 \approx \frac{T}{2} \qquad \textbf{(3-19)}$$

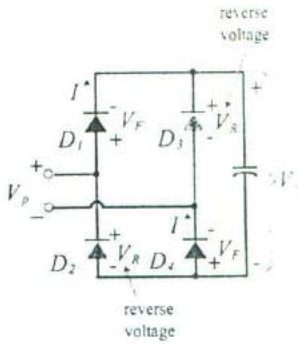


Figure 3-16
Diode reverse voltage (V_R) in a bridge rectifier circuit.

Example 3-6

The full-wave rectifier *dc* power supply in Fig. 3-17 is to supply 20 V to a 500 Ω load. The peak-to-peak ripple voltage is not to exceed 10% of the average output voltage, and the ac input frequency is 60 Hz. Calculate the required reservoir capacitor value. (Note that the specifications for this example are similar to those for the half-wave circuit in Example 3-3.)

Solution

$$V_r = 10\% \text{ of } E_{o(ave)} = 10\% \text{ of } 20 \text{ V}$$
$$= 2 \text{ V}$$

$$E_{o(min)} = E_{o(ave)} - 0.5\,V_r = 20\text{ V} - (0.5 \times 2\text{ V})$$
$$= 19\text{ V}$$

$$E_{o(max)} = E_{o(ave)} + 0.5\,V_r = 20\text{ V} + (0.5 \times 2\text{ V})$$
$$= 21\text{ V}$$

Eq. 3-7, $$\theta_1 = \sin^{-1}\frac{E_{o(min)}}{E_{o(max)}} = \sin^{-1}\frac{19\text{ V}}{21\text{ V}}$$
$$\approx 65°$$

Eq. 3-8, $$\theta_2 = 90° - \theta_1 = 90° - 65°$$
$$= 25°$$

$$T = \frac{1}{f} = \frac{1}{60\text{ Hz}}$$
$$= 16.7\text{ ms}$$

Eq. 3-9, $$t_2 = \frac{\theta_2\,T}{360°} = \frac{25° \times 16.7\text{ ms}}{360°}$$
$$= 1.16\text{ ms}$$

Eq. 3-17, $$t_1 = (T/2) - t_2 = (16.7\text{ ms}/2) - 1.16\text{ ms}$$
$$= 7.19\text{ ms}$$

$$I_L = \frac{E_{o(ave)}}{R_L} = \frac{20\text{ V}}{500\,\Omega}$$
$$= 40\text{ mA}$$

Eq. 3-11, $$C = \frac{I_L\,t_1}{V_r} = \frac{40\text{ mA} \times 7.19\text{ ms}}{2\text{ V}}$$
$$= 143.8\,\mu\text{F (use 150 }\mu\text{F - see Appendix 2-2)}$$

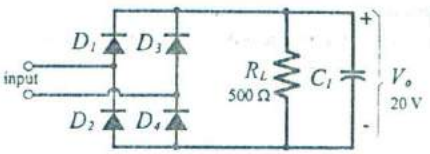


Figure 3-17
Circuit for Example 3-6.

Example 3-7

Assuming that t_2 is very much smaller than t_1, recalculate the required reservoir capacitor value for the circuit in Example 3-5

Solution

$$V_r = 10\%\text{ of } E_{o(ave)} = 10\%\text{ of } 20\text{ V}$$
$$= 2\text{ V}$$

$$T = \frac{1}{f} = \frac{1}{60\text{ Hz}}$$
$$= 16.7\text{ ms}$$

Eq. 3-19, $$t_1 \approx \frac{T}{2} = \frac{16.7\text{ ms}}{2}$$
$$= 8.35\text{ ms}$$

$$I_L = \frac{E_{o(ave)}}{R_L} = \frac{20\text{ V}}{500\,\Omega}$$
$$= 40\text{ mA}$$

Eq. 3-11, $$C = \frac{I_L t_1}{V_r} = \frac{40\text{ mA} \times 8.36\text{ ms}}{2\text{ V}}$$
$$= 167\ \mu\text{F}$$

Example 3-8

Specify the diode for the bridge rectifier circuit in Example 3-6. Select a suitable device and calculate the surge limiting resistance.

Solution

$$V_p = E_{o(max)} + (2\ V_F) = 21\text{ V} + (2 \times 0.7\text{ V})$$
$$= 22.4\text{ V}$$

Eq. 3-18, $$V_R \approx V_p = 22.4\text{ V}$$

Eq. 3-14, $$I_{F(av)} = I_L = 40\text{ mA}$$

Eq. 3-15, $$I_{FRM} = \frac{I_L(t_1 + t_2)}{t_2} = \frac{40\text{ mA} \times 8.35\text{ ms}}{1.16\text{ ms}}$$
$$= 288\text{ mA}$$

From Appendix 1-2, the *1N4001* is suitable.

For the *1N4001*, $I_{F(surge)} = 30\text{ A}$

Eq. 3-16, $$R_S = \frac{V_p}{I_{FSM}} = \frac{22.4\text{ V}}{30\text{ A}}$$
$$\approx 0.75\ \Omega$$

Practise Problems

3-4.1 A *dc* power supply consisting of a bridge rectifier and a reservoir capacitor has to supply 15 V to a 150 Ω load. Determine the capacitance required if the maximum ripple voltage is to be ±5% of the average output, and the input frequency is 60 Hz.

3-4.2 For Problem 3-4.1, recalculate the capacitance approximately by assuming that the capacitor discharge time is very much larger than the charging time.

3-4.3 For the circuit in Problem 3-4.1, specify the diode, select a suitable device from the available data sheets, and determine the required surge limiting resistance.

3-5 Power Supply Performance

Source Effect

The *ac* supply to the input of a transformer in a *dc* power supply does not always remain constant. A ±10% variation in the *ac source voltage* (V_S) (also termed the *line voltage*) is not unusual. When the source voltage varies, there is some variation in the *dc*

output voltage from a power supply, (see Fig. 3-18). This output voltage change (ΔE_o) due to a change in the input is termed the *source effect*. If the output varies by 100 mV when the source voltage changes by ±10%, the *source effect* is 100 mV. An alternative way of stating this output change is to express ΔE_o as a percentage of the *dc* output voltage (E_o). In this case, the term *line regulation* is used.

$$\textbf{Source effect} = \Delta E_o \textbf{ for a 10\% change in } V_S \qquad \textbf{(3-20)}$$

$$\textbf{Line regulation} = \frac{(\Delta E_o \textbf{ for a 10\% change in } V_S) \times 100\%}{E_o} \qquad \textbf{(3-21)}$$

Load Effect

Power supply output voltage is also affected by changes in load current (I_L). The output voltage decreases when I_L is increased, and rises when I_L is reduced. The *load effect* defines how the output voltage changes when the load current is increased from zero to its specified maximum level ($I_{L(max)}$). If the load current change (ΔI_L) produces a voltage change (ΔE_o) of 100 mV, the *load effect* is 100 mV. As for the source effect, the load effect can also be expressed as a percentage of the output voltage. This is termed the *load regulation*.

$$\textbf{Load effect} = \Delta E_o \textbf{ for } \Delta I_{L(max)} \qquad \textbf{(3-22)}$$

$$\textbf{Load regulation} = \frac{(\Delta E_o \textbf{ for } \Delta I_{L(max)}) \times 100\%}{E_o} \qquad \textbf{(3-23)}$$

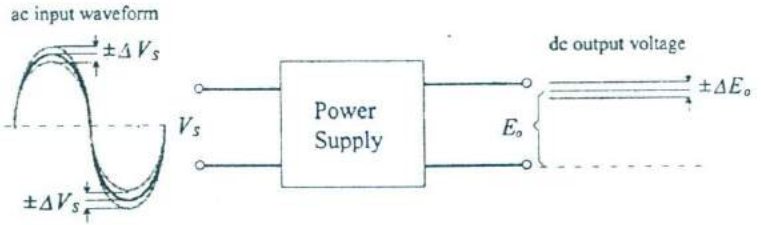


Figure 3-18
Power supply source effect is the output voltage change that occurs when the input voltage changes by ±10%.

Example 3-9

The output voltage of a *dc* power supply changes from 20 V to 19.7 V when the load is increased from zero to maximum. The voltage also increases to 20.2 V when the *ac* supply increases by 10%. Calculate the load and source effects, and the load and line regulations.

Solution

Eq. 3-22, $\quad \text{Load effect} = \Delta E_o \text{ for } \Delta I_{L(max)} = 20\text{ V} - 19.7\text{ V}$

$$= 300\text{ mV}$$

Eq. 3-23, $\quad \text{Load regulation} = \dfrac{(\Delta E_o \text{ for } \Delta I_{L(max)}) \times 100\%}{E_o} = \dfrac{300\text{ mV} \times 100\%}{20\text{ V}}$

$= 1.5\%$

Eq. 3-20, $\text{Source effect} = \Delta E_o \text{ for 10\% change in } V_S = 20.2\text{ V} - 20\text{ V}$

$= 200\text{ mV}$

Eq. 3-21, $\text{Line regulation} = \dfrac{(\Delta E_o \text{ for 10\% change in } V_S) \times 100\%}{E_o}$

$= \dfrac{200\text{ mV} \times 100\%}{20\text{ V}}$

$= 1\%$

Practise Problems

3-5.1 A dc power supply output drops from 15 V to 14.95 V when the ac source voltage falls by 10%. The output also falls from 15 V to 14.9 V when the load current is increased from zero to maximum. Calculate the source effect, load effect, line regulation, and load regulation.

3-6 Zener Diode Voltage Regulators

Regulator Circuit With No Load

The most important application of Zener diodes (discussed in Section 2-9) is *dc* voltage regulator circuits. These can be the simple regulator circuit shown in Fig. 3-19, or the more complex regulators discussed in Chapters 17. The circuit in Fig. 3-19 is usually employed as a voltage reference source that supplies only a very low current (much lower than I_Z) to the output. Resistor R_1 in Fig. 3-19 limits the Zener diode current to the desired level.

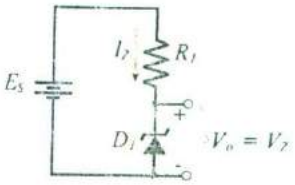


Figure 3-19
Zener diode reference voltage source, or voltage regulator.

$$I_Z = \frac{E_S - V_Z}{R_1} \qquad \textbf{(3-24)}$$

The Zener current may be just greater than the diode knee current (I_{ZK}). However, for the most stable reference voltage, I_Z should be selected as I_{ZT} (the specified test current). Example 3-10 demonstrates the circuit design procedure.

Example 3-10

A 9 V reference source is to be designed using a series-connected Zener diode and resistor connected to a 30 V supply. Select suitable components, and calculate the circuit current when the supply voltage drops to 27 V.

Solution

From the Zener diode data sheet in Appendix 1-4, the most suitable device is a *1N757* which has $V_Z = 9.1$ V, and $I_{ZT} = 20$ mA.

With $E_S = 30$ V,

From Eq. 3-24, $R_1 = \dfrac{E_S - V_Z}{I_Z} = \dfrac{30\text{ V} - 9.1\text{ V}}{20\text{ mA}}$

$= 1.05\text{ k}\Omega$ (use 1 kΩ — see Appendix 2-1)

P_D for R_1, $P_{R1} = I_1^2 R_1 = (20\text{ mA})^2 \times 1\text{ k}\Omega$

$= 0.4\text{ W}$

When $E_S = 27$ V,

$$I_Z = \frac{E_S - V_Z}{R_1} = \frac{27\text{ V} - 9.1\text{ V}}{1\text{ k}\Omega}$$

$= 17.9$ mA

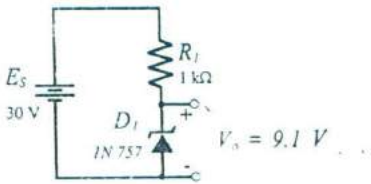


Figure 3-20
Circuit designed in Ex. 3-10.

Loaded Regulator

When a Zener diode regulator is required to supply a load current (I_L), as shown in Fig. 3-21, the total supply current (flowing through resistor R_1) is the sum of I_L and I_Z. Care must be taken to ensure that the minimum Zener diode current is large enough to keep the diode in reverse breakdown. Typically, $I_{Z(min)} = 5$ mA for a Zener diode with $I_{ZT} = 20$ mA. The circuit current equation is,

$$I_Z + I_L = \frac{E_S - V_Z}{R_1} \qquad \textbf{(3-25)}$$

In some cases, the load current in the type of circuit shown in Fig. 3-21 may be reduced to zero. Because the voltage drop across R_1 remains constant, the supply current remains constant at,

$$I_{R1} = I_Z + I_L$$

All of this current flows through the Zener diode when R_L is disconnected. The circuit design must ensure that the total current does not exceed the maximum Zener diode current.

Example 3-11 demonstrates the design process for a loaded voltage reference source that uses a low-power Zener diode. It should be noted that high-power Zener diodes are available for higher current levels.

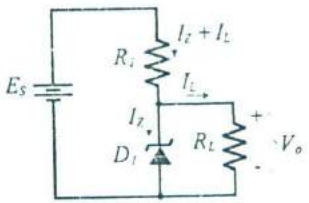


Figure 3-21
Zener diode voltage regulator circuit supplying a load current. The diode must be able to pass a current of $(I_L + I_Z)$.

Example 3-11

Design a 6 V dc reference source to operate from a 16 V supply. The circuit is to use a low-power Zener diode (as in Appendix 1-4) and is to produce maximum possible load current. Calculate the maximum load current that can be produced by the circuit.

Solution

From the Zener diode data sheet in Appendix 1-4, the *1N753* has $V_Z = 6.2$ V, and $P_D = 400$ mW.

from Eq. 2-11, $I_{ZM} = \dfrac{P_D}{V_Z} = \dfrac{400\text{ mW}}{6.2\text{ V}}$

$= 64.5$ mA

$I_{L(max)} + I_{Z(min)} = I_{ZM} = 64.5$ mA

from Eq. 3-24, $R_1 = \dfrac{E_S - V_Z}{I_{ZM}} = \dfrac{16\text{ V} - 6.2\text{ V}}{64.5\text{ mA}}$

$= 152\ \Omega$ (use $150\ \Omega$ standard value)

$P_{R1} = I_1^2 R_1 = (64.5\text{ mA})^2 \times 150\ \Omega$

$= 0.62$ W

select $I_{Z(min)} = 5$ mA

$I_{L(max)} = I_{ZM} - I_{Z(min)} = 64.5\text{ mA} - 5\text{ mA}$

$= 59.5$ mA

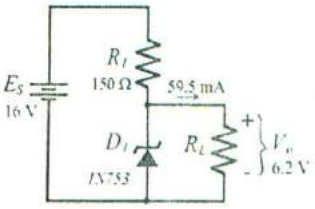


Figure 3-22
Circuit designed in Ex. 3-11.

Regulator Performance

The performance of a Zener diode voltage regulator may be expressed in terms of the source and load effects, and the line and load regulations, exactly as discussed in Section 3-5. Equations 3-20 through 3-23 may be applied. If there is an input ripple voltage, the output ripple will be severely attenuated. The *ripple rejection ratio* is the ratio of the output to input ripple amplitudes.

To assess the performance of a Zener diode voltage regulator, the *ac* equivalent circuit is first drawn by replacing the diode with its dynamic impedance (Z_Z), as shown in Fig. 3-23(a). The complete *ac* equivalent circuit is seen to be a simple voltage divider. When the input voltage changes by ΔE_S, the output voltage change is,

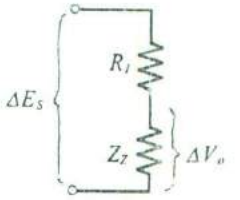
$$\Delta V_o = \frac{\Delta E_S \times Z_Z}{R_1 + Z_Z} \qquad \textbf{(3-26)}$$

Equation 3-26 assumes that there is no load connected to the regulator output. When a load is present, R_L appears in parallel with Z_Z in the *ac* equivalent circuit, [see Fig. 3-23(b)]. The equation for the output voltage change now becomes,

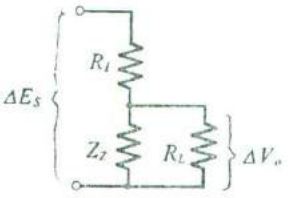
$$\Delta V_o = \frac{\Delta E_S \times (Z_Z \| R_L)}{R_1 + (Z_Z \| R_L)} \qquad \textbf{(3-27)}$$

The regulator source effect can be determined from Eq. 3-26 or Eq. 3-27, as appropriate. The equations can also be used for calculating ripple rejection ratio. The input ripple amplitude (V_{ri}) and the output ripple (V_{ro}) are substituted in place of the input and output voltages in Eq. 3-26 and Eq. 3-27. Thus, Eq. 3-26 can be modified to give a ripple rejection ratio equation,

$$\frac{V_{ro}}{V_{ri}} = \frac{Z_Z}{R_1 + Z_Z} \qquad \textbf{(3-28)}$$



(a) Regulator without a load



(b) Regulator with a load

Figure 3-23
AC equivalent circuits for Zener diode voltage regulators.

and, for a loaded regulator, Eq. 3-27 gives,

$$\frac{V_{ro}}{V_{ri}} = \frac{Z_Z||R_L}{R_1 + (Z_Z||R_L)} \qquad \textbf{(3-29)}$$

To determine the load effect of the Zener diode voltage regulator, the circuit output resistance has to be calculated. The regulator Thevenin equivalent circuit in Fig. 3-24 shows that, assuming a zero source resistance, the circuit output resistance is,

$$R_o = Z_Z||R_1 \qquad \textbf{(3-30)}$$

When the load current changes by ΔI_L, the output voltage change is,

$$\Delta V_o = \Delta I_L(Z_Z||R_1) \qquad \textbf{(3-31)}$$

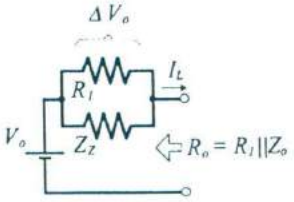


Figure 3-24
Thevenin equivalent circuit for a Zener diode regulator.

Example 3-12

Calculate the line regulation, load regulation, and ripple rejection ratio for the voltage regulator in Example 3-11.

Solution

From Appendix 1-4, the *1N753* has $Z_Z = 7\ \Omega$.

Source effect,

$$\Delta E_S = 10\% \text{ of } E_S = 10\% \text{ of } 16\text{ V}$$
$$= 1.6\text{ V}$$

$$R_L = \frac{V_o}{I_L} = \frac{6.2\text{ V}}{59.5\text{ mA}}$$
$$= 104\ \Omega$$

Eq. 3-27,
$$\Delta V_o = \frac{\Delta E_S \times (Z_Z||R_L)}{R_1 + (Z_Z||R_L)} = \frac{1.6\text{ V} \times (7\ \Omega||104\ \Omega)}{150\ \Omega + (7\ \Omega||104\ \Omega)}$$
$$= 67\text{ mV}$$

Eq. 3-21,
$$\text{Line regulation} = \frac{(\Delta E_o \text{ for 10\% change in } E_S) \times 100\%}{E_o}$$
$$= \frac{67\text{ mV} \times 100\%}{6.2\text{ V}}$$
$$= 1.08\%$$

Load effect,

Eq. 3-31,
$$\Delta V_o = \Delta I_L (Z_Z||R_1) = 59.5\text{ mA} \times (7\ \Omega||150\ \Omega)$$
$$= 398\text{ mV}$$

3-23,
$$\text{Load regulation} = \frac{(\Delta E_o \text{ for } \Delta I_{L(max)}) \times 100\%}{E_o} = \frac{398\text{ mV} \times 100\%}{6.2\text{ V}}$$
$$= 6.4\%$$

Ripple rejection,

Eq. 3-30,

$$\frac{V_{ro}}{V_{ri}} = \frac{Z_Z \| R_L}{R_1 + (Z_Z \| R_L)} = \frac{7\ \Omega \| 104\ \Omega}{150\ \Omega + (7\ \Omega \| 104\ \Omega)}$$

$$= 4.19 \times 10^{-2}$$

Practise Problems

3-6.1 Design a 12 V *dc* reference source (consisting of a Zener diode and series-connected resistor) to operate from a 25 V supply. Determine the effect on the diode current when the supply drops to 22 V.

3-6.2 An 8 V *dc* reference source is to be designed to produce the maximum possible output current from a low-power Zener diode. The supply voltage is 20 V. Design the circuit and determine the maximum load current.

3-6.3 Calculate the line effect, load effect, and ripple rejection for the circuit designed in Problem 3-6.2.

3-7 Series Clipping Circuits

Series Clipper

The function of a *clipper* (or *limiter*) is to clip off an unwanted portion of a waveform. This is sometimes necessary to protect a device or circuit that might be destroyed by a large amplitude (negative or positive) signal.

A half-wave rectifier can be described as a clipper, because it passes only the positive (or negative) half-cycle of an alternating waveform and clips off the other half-cycle. In fact, a diode *series clipper* is simply a half-wave rectifier circuit.

Figure 3-25(a) shows a *negative series clipper circuit* with a square wave input symmetrical above and below ground level. While the input is positive, D_1 is forward biased and the positive half-cycle is passed to the output.

$$V_o = E - V_F \qquad \textbf{(3-32)}$$

During the negative half-cycle of the input, the diode is reverse biased. Consequently, the output remains at zero and the negative half-cycle is effectively clipped off.

The *zero level* output from a series clipper circuit is not exactly zero. The reverse saturation current (I_R) of the diode produces a voltage drop across resistor R_1,

$$V_o = -I_R R_1 \qquad \textbf{(3-33)}$$

This is almost always so small that it can be neglected.

If the diode in Fig. 3-25(a) is reconnected with reversed polarity, as shown in Fig. 3-25(b), the *positive* half-cycles are clipped off, and the circuit becomes a *positive series clipper*. The input waveforms to a clipper may be square, or sinusoidal, or any other shape.

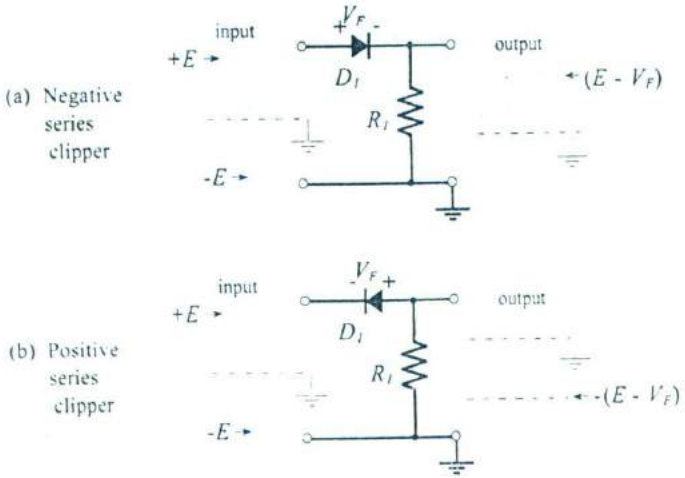


Figure 3-25
Diode series clipping circuits clip off unwanted portions of input waveforms. These are essentially half-wave rectifier circuits.

The output terminals of series clippers are usually connected to circuits that have a high input resistance, so (current-limiting) resistor R_1 is selected to pass an acceptable minimum current through the diode. This current must be sufficient to operated the diode beyond the *knee* of its forward characteristic. (see Fig. 2-4). Typically, a current of 1 mA is appropriate. The resistor value is calculated from the output voltage and the selected current level. The remaining part of the design process is specifying the diode.

Example 3-13

The negative series clipper in Fig. 3-26 has a ±9 V input, and zero load current. Determine a suitable resistance for R_1, and specify the diode forward current and reverse voltage. Use a silicon diode.

Solution

$$V_o = E - V_f = 9\text{ V} - 0.7\text{ V}$$
$$= 8.3\text{ V}$$

select $I_F = 1\text{ mA}$

$$R_1 = \frac{V_o}{I_f} = \frac{8.3\text{ V}}{1\text{ mA}}$$

$$= 8.3\text{ mA (use 8.2 k}\Omega\text{ standard value)}$$

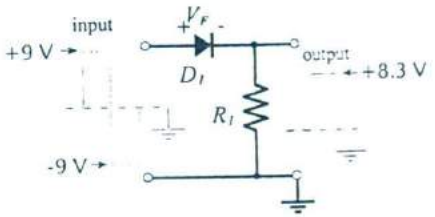


Figure 3-26
Series clipper circuit for Example 3-13.

Diode specification,

$$V_R = E = 9\text{ V}$$
$$I_f = 1\text{ mA}$$

Current Level Selection

In most electronic circuits it is best to select the smallest possible level of current. One reason for this is to keep the total supply current to a minimum. High supply currents require larger, more

expensive, power supplies than low current levels. Where a battery supply is used, batteries last longer with low supply current levels. Another reason to keep circuit current levels low whenever possible, is to minimise component power dissipations. Low power dissipation allows the smallest components to be used, and avoids circuit heating problems.

Series Noise Clipper

Digital signal waveforms sometimes have unwanted lower-level *noise* voltages. The noise can be removed by a *series noise clipping circuit*, which simply consists of two inverse-parallel connected diodes, as illustrated in Fig. 3-27. When the noise amplitude is much smaller than the diode forward voltage drop (V_F), and the signal amplitude is larger than V_F, the signals are passed and the noise is blocked. The signal peak output voltage is (E - V_F).

A *dead zone* of $\pm V_F$ exists around ground level in the output waveform, indicating that inputs must exceed $\pm V_F$ to pass to the output. For noise voltage amplitudes that approach $\pm V_F$, two diodes may be connected in series to give a larger dead zone.

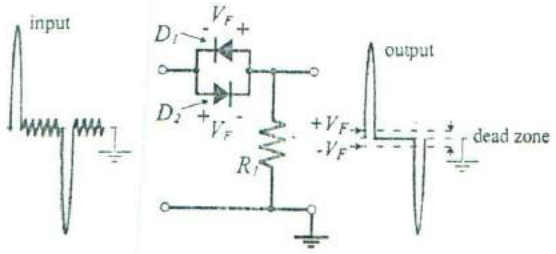


Figure 3-27
Series noise clipping circuit. Noise amplitudes lower than $\pm V_F$ cannot pass to the output.

Practise Problems

3-7.1 A positive series clipping circuit, as in Fig. 3-25(b), has a ±7 V input, and zero load current. Calculate a suitable resistance for R_1, and specify the diode.

3-7.2 A ±6 V square wave is applied via a series clipping circuit to a device that cannot survive +6 V. The device input current is 100 μA when its input voltage is negative. Select a suitable clipping circuit, determine the required resistance, and specify the diode.

3-8 Shunt Clipping Circuits

Shunt Clipper

A *positive shunt clipper circuit* is illustrated in Fig. 3-28(a). Here the diode is connected in *shunt* (or parallel) with the output terminals. When the input is negative, the diode is reverse biased and only a small voltage drop occurs across R_1, due to load current I_L. This means that the circuit output voltage (V_o) is approximately equal to the negative input peak (-E). When the input is +E, D_1 is forward biased, and the output voltage equals the diode voltage

drop ($+V_F$). Thus, the positive half of the waveform is clipped off. As illustrated, the upper and lower levels of the output of a positive shunt clipper are approximately $+V_F$ and $-E$.

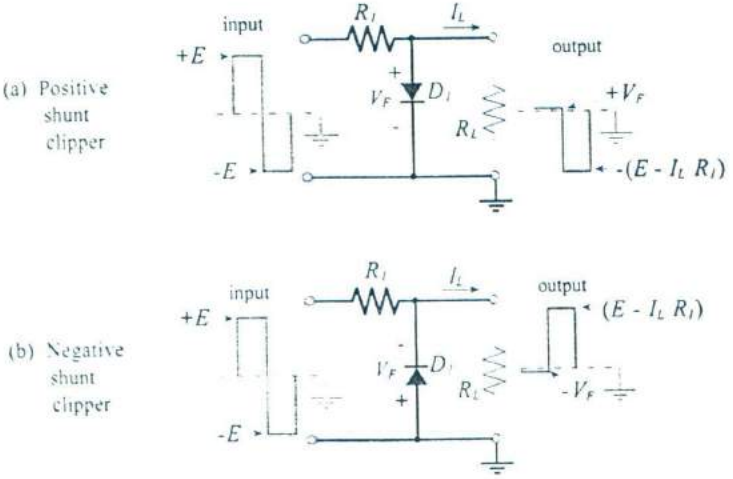


Figure 3-28
Shunt clipping circuits. The output voltage cannot exceed the diode voltage drop (V_F) when the input voltage forward biases the diode.

A *negative shunt clipper* circuit is exactly the same as a positive shunt clipper with the diode polarity reversed, [see Fig. 3-28(b)]. The negative half-cycle of the waveform is clipped off.

The load current on a shunt clipper produces a voltage drop ($I_L R_1$) across the resistor, which might be insignificant where the load current is very low.

$$V_o = E - (I_L R_1) \qquad \textbf{(3-34)}$$

As in the case of series clipping circuits, shunt clippers may be used with square, sinusoidal, or other input waveforms.

Example 3-14

The negative shunt clipper in Fig. 3-29 has a ±5 V input, and is to produce a +4.5 V minimum output when the load current is 2 mA. Determine a suitable resistance for R_1, and specify the diode forward current and reverse voltage.

Solution

When the diode is reverse biased,

Eq. 3-34, $V_o = E - (I_L R_1)$

or, $$R_1 = \frac{E - V_o}{I_L} = \frac{5\text{ V} - 4.5\text{ V}}{2\text{ mA}}$$

$$= 250\ \Omega \quad (\text{use } 220\ \Omega)$$

Diode reverse voltage,

$$V_R = E - 5\text{ V}$$

When the diode is forward biased,

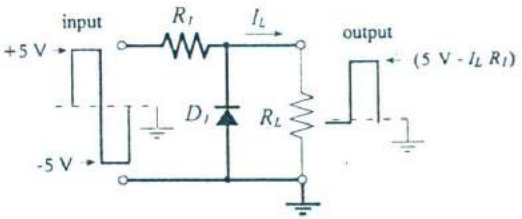


Figure 3-29
Negative shunt clipper for Example 3-14.

$$I_f = \frac{E - V_f}{R_1} = \frac{5\text{ V} - 0.7\text{ V}}{220\ \Omega}$$

$$= 19.5\text{ mA}$$

Shunt Noise Clipper

The *shunt noise clipper* shown in Fig. 3-30 removes noise riding on the peaks of an input waveform. The signal amplitude must be greater than the diode forward voltage drop. The output waveform is clipped at $\pm V_F$, so that the noise is not passed to the output. This type of clipper is used with pulse signals, where the pulse amplitude is not important. In this case, information is contained in the pulse width, or simply in its presence or absence.

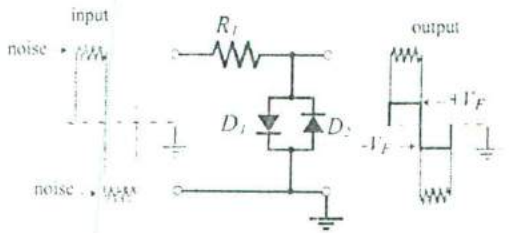


Figure 3-30
Shunt noise clipper circuit. Input amplitudes greater than $\pm V_F$ are clipped off.

Biased Shunt Clipper

Figure 3-31 shows a clipping circuit that uses two diodes which have different bias voltages. The cathode of D_1 is connected to a +2 V bias (V_{B1}), and the anode of D_2 has a -2 V bias (V_{B2}). While the input waveform amplitude is less than $\pm(V_B + V_F)$, neither diode is forward biased, and the input is simply passed to the output. When the positive input is greater than $(V_{B1} + V_F)$, D_1 becomes forward biased, and the output cannot exceed this voltage. Similarly, when the negative input goes below $(-V_{B2} - V_F)$, D_2 is forward biased, and the output is limited to $-(V_{B2} + V_F)$.

$$V_o = \pm(V_B + V_F) \qquad \textbf{(3-35)}$$

For obvious reasons, the circuit is termed a *biased shunt clipper*. Biased shunt clippers are used to protect circuits or devices from (positive/negative) input voltages that must not exceed specified levels.

The voltage across resistor R_1 is $(E - V_o)$, and the resistor current is the sum of the load current and the diode forward current $(I_L + I_F)$. As in other diode circuits, a minimum level of I_F is selected, and the resistor value is calculated as,

$$R_1 = \frac{E - V_o}{I_L + I_F} \qquad \textbf{(3-36)}$$

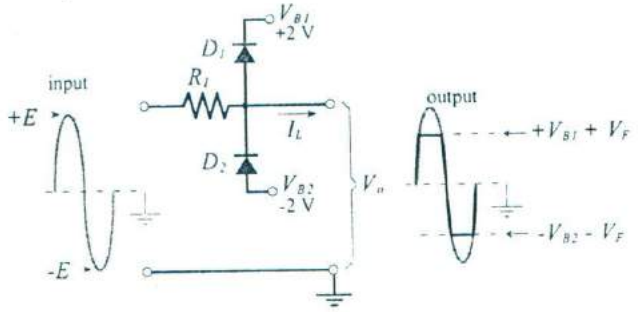


Figure 3-31
Biased shunt clipper circuit. Inputs amplitudes greater than $\pm(V_B + V_f)$ are clipped off.

Example 3-15

The biased shunt clipper in Fig. 3-31 has a ±9 V input, and its output is to be limited to ±2.7 V. Determine a suitable resistance for R_1 if the clipper output current is to be ±1 mA.

Solution

Eq. 3-35, $$V_o = \pm(V_B + V_f)$$

giving, $$V_B = \pm(V_o - V_f) = \pm(2.7\text{ V} - 0.7\text{ V}) = \pm 2\text{ V}$$

Select the diode forward current as,

$$I_f = 1\text{ mA}$$

Eq 3-36, $$R_1 = \frac{E - V_o}{I_L + I_F} = \frac{9\text{ V} - 2.7\text{ V}}{1\text{ mA} + 1\text{ mA}}$$

$$= 3.15\text{ k}\Omega \quad (\text{use } 2.7\text{ k}\Omega \text{ to give } I_f > 1\text{ mA})$$

Zener Diode Shunt Clipper

A *Zener diode shunt clipper* produces the same kind of result as a biased shunt clipper without the need for bias voltages. The clipper circuit in Fig. 3-32 has two back-to-back series-connected Zener diodes. When the input voltage is positive and has sufficient amplitude, D_1 is forward bias and D_2 is biased into reverse breakdown. At this time, the output voltage is limited to $(V_F + V_{Z2})$. A negative input voltage produces a maximum negative output of $-(V_F + V_{Z1})$. With equal-voltage Zener diodes, the maximum output voltage is,

$$\mathbf{V_o = \pm(V_F + V_Z)} \qquad \textbf{(3-37)}$$

The resistor voltage is $(E - V_o)$, and the resistor current is $(I_L + I_Z)$. A minimum level of I_Z (greater than the device knee current) is selected, and the resistor value is calculated as,

$$\mathbf{R_1 = \frac{E - V_o}{I_L + I_Z}} \qquad \textbf{(3-38)}$$

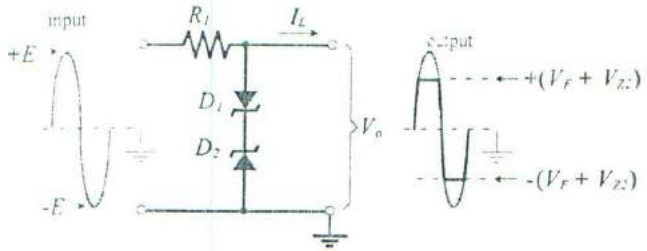


Figure 3-32
Zener diode shunt clipper circuit. Inputs amplitudes greater than $\pm(V_F + V_Z)$ are clipped off.

Example 3-16

A Zener diode shunt clipper, as in Fig. 3-32, is to be connected between a ±20 V square wave signal and a circuit which cannot accept inputs greater than ±5 V. Select suitable Zener diodes, and determine R_1. The clipper output current is to be ±1 mA.

Solution

From Eq. 3-37, $V_Z = V_o - V_F = 5\text{ V} - 0.7\text{ V}$
$= 4.3\text{ V}$

From Appendix 1-4, the 1N749 has $V_Z = 4.3$ V. Use 1N749 Zener diodes.

Select, $I_{Z(min)} = 5\text{ mA}$

Eq. 3-38, $$R_1 = \frac{E - V_o}{I_L + I_Z} = \frac{20\text{ V} - 5\text{ V}}{1\text{ mA} + 5\text{ mA}}$$
$= 1.86\text{ k}\Omega$ (use 1.8 kΩ to give $I_Z > 5$ mA)

Practise Problems

3-8.1 A positive shunt clipper, as in Fig. 3-28(a), has a ±7 V input. The negative output voltage is to be 6.5 V when the load current is 1.5 mA. Calculate the required resistance for R_1, and specify the diode forward current and reverse voltage.

3-8.2 A ±8 V square wave is applied to a device that cannot accept inputs greater than ± 3.5 V. The device input current is ± 600 μA. Design a suitable biased shunt clipping circuit.

3-8.3 A Zener diode shunt clipping circuit is to be used to clip a ±18 V square wave off at approximately ±7 V. The output current is to be ±1.2 mA. Design the circuit.

3-9 *Clamping Circuits*

Negative and Positive Voltage Clamping Circuits

A *clamping circuit*, also known as a *dc restorer*, changes the *dc* voltage level of a waveform, but does not affect its shape. Consider the clamping circuit shown in Fig. 3-33. When the square wave

input is positive, diode D_1 is forward biased, and the output voltage equals the diode forward voltage drop (V_F).

$$V_o = V_F \tag{3-39}$$

During the positive half-cycle of the input, the voltage on the right side of the capacitor is $+V_F$, while that on the left side is $+E$. Thus, C_1 is charged with the polarity shown to a voltage,

$$V_C = (E - V_F) \tag{3-40}$$

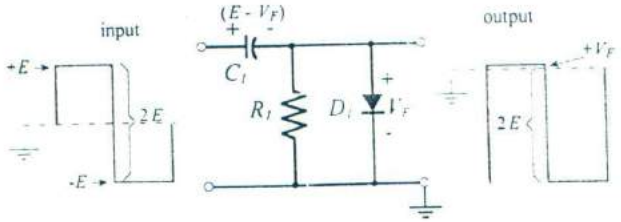


Figure 3-33
A negative voltage clamping circuit passes the complete input waveform to the output, but clamps the positive peak of the output close to ground level.

When the input goes negative, the diode is reverse biased and has no further effect on the capacitor voltage. Also, R_1 has a very high resistance, so that it cannot discharge C_1 significantly during the negative portion of the input waveform. While the input is negative, the output voltage is the sum of the input and capacitor voltages. Since the polarity of the capacitor voltage is the same as the (negative) input, the output is,

$$\begin{aligned} V_o &= -(E + V_c) \\ &= -[E + (E - V_F)] \end{aligned}$$

or,

$$V_o = -[2E - V_F] \tag{3-41}$$

The peak-to-peak output voltage ($V_{o(pp)}$) is the difference between the positive output peak (V_F) and negative output peak $-(2E - V_F)$.

$$V_{o(pp)} = V_F - [-(2E - V_F)]$$

or,

$$V_{o(pp)} = 2E \tag{3-42}$$

It is seen that the peak-to-peak amplitude of the output waveform from the clamping circuit is exactly the same as the peak-to-peak input. Instead of the waveform being symmetrical above and below ground, however, the output positive peak is clamped at a level of $+V_F$.

The circuit in Fig. 3-33 is known as a *negative voltage clamping circuit*, because the output waveform is (almost) completely negative. Reversing the polarity of the diode and capacitor in Fig. 3-33 creates the *positive voltage clamping circuit* shown in Fig. 3-34. As illustrated, the output waveform is clamped to keep it (almost) completely positive.

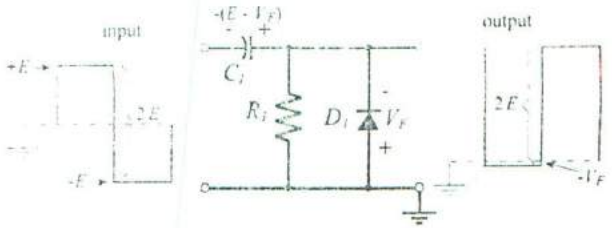


Figure 3-34
A positive voltage clamping circuit passes the complete input waveform to the output, but clamps the negative peak of the output close to ground level.

Output Slope

Resistor R_1 in Figs. 3-33 and 3-34 is sometimes termed a *bleeder resistor*. Its function is to gradually discharge the capacitor over several cycles of input waveform, so that it can be charged to a new voltage level if the input changes. However, R_1 partially discharges the capacitor during the time that D_1 is reverse biased, and this produces a *slope*, or *tilt* (ΔV_c) on the output waveform, as illustrated in Fig. 3-35. The tilt voltage can be calculated from a knowledge of the waveform frequency and the circuit component values. The constant-current equation for charging or discharging a capacitor may be applied.

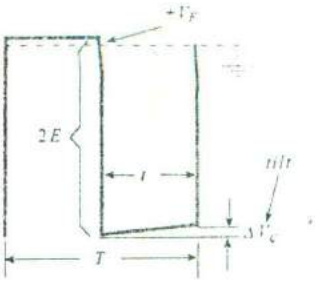


Figure 3-35
The output voltage from a clamping circuit has a slope (ΔV_c) produced by capacitor discharge.

$$\Delta V_c = \frac{I_c \times t}{C_1} \qquad \textbf{(3-43)}$$

Example 3-17

The diode clamping circuit in Fig. 3-36, has ±10 V, 1 kHz square wave input. Calculate the tilt on the output waveform.

Solution

While the diode is reverse biased,

$$V_{o(pp)} = 2E = 2 \times 10\ \text{V} = 20\ \text{V}$$

and,

$$I_c \approx \frac{V_{o(pp)}}{R_1} = \frac{20\ \text{V}}{56\ \text{k}\Omega} = 367\ \mu\text{A}$$

$$t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 1\ \text{kHz}} = 500\ \mu\text{s}$$

Eq. 3-43,

$$\Delta V_C = \frac{I_c \times t}{C_1} = \frac{367\ \mu\text{A} \times 500\ \mu\text{s}}{1\ \mu\text{F}} = 184\ \text{mV}$$

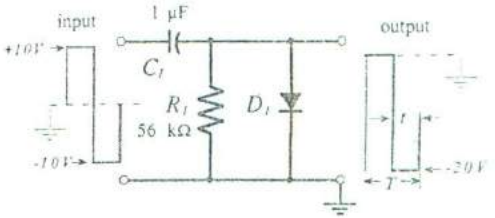


Figure 3-36
Clamping circuit for Ex. 3-17.

Component Determination

When designing a clamping circuit, capacitor C_1 is selected so that it becomes completely charged in approximately five cycles of the input waveform. As already discussed (and illustrated in Fig. 3-37), diode D_1 is forward biased when C_1 is being charged. Resistor R_1 is

not part of the C_1 charging circuit, because D_1 bypasses R_1. As illustrated, C_1 charge is controlled by the signal source resistance (R_S). A capacitor is completely charged in approximately five time constants of the circuit. In the case of a resistor-capacitor circuit, the time constant is RC. So, the charging time is,

$$5\,RC = 5 \times [\textit{input pulse width } (PW)]$$

or,
$$RC = PW$$

This gives,
$$\boldsymbol{C_1 R_S = PW} \qquad \textbf{(3-44)}$$

When the pulse width and source resistance of the input waveform is known, C_1 can be determined from Eq. 3-44.

So long as the slope on the output waveform is very small, the capacitor discharge current is essentially a constant quantity.

$$I_C = \frac{V_o}{R_1}$$

or,
$$\boldsymbol{I_C = \frac{2E}{R_1}} \qquad \textbf{(3-45)}$$

When the output waveform slope is specified, I_C can be calculated from Eq. 3-43, and a suitable resistance for R_1 is then determined by substituting I_C into Eq. 3-45.

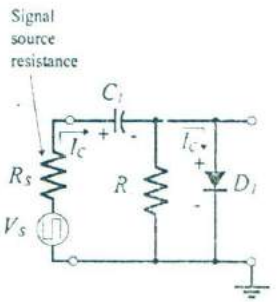


Figure 3-37
Capacitor C_1 is charged via signal source resistance R_S.

Example 3-18

The negative voltage clamping circuit in Fig. 3-38, has a ±8 V, 500 Hz square wave input with a 600 Ω signal source resistance. The output waveform is to have a maximum slope of 1%. Determine suitable values for R_1 and C_1.

Solution

$$t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 500\ \text{Hz}}$$

$$= 1\ \text{ms}$$

$$PW = t = 1\ \text{ms}$$

From Eq. 3-44,
$$C_1 = \frac{PW}{R_S} = \frac{1\ \text{ms}}{600\ \Omega}$$

$$= 1.7\ \mu\text{F}\ (\text{use } 1.8\ \mu\text{F})$$

$$V_{o(PP)} = 2E = 2 \times 8\ \text{V}$$
$$= 16\ \text{V}$$

$$\Delta V_C = 1\%\ \text{of}\ V_{o(PP)} = 1\%\ \text{of}\ 16\ \text{V}$$
$$= 0.16\ \text{V}$$

From Eq. 3-43,
$$I_c = \frac{\Delta V_C\, C_1}{t} = \frac{0.16\ \text{V} \times 1.8\ \mu\text{F}}{1\ \text{ms}}$$
$$= 288\ \mu\text{A}$$

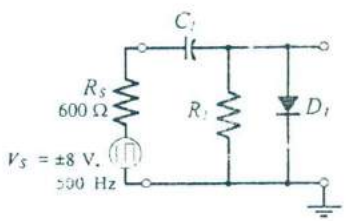


Figure 3-38
Clamping circuit for Ex. 3-18.

From Eq. 3-45, $R_1 = \frac{2E}{I_c} = \frac{16\,V}{288\,\mu A}$

$= 55.5\ k\Omega$ (use 56 kΩ)

Biased Clamping Circuit

The *biased clamping circuit* shown in Fig. 3-39 has a bias voltage (V_B) at the cathode of diode D_1. In this case, the output voltage cannot exceed ($V_{B1} + V_F$), as illustrated. The capacitor charges to ($E - V_{B1} - V_F$) when the input is positive. When the input goes negative, the output voltage is $-(E + V_C)$, giving.

$$V_o = -[E + (E - V_{B1} - V_F)]$$
$$= -2E + V_{B1} + V_F$$

The peak-to-peak output voltage is the difference between the positive and negative output peak levels.

$$V_o = (V_{B1} + V_F) - [-2E + V_{B1} + V_F]$$
$$= 2E$$

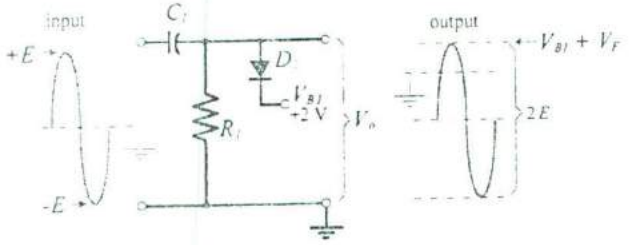


Figure 3-39
A biased clamping circuit clamps one peak of the output voltage at a selected level.

It is seen that, as for other clamping circuits, the peak-to-peak output waveform from the biased clamper is the same as the input. The positive level of the output is clamped to ($V_B + V_F$).

Virtually any bias voltage level (positive or negative) can be used with a biased clamping circuit. The diode polarity determines whether the positive or the negative peak of the output is clamped. Care must be taken to ensure that the capacitor is connected with the correct polarity. Biased clamping circuits are designed in exactly the same way as unbiased clamping circuits.

Example 3-19

Determine the upper and lower levels of the output voltage for the circuits shown in Fig. 3-40 when the input voltage is ±6 V. Also, calculate the capacitor voltage in each case.

Solution

For Fig. 3-40(a),
D_1 is forward biased when the input goes negative.

When the input is -E, $V_C = V_{B1} - V_F - E = 3\text{ V} - 0.7\text{ V} - (-6\text{ V})$
$= 8.3\text{ V}$ (+ on the right)

$V_o = V_{B1} - V_f = 3\text{ V} - 0.7\text{ V}$
$= 2.3\text{ V}$ (low level of output)

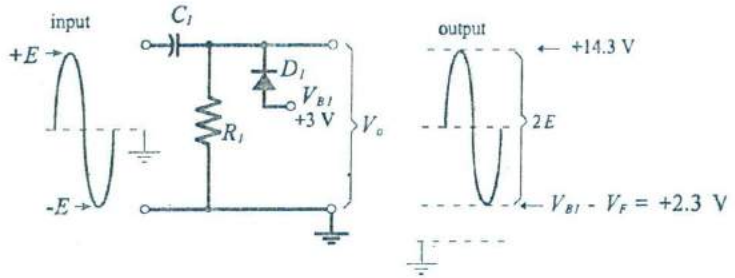
When the input is +E, $V_o = E + V_C = 6\text{ V} + 8.3\text{ V}$
$= 14.3\text{ V}$ (high level of output)

For Fig. 3-40(b),
D_1 is forward biased when the input goes positive.

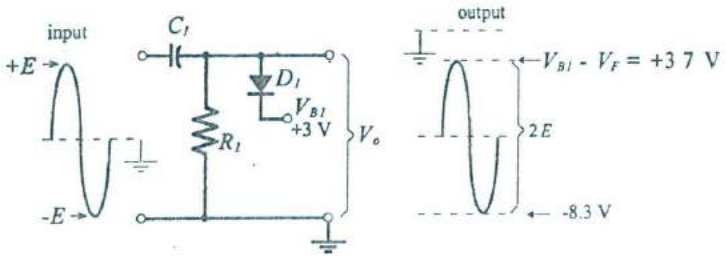
When the input is +E, $V_C = E - V_{B1} - V_F = 6\text{ V} - 3\text{ V} - 0.7\text{ V}$
$= 2.3\text{ V}$ (+ on the left)

$V_o = V_{B1} + V_f = 3\text{ V} + 0.7\text{ V}$
$= 3.7\text{ V}$ (high level of output)

When the input is -E, $V_o = E + V_C = -6\text{ V} - 2.3\text{ V}$
$= -8.3\text{ V}$ (low level of output)



(a) Output voltage cannot go below $V_{B1} - V_F$



(b) Output voltage cannot go above $V_{B1} - V_F$

Figure 3-40
Biased clamping circuits use positive or negative bias voltages to clamp the level of one of the peaks of the output waveform.

Zener Diode Clamping Circuit

Zener diode clamping circuits operate just like biased voltage clampers, with the Zener diode voltage (V_Z) substituting for the bias voltage. The circuit in Fig. 3-41 has an ordinary diode (D_1) connected in series with a Zener diode (D_2). When the input voltage is at its positive peak, the output voltage is.

$$V_o = V_Z + V_F$$

and C_1 charges (+ on the left) to.

$$V_C = E - (V_Z + V_F)$$

When the input goes to its negative peak, the output voltage is.

$$V_o = -(E + V_C)$$
$$V_o = -[E + (E - (V_Z + V_F)]$$
$$= -(2E - V_Z - V_F)$$

The peak-to-peak output remains equal to the peak-to-peak input voltage ($2E$). If the polarity of the diodes (and the capacitor) are reversed, the negative output peak is clamped at $-(V_Z + V_F)$.

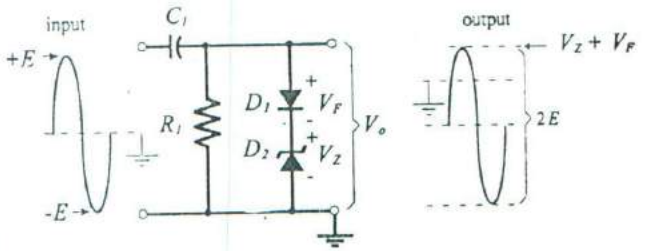


Figure 3-41
Zener diode clamping circuits clamp the output voltage at (V_z + V_f). The positive peak or the negative peak can be clamped above or below ground

Practise Problems

3-9.1 A ±8 V, 300 Hz square wave is applied to the clamping circuit in Fig. 3-34. If C_1 = 1.5 μF and R_1 = 33 kΩ, determine the tilt voltage on the output waveform.

3-9-2 A positive voltage clamping circuit, as in Fig. 3-34, is to have an output waveform with a maximum of 0.5% tilt. The signal is a ±7 V, 1 kHz square wave with a 500 Ω source resistance. Calculate suitable values for R_1 and C_1.

3-9.3 A clamping circuit, as in Fig. 3-41, uses a *1N754* Zener diode. Determine the upper and lower levels of the output voltage if the input is a ±12 V square wave. Also, calculate the capacitor voltage.

3-10 DC Voltage Multipliers

Voltage Doubler

A *voltage doubling circuit* produces an output voltage which is

approximately double the peak voltage of the input waveform. Consideration of the voltage doubling circuit in Fig. 3-42 shows that it is simply a combination of two diode-capacitor clamping circuits without the discharge resistors. In fact, the circuit operation is similar to that of clamping circuits.

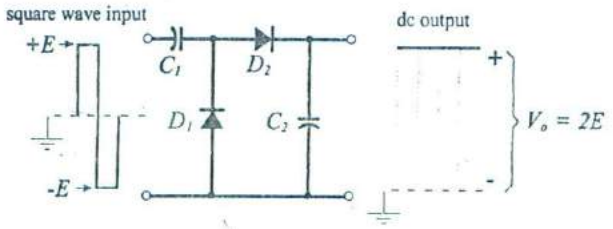


Figure 3-42
A voltage doubling circuit produces a dc output voltage which is approximately double the peak input voltage.

When the input voltage is negative, as shown in Fig. 3-43(a), diode D_1 is forward biased, and C_1 charges to $(E - V_{F1})$ with the polarity illustrated. D_2 is reverse biased during the negative half-cycle of the input, so the charge on C_2 is not affected at this time.

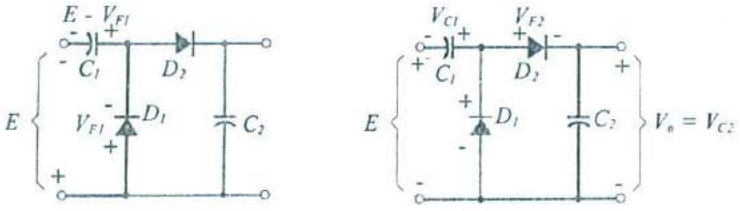
Figure 3-43(b) shows what occurs during the input positive half-cycle. D_1 is now reverse biased, and D_2 is forward biased. The voltage applied to D_2 and C_2 is the sum of the input voltage and the voltage on C_1. So, as illustrated, capacitor C_2 is charged to,

$$\begin{aligned} V_{C2} &= E + V_{C1} - V_{F2} \\ &= E + (E - V_{F1}) - V_{F2} \\ &= 2(E - V_F) \end{aligned}$$

so,

$$\boldsymbol{V_o = 2(E - V_F)} \qquad \textbf{(3-46)}$$

It is seen that, when the diode voltage drop is much smaller than the input voltage, the output is approximately double the peak input amplitude. The polarity of the output voltage can be reversed by reversing the polarity of the diodes and capacitors.



(a) C_1 charges while E is negative (b) C_2 charges while E is positive

Figure 3-43
Capacitor C_1 charges to $(E - V_{F1})$ during the negative half-cycle of the input. Then, $+[E + (E - V_{F1}) - V_{F2}]$ is passed to C_2 during the input positive half-cycle.

The output terminals of the voltage doubler are the terminals of capacitor C_2. The load current partially discharges the capacitors, producing an output voltage drop in the same way that tilt is created on a clamping circuit output. The repeated charge and discharge of C_1 and C_2 results in a ripple waveform on the output.

A sinusoidal input waveform to a voltage doubler produces exactly the same type of output ripple that occurs with a half-wave rectifier, [Fig. 3-44(a)]. However, the input most often used is a *dc* voltage source which has been *chopped*, or converted into a square waveform, [Fig. 3-44(b)].

Capacitor C_2 supplies the load current (I_L) while diode D_2 is reverse biased, [Fig. 3-45(a)]. The discharge of C_2 accounts for half the output ripple voltage amplitude, and the discharge of C_1 produces the other half of the ripple amplitude. Equation 3-43 can be modified for calculating the capacitance of C_2.

$$C_2 = \frac{I_L\, t}{\Delta V_C} \qquad (3\text{-}47)$$

While D_2 is forward biased [Fig. 3-45(b)], capacitor C_1 supplies I_L and the recharging current to C_2. The recharging current must equal I_L to maintain the full charge on C_2, so C_1 supplies $2I_L$. Applying Eq. 3-43 to calculate C_1, it is found that,

$$C_1 = 2C_2 \qquad (3\text{-}48)$$

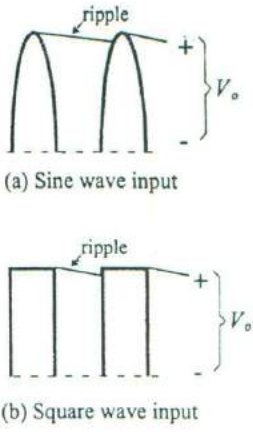


Figure 3-44
A ripple waveform occurs at the output of a voltage doubler.

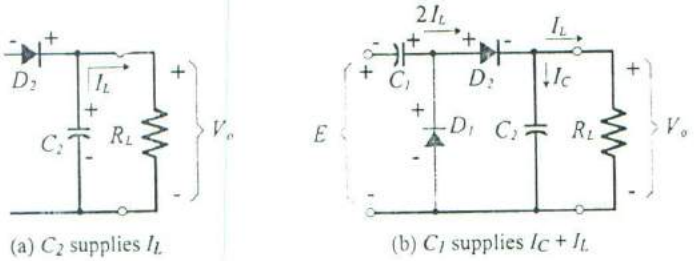


Figure 3-45
Capacitor C_2 supplies I_L while diode D_2 is reverse biased, and C_1 supplies $2I_L$ when D_2 is forward biased.

Example 3-20

Determine C_1 and C_2 for the voltage doubling circuit in Fig. 3-46 to produce a 1% maximum output ripple. The input is a ±12 V, 5 kHz square wave.

Solution

Eq. 3-46,
$$V_o = 2(E - V_f) = 2(12\text{ V} - 0.7\text{ V}) = 22.6\text{ V}$$

$$I_L = \frac{V_o}{R_L} = \frac{22.6\text{ V}}{47\text{ k}\Omega} = 481\ \mu\text{A}$$

Capacitor discharge time,
$$t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 5\text{ kHz}} = 100\ \mu\text{s}$$

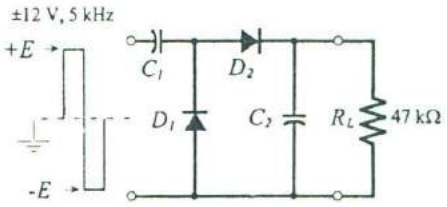


Figure 3-46
Diode voltage doubling circuit for Ex. 3-20.

For 1% output ripple, allow 0.5% due to discharge of C_2 and 0.5% due to discharge of C_1.

$$\Delta V_C = 0.5\%\text{ of } V_{o(PP)} = 0.5\%\text{ of } 22.6\text{ V} = 113\text{ mV}$$

Eq. 3-47, $$C_2 = \frac{I_L t}{\Delta V_C} = \frac{481\ \mu A \times 100\ \mu s}{113\ mV}$$

$$= 0.43\ \mu F \text{ (use } 0.47\ \mu F)$$

Eq. 3-48, $$C_1 = 2\,C_2 = 2 \times 0.47\ \mu F$$

$$= 0.94\ \mu F \text{ (use } 1\ \mu F)$$

Multistage Voltage Multipliers

A four-stage *dc* voltage multiplier is shown in Fig. 3-47. Comparing to the voltage doubler in Fig. 3-42, it is seen that this circuit consists of two cascade-connected voltage doubling circuits. To simplify the explanation of the circuit operation, assume ideal diodes with $V_F = 0$.

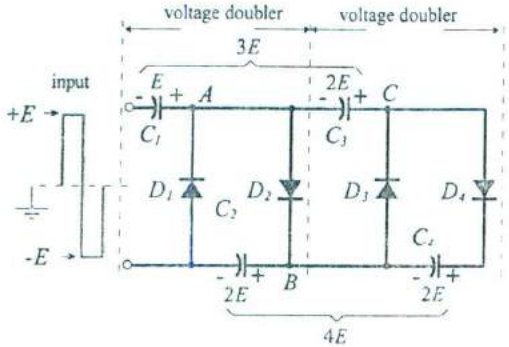


Figure 3-47
Four stage dc voltage multiplying circuit. Neglecting the diode voltage drops, C_1 is charged to E volts, and all other capacitors are charged to approximately 2E. The final output is 4E volts.

- When $V_i = -E$; D_1 is forward biased, and C_1 charges via D_1 to E.
- When $V_i = +E$; point A is at $+2E$, D_1 is reverse biased, D_2 is forward biased, C_2 charges via D_2 to $2E$.
- When $V_i = -E$; point A is close to ground level, point B is at $2E$ (because of V_{C2}), D_2 is reverse biased, D_3 is forward biased, and C_3 charges via D_3 to $2E$ volts.
- When $V_i = +E$; point A is at $+2E$, point B is at $+2E$, and point C is at $+4E$, D_4 is forward biased, and C_4 charges via D_4 to $2E$ volts.

The resulting output voltage, taken across C_2 and C_4 is $4E$ volts, as illustrated. Additional stages may be added to the circuit to produce higher levels of *dc* output voltage. Figure 3-48 shows another way that *dc* voltage multiplier circuit diagrams are often drawn. Examination of the circuit shows that it is exactly the same as Fig. 3-47.

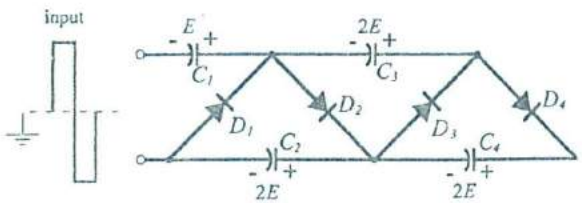


Figure 3-48
Another way of drawing the circuit of a four-stage dc voltage multiplier circuit.

Practise Problems

3-10.1 For the circuit designed in Example 3-20, determine the effect on the output ripple; (a) when R_L is changed to 27 kΩ, (b) when the input square wave frequency is increased to 7 kHz.

3-10.2 A voltage doubling circuit with a 39 kΩ load resistor is to have a 20 V output. Determine the required amplitude for a 700 Hz square wave input, and calculate suitable capacitor values to produce a 0.2 V maximum output ripple. Use silicon diodes.

3-11 Diode Logic Circuits

AND Gate

A logic circuit produces an output voltage which is either *high* or *low*, depending upon the levels of several input voltages. The two basic logic circuits are the *AND* gate and the *OR* gate.

Figure 3-49 shows the circuit diagram of a diode *AND* gate. It is seen that the diode anodes are connected to a 5 V supply (V_{CC}) via resistor R_1. The circuit has a single output terminal at the diode anodes, and three input terminals at the device cathodes. (An *AND* gate could have any number of inputs from 2 up to perhaps 50.)

If one (or more) of the input terminals is grounded, current flows from the supply through R_1 and through the forward-biased diode to ground. In this case, the output voltage is just V_F above ground, (0.7 V for silicon). The output is said to be at a *low* level. When input levels of 5 V are applied to all three input terminals, none of the diodes is forward biased, no resistor current flows, and no significant voltage drop occurs across R_1. Thus, the output voltage is equal to V_S, and it is referred to as a *high* output level.

*An AND gate produces a high output only when input A is high, **AND** input B is high, **AND** input C is high.*

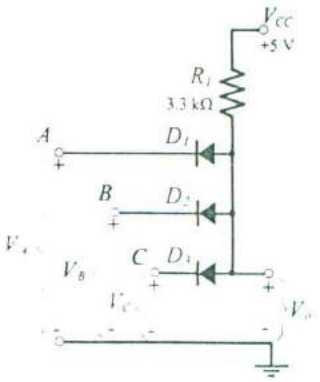


Figure 3-49
*Circuit of a three-input diode **AND** gate. A high output occurs only when high inputs are present at input A, **and** input B, **and** input C.*

Example 3-21

For the *AND* gate circuit in Fig. 3-49, determine each diode forward current level, (a) when all three inputs are *low*, (b) when only input *A* is *high*, (c) when inputs *A* and *B* are both *high*, and *C* is *low*.

Solution

(a)
$$I_{R1} = \frac{V_{CC} - V_F}{R_1} = \frac{5\text{ V} - 0.7\text{ V}}{3.3\text{ k}\Omega}$$
$$= 1.3\text{ mA}$$

For each diode,
$$I_F = \frac{I_{R1}}{3} = \frac{1.3\text{ mA}}{3}$$
$$= 433\ \mu\text{A}$$

(b) $I_{R1} = 1.3$ mA (as above)

$$I_{F2} = I_{F3} = \frac{I_{R1}}{2} = \frac{1.3\text{ mA}}{2}$$
$$= 650\,\mu\text{A}$$

(c) $I_{F3} = I_{R1} = 1.3$ mA

OR Gate

The circuit diagram of an *OR* gate with three input terminals is shown in Fig. 3-50. Like the *AND* gate, the *OR* gate could have two or more inputs. It is obvious that the output voltage (V_o) of the *OR* gate in Fig. 3-50 is *low* when all three inputs are *low*. Now suppose that a +5 V input is applied to terminal *A*, while terminals *B* and *C* remain grounded. Diode D_1 becomes forward biased, and its cathode voltage is $V_o = (5\text{ V} - V_F)$. The gate output voltage is *high*, and diodes D_2 and D_3 are reverse biased with $+V_o$ at the cathodes and ground at the anodes. The output will be *high* if a *high* input voltage is applied to any one (or more) of the inputs.

An OR gate produces a high output when input A is high, ***OR*** *or when input B is high,* ***OR*** *when input C is high.*

Diode *AND* and *OR* gates can be designed and constructed using discrete components. However, *integrated-circuit* (*IC*) packages are available containing many diodes already fabricated in the form of one or more gates.

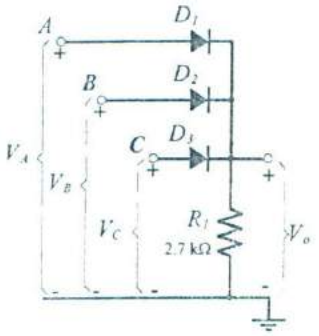


Figure 3-50
Circuit of a three-input OR gate. A high output occurs when high inputs are present at input A, ***or*** *at input B,* ***or*** *at input C.*

Practise Problems

3-11.1 The diodes in the *AND* gate in Fig. 3-49 are each to have a 2 mA maximum forward current. Calculate the required resistance for R_1.

3-11.2 Calculate the maximum and minimum levels of diode forward current for the *OR* gate in Fig. 3-50 when $V_i = 4.5$ V, and $R_1 = 2.7$ kΩ.

Chapter-3 Review Questions

Section 3-1

3-1 Sketch a half-wave rectifier circuit showing input and output waveforms, and explain the circuit operation.

Section 3-2

3-2 Sketch a two-diode full-wave rectifier circuit showing input and output waveforms. Explain the circuit operation.

3-3 Draw the circuit diagram for a bridge rectifier, together with its input and output waveforms. Carefully explain the operation of the bridge rectifier circuit, identifying the forward-biased and reverse-biased diodes during each half-wave of the input waveform.

Section 3-3

3-4 Draw the circuit diagram for a *dc* power supply that uses a half-wave rectifier and a capacitor filter circuit. Sketch the output waveform, and explain the circuit operation.

3-5 For a rectifier circuit with capacitor filtering, explain: ripple voltage, repetitive surge current, non-repetitive surge current, diode peak reverse voltage.

Section 3-4

3-6 Draw the circuit diagram for a *dc* power supply that uses a bridge rectifier and a capacitor filter circuit. Sketch the output waveform, and explain the circuit operation.

3-7 Compare half-wave and full-wave rectifier circuits with capacitor filtering, referring to capacitor size for a given ripple amplitude, and regarding diode specification.

Section 3-5

3-8 Define power supply source effect and load effect, and write equations for each. Also, write equations for line regulation and load regulation.

Section 3-6

3-9 Sketch the circuit diagram for a Zener diode voltage regulator. Briefly explain the circuit operation, and discuss the effects of load current.

3-10 Sketch the *ac* equivalent circuit for a Zener diode voltage regulator. Write equations for source effect and load effect.

Section 3-7

3-11 Draw circuit diagrams for negative and positive series clipping circuits. Show input and output waveforms and explain the operation of each circuit.

3-12 Sketch the circuit of a diode series noise clipper circuit, and explain its application.

Section 3-8

3-13 Draw circuit diagrams for negative and positive shunt clipping circuits. Show input and output waveforms, and explain the operation of each circuit.

3-14 Sketch a shunt noise clipping circuit, and explain its application.

3-15 Draw a biased shunt clipping circuit. Sketch input and output waveforms, and explain the circuit operation.

3-16 A biased shunt clipper has ±9 V bias voltages. Sketch the output waveform produced by a ±12 V square wave input.

3-17 Draw a diagram for a Zener diode shunt clipping circuit, and explain its application.

Section 3-9

3-18 Explain the difference between clipping circuits and clamping circuits. A positive voltage clamping circuit and a positive voltage clipping circuit each have a ±12 V square wave input. Sketch the output waveform from each circuit.

3-19 Draw circuit diagrams for negative and positive voltage clamping circuits. Show input and output waveforms, and explain the operation of each circuit.

Section 3-10

3-20 Draw a voltage doubling circuit. Sketch input and output waveforms, and explain the circuit operation.

3-21 Draw the circuit diagram for a four-stage voltage multiplier circuit. Briefly explain its operation, and identify the output terminals and the output voltage level relative to the input. Show how two additional diode-capacitor circuits may be added, and estimate the new output-to-input voltage ratio.

Section 3-11

3-22 Sketch the circuit diagram for a diode AND gate with five input terminals. Briefly explain the circuit operation.

3-23 Sketch the circuit diagram for a diode OR gate with five input terminals. Briefly explain the circuit operation.

Chapter-3 Problems

Section 3-1

3-1 A half-wave rectifier circuit has a 25 V (*rms*) sinusoidal *ac* input and a 600 Ω load resistance. Calculate the peak output voltage, peak load current, and diode peak reverse voltage. Assume $V_F = 0.7$ V.

3-2 A half-wave rectifier circuit produces a 55 mA peak current in an 820 Ω load resistor. Calculate the *rms ac* input voltage, and the diode peak reverse voltage if $V_F = 0.7$ V.

3-3 Calculate the power dissipated in a 560 Ω load resistor connected to the output of a half wave rectifier circuit. The *ac* input is 25 V (*rms*), and the diode voltage drop is 0.7 V.

Section 3-2

3-4 A 470 Ω load resistor is connected at the output of a bridge rectifier circuit that has a 15 V (*rms*) input. Calculate the peak output voltage, peak load current, and load power dissipation, if the rectifiers have 0.3 V forward voltage drop.

3-5 A bridge rectifier circuit has a 25 V (*rms*) sinusoidal *ac* input and a 600 Ω load resistance. Calculate the peak output voltage, peak load current, diode power dissipation, and diode peak reverse voltage. Assume $V_F = 0.7$ V.

3-6 A two-diode full-wave rectifier circuit (as in Fig. 3-2) dissipates 640 mW in a 400 Ω load resistor. If the diodes are silicon, calculate the peak output voltage from each half of the transformer secondary.

Section 3-3

3-7 A *dc* power supply consisting of a half-wave rectifier and a reservoir capacitor is required to supply 24 V with a 200 mA maximum load current. The output ripple is not to exceed ±500 mV, and the *ac* input frequency is 60 Hz. Determine a suitable capacitance for the reservoir capacitor.

3-8 Recalculate the capacitance approximately for the circuit in Problem 3-7, assuming that the capacitor discharge time is much greater than the charge time.

3-9 Specify the diodes required for the half-wave rectifier circuit in Problem 3-7. Select a suitable device from Appendix 1, and calculate the required surge limiting resistance.

3-10 Calculate the reservoir capacitance for a half-wave rectifier *dc* power supply which produces a 15 V output with a 300 mA maximum load current. The peak-to-peak output ripple voltage is to be a maximum of ±10% of V_o, and the *ac* input frequency is 60 Hz.

3-11 Specify the diodes required for the power supply in Problem 3-10. Select a suitable device from Appendix 1, and calculate the required surge limiting resistance.

3-12 Recalculate the capacitance for the power supply in Problem 3-10 for a 400 Hz *ac* supply.

Section 3-4

3-13 A *dc* power supply consisting of a bridge rectifier circuit and a reservoir capacitor is to supply 24 V with a 200 mA maximum load current. The output ripple is not to exceed ±500 mV, and the *ac* input frequency is 60 Hz. Determine a suitable capacitance for the reservoir capacitor.

3-14 Recalculate the capacitance for the circuit in Problem 3-13, using the approximation that the capacitor discharge time is much greater than the charge time.

3-15 Specify the diodes required for the rectifier circuit in Problem 3-13. Select a suitable device from Appendix 1, and calculate the required surge limiting resistance.

3-16 Calculate the reservoir capacitance for a *dc* power supply which produces an 18 V output with a 300 mA maximum load current. A bridge rectifier circuit is used and the *ac* input frequency is 60 Hz. The peak-to-peak output ripple voltage is to be a maximum of ±10% of V_o.

3-17 Specify the diodes required for the power supply in Problem 3-16. Select a suitable device from Appendix 1, and calculate

the required surge limiting resistance.

3-18 Recalculate the capacitance for the power supply in Problem 3-16 for a 400 Hz *ac* supply.

Section 3-5

3-19 A *dc* power supply output voltage changes from 12 V to 11.6 V when the input drops by 10%, and from 12 V to 11.5 V when the load current increases from zero to maximum. Determine the source and load effects, and the line and load regulations.

3-20 A *dc* power supply with a 20 V output has a 3% line regulation and a 5% load regulation. Calculate the source effect and the load effect.

3-21 Calculate the line and load regulation for the circuit designed in Problem 3-7.

3-22 Calculate the line and load regulation for the circuit designed in Problem 3-16.

Section 3-6

3-23 A series-connected Zener diode and resistor is to be used as a 10 V reference source with a load current less than 1 mA. The available supply voltage is 25 V. Select suitable components, and calculate the effect of a ±10% supply voltage change on the diode current.

3-24 A 5 V Zener diode voltage source is to be designed to produce maximum possible output current from a low-power Zener diode. Design the circuit to operate from an 22 V supply, and calculate the maximum load current.

3-25 Determine the source effect, load effect, and ripple rejection for the circuit designed in Problem 3-24.

3-26 Recalculate the maximum output current for the circuit designed in Problem 3-24 when the ambient temperature is raised to 100°C. The diode derating factor is 3.2 mW/°C for temperatures above 50°C.

3-27 A *1N751* Zener diode is connected in series with a 330 Ω resistor to a 25 V supply. Determine the maximum and minimum level of the Zener diode voltage, and calculate the minimum resistance that may be connected in parallel with the diode.

3-28 Calculate the source effect, load effect, and ripple rejection for the circuit in Problem 3-27.

Section 3-7

3-29 A diode-resistor negative series clipping circuit [as in Fig. 3-25(a)] has a ±12 V input, and zero load current. Determine a suitable resistor value and specify the diode.

3-30 A device is to be protected from the negative half-cycle of a ±8

V square wave input. The device input current is 50 μA when the input is positive. Select a suitable clipping circuit, determine an appropriate resistor, and specify the diode.

3-31 Specify the diodes for the series noise clipper circuit in Fig. 3-27, if R_l = 270 Ω, and the input peaks are ±7 V.

Section 3-8

3-32 A positive shunt clipping circuit [as in Fig. 3-28(a)] with a ±10 V input is to produce a -9 V output when the load current is 500 μA. Determine a suitable resistor value and specify the diode.

3-33 A device is to be protected from the negative half-cycle of a ±6 V square wave input. The device current is 750 μA when its input is +4 V. Select a suitable shunt clipping circuit, determine an appropriate resistor, and specify the diode.

3-34 Specify the diodes for the shunt noise clipper circuit in Fig. 3-30, if R_l = 470 Ω, and the input peaks are ±5 V.

3-35 A ±12 V square wave is applied to a circuit that cannot accept inputs in excess of ±4 V. The circuit input current is ±100 μA. Design a suitable biased shunt clipping circuit.

3-36 Design a Zener diode shunt clipping circuit to satisfy the requirements in Problem 3-35.

3-37 A Zener diode shunt clipping circuit with a ±15 V input is to have a maximum output of ±9 V with an output current of ±750 μA. Design the circuit.

3-38 A biased shunt clipper circuit is to produce a maximum output of ±6 V to a 10 kΩ load. The input voltage peaks can be as high as ±11 V. Design the circuit.

3-39 Design a Zener diode shunt clipping circuit to satisfy the requirements in Problem 3-38.

3-40 Sketch the output waveforms from each of the circuits in Fig. 3-51 when a ±8 V square wave is applied at the input.

Section 3-9

3-41 A positive voltage clamping circuit (as in Fig. 3-34) has C_l = 2 μF and R_l = 27 kΩ. Determine the tilt on the output when a ±5 V, 700 Hz square wave input is applied.

3-42 A negative voltage clamping circuit has a ±9 V, 1 kHz square wave input with a 500 Ω source resistance. The slope on the output waveform is not to exceed 0.5%. Determine suitable resistance and capacitance values.

3-43 A biased clamping circuit (as in Fig. 3-39) has a ±12 V, 330 Hz sine wave input with a 600 Ω source resistance. The positive output peak is to be clamped at 5 V, and the slope between peaks is not to exceed 1%. Determine the required bias voltage and suitable resistance and capacitance values.

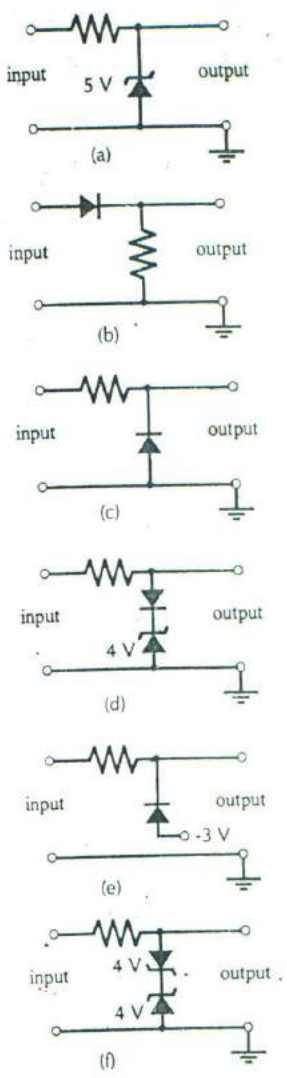


Figure 3-51
Circuits for Problem 3-40.

3-44 Design a Zener diode clamping circuit that will perform as specified in Problem 3-43.

3-45 A Zener diode clamping circuit, as in Fig. 3-41, uses a germanium diode and a *1N746* Zener diode. The input voltage is a ±8 V, 1 kHz square wave. Determine the output voltage levels, and calculate the capacitor voltage.

3-46 Sketch the output waveforms from each of the circuits in Fig. 3-52 when a ±15 V square wave is applied at the input.

3-47 A ±20 V, 700 Hz square wave with a 500 Ω source resistance is to be clamped to a maximum level of approximately 12 V. Design a suitable Zener diode circuit that will produce a maximum output tilt of 3%.

Section 3-10

3-48 A voltage doubling circuit is to be designed to produce an output of 25 V to a 56 kΩ resistor. Determine the required amplitude for a 1 kHz square wave input, and calculate suitable capacitor values if the output ripple is to be a maximum of 0.5 V.

3-49 A voltage doubling circuit with a ±10 V, 2 kHz square wave input has a 33 kΩ load resistance. Determine suitable capacitance values to give a 1% maximum output ripple.

3-50 Refer to the voltage doubling circuit designed for Problem 3-48. Determine the effect of (a) changing R_L to 33 kΩ, (b) changing the input frequency to 1.5 kHz.

Section 3-11

3-51 A three-input diode *AND* gate, as in Fig. 3-49, is to have a minimum diode current of 1 mA. If the circuit supply voltage is 9 V, determine a suitable resistance for R_1.

3-52 A five-input diode *OR* gate used diodes which require a 500 μA minimum forward current. Determine a suitable resistance value if the input voltages are +5 V.

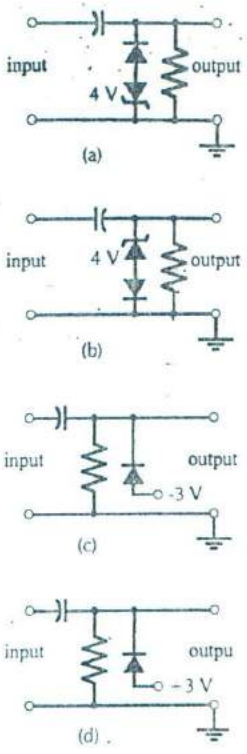


Figure 3-52
Circuits for Problem 3-46.

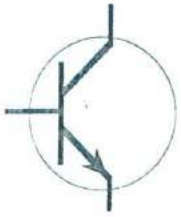
Practise Problem Answers

3-1.1 20.51 V, 62.2 mA, 21.2 V
3-1.2 33.95 V, 48.7 V
3-2.1 32.54 V, 69.2 mA, 1.12 V
3-2.2 238 mW, 13.7 V
3-3.1 1000 μF
3-3.2 835 μF
3-3.3 253.4 V, 600 mA, 8.6 A, 1N4004, 4.2 Ω
3-4.1 500 μF
3-4.2 557 μF
3-4.3 1N4001, 0.57 Ω
3-5.1 50 mV, 100 mV, 0.33%, 0.66%
3-6.1 1N756, 680 Ω, 14.7 mA

3-6.2 1N756, (220Ω + 22 Ω), 43.8 mA
3-6.3 61.4 mV, 336 mV, 3.07×10^{-2}
3-7.1 5.6 kΩ, 7 V, 1 mA
3-7.2 4.7 kΩ, 6 V, 1 mA
3-8.1 330 Ω, 7 V, 19 mA
3-8.2 ±2.8 V, 2.7 kΩ
3-8.3 1N753, 1.8 kΩ
3-9.1 550 mV
3-9.2 1 μF, 100 kΩ
3-9.3 7.5 V, -16.5 V, 4.5 V
3-10.1 1.6%, 0.65%
3-10.2 ±10.7 V, 3.9 μF, 8 μF
3-11.1 680 Ω
3-11.2 1.41 mA, 469 μA

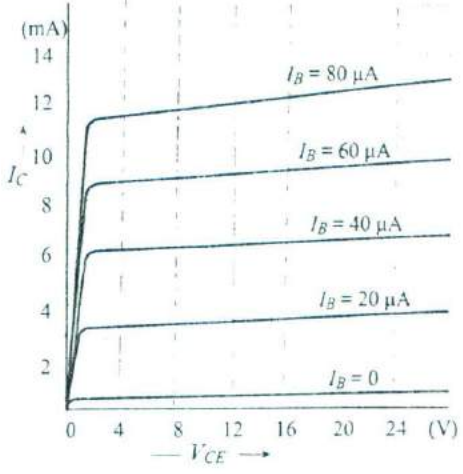
Chapter 4

Bipolar Junction Transistors



Chapter Contents

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Objectives

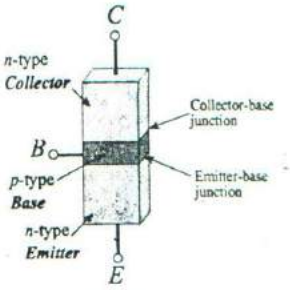
You will be able to:

1. Draw block representations of npn and pnp transistors showing depletion regions and barrier voltages. Explain the operation of each device in terms of junction bias voltages and charge carrier movement.
2. Sketch the circuit symbols for npn and pnp transistors. Identify current directions and junction bias polarities, and state typical terminal voltage levels.
3. Identify and describe the various current components in a transistor. Define α and β. Write equations relating the base, emitter, and collector currents, and calculate transistor current levels.
4. Describe how a transistor can be used for current amplification and voltage amplification. Calculate current and voltage gains.
5. Sketch typical transistor common-base, common-emitter, and common-collector characteristics. Draw circuits to show how each type of characteristic is obtained.
6. Discuss various methods of transistor testing.

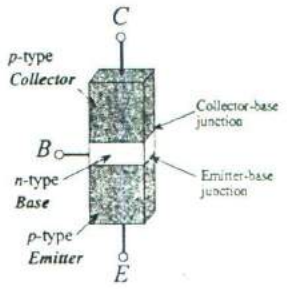
Introduction

A *bipolar junction transistor* (*BJT*) has three layers of semiconductor material. These are arranged either in *npn* (*n*-type—*p*-type—*n*-type) sequence, or in *pnp* sequence, and each of the three layers has a terminal. A small current at the central region terminal controls the much larger total current flow through the device. This means that the transistor can be used for current amplification. As will be explained, it can also perform voltage amplification.

Because the transistor has two *pn*-junctions, its operation can be understood by applying *pn*-junction theory. The currents that flow in a transistor are similar to those that flow across a single *pn*-junction, and the transistor equivalent circuit is essentially two *pn*-junction equivalent circuits. There are three sets of current-voltage characteristics for defining the performance of a transistor.



(a) *npn* transistor



(b) *pnp* transistor

Figure 4-1
Block representation of npn and pnp transistors.

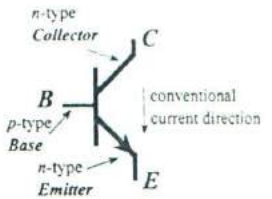
4-1 Transistor Operation

pnp and npn Transistors

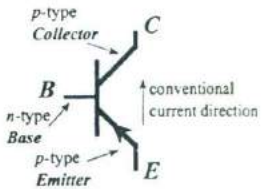
A junction transistor is simply a sandwich of one type of semiconductor material (*p*-type or *n*-type) between two layers of the opposite type. A block representation of a layer of *p*-type material between two layers of *n*-type is shown in Fig. 4-1(a). This is described as an *npn* transistor. Figure 4-1(b) shows a *pnp* transistor, consisting of a layer of *n*-type material between two layers of *p*-type. For reasons which will be understood later, the centre layer is called the *base*, one of the outer layers is termed the *emitter*, and the other outer layer is referred to as the *collector*. The emitter, base, and collector are provided with terminals which are appropriately labelled *E*, *B*, and *C*. Two *pn*-junctions exist within each transistor; the *collector-base junction* and the *emitter-base junction*. Each of these junctions has the characteristics discussed in Chapters 1 and 2.

Circuit symbols for *pnp* and *npn* transistors are shown in Fig. 4-2. The arrowhead on each symbol identifies the transistor emitter terminal, and indicates the conventional direction of current flow. For an *npn* transistor, the arrowhead points from the *p*-type base to the *n*-type emitter. For a *pnp* device, the arrowhead points from the *p*-type emitter to the *n*-type base. Thus, the arrowhead always points from *p* to *n*.

Two transistor packages are illustrated in Fig. 4-3; a low-power transistor, and a high power device. Low-power transistors typically pass currents of 1 mA to 20 mA. Current levels for high-power transistors range from 100 mA to several amps. The high-power transistor is designed for mechanical connection to a heat sink in order to prevent device overheating. Semiconductor device packages are further investigated in Chapter 7.



(a) *npn* transistor



(b) *pnp* transistor

Figure 4-2
Transistor circuit symbols. The arrowhead identifies the emitter terminal, and always points in the conventional current direction.

npn Transistor Operation

Figure 4-4 illustrates the depletion regions and barrier voltages at

the junctions of an unbiased *npn* transistor. These were originally explained in Chapter 1. Although it is not shown in the illustration, the centre layer of the transistor is very much narrower than the two outer layers. Also, the outer layers are much more heavily doped than the centre layer, causing the depletion regions to penetrate deep into the base, as illustrated. Because of this penetration, the distance between the two depletion regions is very short (within the base). Note that the junction barrier voltages are positive on the emitter and collector, and negative on the base of the *npn* device.

Consider Fig. 4-5 which shows an *npn* transistor with external bias voltages. For normal operation, the base-emitter (*BE*) junction is forward biased and the collector-base (*CB*) junction is reverse biased. Note the external bias voltage polarities. The forward bias at the *BE* junction reduces the barrier voltage and causes electrons to flow from the *n*-type emitter to the *p*-type base. The electrons are *emitted* into the base region; hence the name *emitter*. Holes also flow from the *p*-type base to the *n*-type emitter, but because the base is much more lightly doped than the collector, almost all of the current flow across the *BE* junction consists of electrons entering the base from the emitter. Thus, electrons are the *majority charge carriers* in an *npn* device.

The reverse bias at the *CB* junction causes the *CB* depletion region to penetrate deeper into the base than when the junction is unbiased. (see Fig. 4-5). The electrons crossing from the emitter to the base arrive quite close to the large negative-positive electric field (or barrier voltage) at the *CB* depletion region. Because electrons have a negative charge, they are drawn across the *CB* junction by this bias voltage. They are said to be *collected*.

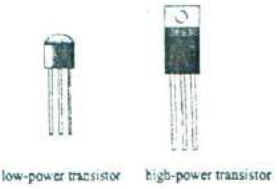


Figure 4-3
Low-power and high-power transistors.

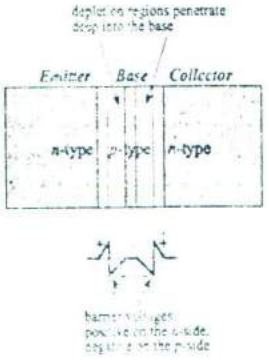


Figure 4-4
Unbiased npn transistor depletion regions and barrier voltages.

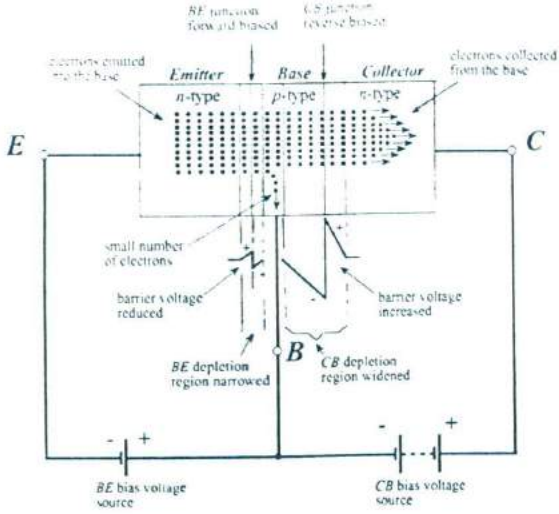


Figure 4-5
For transistor operation, the base-emitter junction is forward biased, and the collector-base junction is reverse biased. Almost all the charge carriers emitted into the base flow to the collector.

Some of the charge carriers entering the base from the emitter do not reach the collector, but flow out via the base connection, as illustrated in Fig. 4-5. However, the path from the *BE* junction to the *CB* depletion region is much shorter than that to the base terminal. So, only a very small percentage of the total charge carriers flow out of the base terminal. Also, because the base region is very lightly doped, there are few holes in the base to recombine with electrons from the emitter. The result is that about 98% of the charge carriers from the emitter are drawn across the *CB* junction to flow via the collector terminal and the voltage sources back to the emitter.

Another way of looking at the effect of the reverse-biased *CB* junction is from the point of view of minority and majority charge carriers. It has already been shown (in Section 1-6) that a reverse-biased junction opposes the flow of majority charge carriers and assists the flow of minority carriers. Majority carriers are, of course, holes from the *p*-side of a junction and electrons from the *n*-side. Minority carriers are holes from the *n*-side and electron from the *p*-side, (see Fig. 4-6). In the case of an *npn* transistor, the charge carriers arriving at the *CB* junction are electrons (from the emitter) travelling through the *p*-type base. Consequently, to the *CB* junction they appear a minority charge carriers, and the reverse bias assists them to cross the junction.

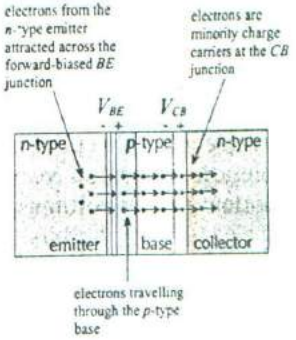


Figure 4-6
Electrons crossing from the emitter into the base become minority charge carriers at the collector-base junction.

Because the *BE* junction is forward biased, it has the characteristics of a forward-biased diode. Substantial current will not flow until the forward bias is about 0.7 V for a silicon device, or about 0.3 V for germanium. Reducing the level of the *BE* bias voltage reduces the *pn*-junction forward bias, and thus reduces the current that flows from the emitter through the base to the collector. Increasing the *BE* bias voltage increases this current. Decreasing the *BE* bias voltage to zero, or reversing it, cuts the current *off* completely. Thus, variation of the small forward-bias voltage on the *BE* junction controls the emitter and collector currents, and the *BE* controlling voltage source has to supply only the small base current. This is illustrated in Fig. 4-7.

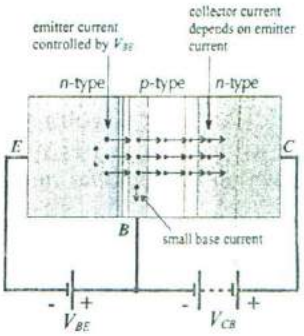


Figure 4-7
The emitter and collector currents are controlled by the base-emitter voltage.

pnp Transistor Operation

In an unbiased *pnp* transistor, the barrier voltages are positive on the base and negative on the emitter and collector, (see Fig. 4-8). As in the case of the *npn* device, the collector and emitter are heavily-doped, so that the *BE* and *CB* depletion regions penetrate deep into the lightly-doped base.

A *pnp* transistor behaves exactly the same as an *npn* device, with the exception that the majority charge carriers are holes. As illustrated in Fig. 4-9, the *BE* junction is forward biased by an external voltage source, and the *CB* junction is reverse biased. Holes are emitted from the *p*-type emitter across the forward-biased *BE* junction into the base. In the lightly doped *n*-type base, the holes find few electrons to absorb. Some of the holes flow out via the base terminal, but most are drawn across to the collector by the positive-negative electric field at the reverse-biased *CB*

junction. Variation of the forward bias voltage at the *BE* junction controls the small base current and the much larger collector and emitter currents.

Bipolar Devices

Although one type of charge carrier is in the majority in a *pnp* or *npn* transistor, two types of charge carrier (holes and electrons) are involved in the current flow. Consequently, these devices are termed *bipolar junction transistors* (*BJT*). This is to distinguish them from *field-effect transistors* (*FET*), (see Chapter 9), which are termed *unipolar* devices, because they use only one type of charge carrier.

Summary

A transistor is a sandwich of *npn* or *pnp* semiconductor materials. The outer layers are called the emitter and the collector, and the centre layer is termed the base. Two *pn*-junctions are formed, with depletion regions and barrier voltages at each junction. The barrier voltages are negative on the *p*-side and positive on the *n*-side.

The base-emitter junction is forward biased, so that charge carriers are emitted into the base. The collector-base junction is reverse biased, and its depletion region penetrates deep into the base. The base section is made as narrow as possible so that charge carriers can easily move across from emitter to collector. The base is also lightly doped, so that few charge carriers are available to recombine with the majority charge carriers from the emitter. Most charge carriers from the emitter flow to the collector; few flow out through the base terminal. Variation of the base-emitter junction bias voltage alters the base, emitter, and collector currents.

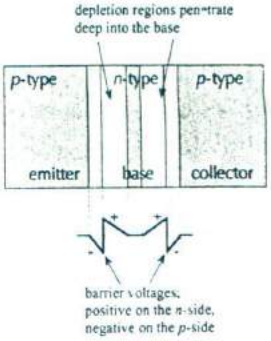


Figure 4-8
Unbiased pnp transistor depletion regions and barrier voltages.

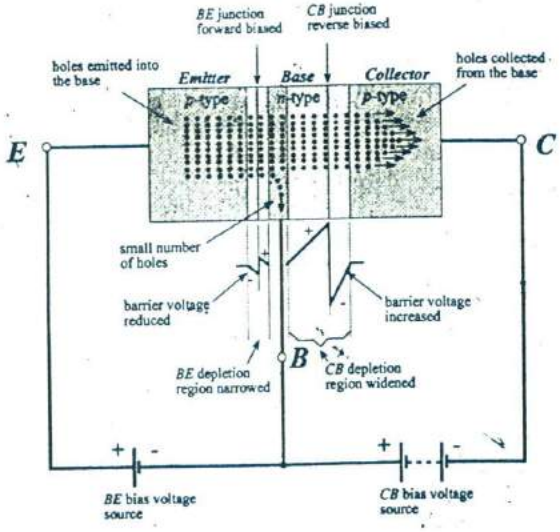


Figure 4-9
In a pnp transistor, the forward-biased base-emitter junction causes charge carriers (holes) to be emitted into the base. Most of these flow across the reverse-biased collector-base junction.

Section 4-1 Review

4-1.1 Sketch a block diagram of a biased *npn* transistor. Show the depletion regions, barrier voltages, and the movement of charge carriers across the junctions. Explain the device operation.

4-1.2 Repeat Question 4-1.1 for a *pnp* transistor.

4-2 Transistor Voltages and Currents

Terminal Voltages

The terminal voltage polarities for an *npn* transistor are shown in Fig. 4-10(a). As well as conventional current direction, the direction of the arrowhead indicates the transistor bias polarities. For an *npn* transistor, the base is biased positive with respect to the emitter, and the arrowhead points from the (positive) base to the (negative) emitter. The collector is then biased to a higher positive voltage than the base.

Figure 4-10(b) shows that the voltage sources are usually connected to the transistor via resistors. The base bias voltage (V_B) is connected via resistor R_B, and the collector supply (V_{CC}) is connected via R_C. The negative terminals of the two voltage sources are connected at the transistor emitter terminal. V_{CC} is always much larger than V_B, and this ensures that the *CB* junction remains reverse biased; positive on the collector (*n*-side), and negative on the base (*p*-side).

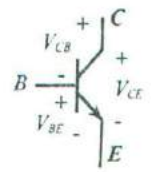
Typical transistor base-emitter voltages are similar to diode forward voltages; 0.7 V for a silicon transistor, and 0.3 V for a germanium device. Typical collector voltages might be anything from 3 V to 20 V for most types of transistors, although in many the collector voltage may be greater than 20 V.

For a *pnp* device [Fig. 4-11(a)] the base is biased negative with respect to the emitter. The arrowhead points from the (positive) emitter to the (negative) base, and the collector is made more negative than the base. Figure 4-11(b) shows the voltage sources connected via resistors, and the source positive terminals connected at the emitter. With V_{CC} larger than V_B, the (*p*-type) collector is more negative than the (*n*-type) base, keeping the *CB* junction reverse biased.

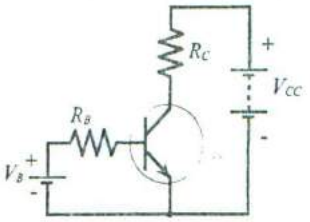
All transistors (*npn* and *pnp*) are normally operated with the *CB* junction reverse biased and the *BE* junction forward biased. In the case of a switching transistor, (a transistor that is not operated as an amplifier, but is either switched *on* or *off*), the *CB* junction may become forward biased by approximately 0.5 V. Also, in transistor switching circuits (and some other circuits) the *BE* junction can become reverse biased.

Transistor Currents

The various current components that flow within a transistor are illustrated in Fig. 4-12. The current flowing into the emitter terminal is referred to as the *emitter current* and is identified as I_E. For the *pnp* device shown, I_E can be thought of as a flow of holes

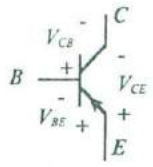


(a) *npn* terminal voltage polarities

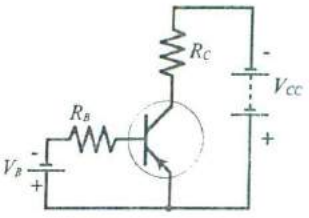


(b) Voltage source connections

Figure 4-10
An npn transistor must have its base biased positive with respect to its emitter, and its collector more positive than the base.



(a) *pnp* terminal voltage polarities



(b) Voltage source connections

Figure 4-11
An pnp transistor must have its base biased negative with respect to its emitter, and its collector more negative than the base.

from the emitter to the base. Note that the indicated I_E direction is the conventional current direction from positive to negative. *Base current* I_B and *collector current* I_C are also shown as conventional current direction. Both I_C, and I_B flow *out* of the transistor, while I_E flows *into* the transistor, (see Fig. 4-12 and 4-13). Therefore,

$$I_E = I_C + I_B \tag{4-1}$$

As already discussed, almost all of I_E crosses to the collector, and only a small portion flows out of the base terminal. Typically 96% to 99.5% of I_E flows across the collector-base junction to become the collector current. As shown in Fig. 4-12,

$$I_C = \alpha_{dc} I_E \tag{4-2}$$

α_{dc} (*alpha dc*) is the *emitter-to-collector current gain*, or the ratio of collector current to emitter current. From Eq. 4-2, $\alpha_{dc} = I_C/I_E$. Numerically, α_{dc} is typically 0.96 to 0.995. So, the collector current is almost equal to the emitter current, and in many circuit situations I_C is assumed equal to I_E. For reasons that will be explained later, α_{dc} is termed *the common-base dc current gain.*

Because the *CB* junction is reverse biased, a very small *reverse saturation current* (I_{CBO}) flows across the junction. (see Fig. 4-12). I_{CBO} is named the *collector-to-base leakage current*, and it is normally so small that it can be neglected.

Substituting for I_E from Eq. 4-1 into Eq. 4-2,

$$I_C = \alpha_{dc} (I_C + I_B) \tag{4-3}$$

which gives,
$$I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} \tag{4-4}$$

Equation 4-4 can be rewritten as,

$$I_C = \beta_{dc} I_B \tag{4-5}$$

where,
$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \tag{4-6}$$

β_{dc} (*beta dc*) is the *base-to-collector current gain*, or the ratio of collector current to base current, (see Fig. 4-13). From Eq. 4-5, $\beta_{dc} = I_C/I_B$. Typically, β_{dc} ranges from 25 to 300. As will be explained, β_{dc} is also termed the *common-emitter dc current gain.* Instead of β_{dc}, another symbol for common-emitter *dc* current gain is h_{FE}. This originates from the *h-parameter* circuit discussed in Section 6-3. h_{FE} *is the symbol used on transistor data sheets.*

Although Equations 4-1 through 4-6 were derived for a *pnp* device, they apply equally to *npn* transistors. One difference in the case of an *npn* transistor is that I_B and I_C are assumed to flow *into* the device (conventional current direction), and I_E is taken as flowing *out*, (see Fig. 4-14). As explained in Section 4-1, electrons are the majority charge carriers in an *npn* transistor, and they move in a direction opposite to conventional current direction.

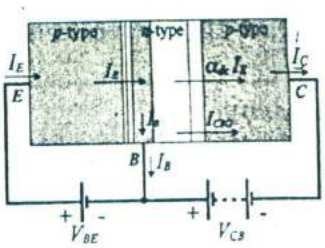


Figure 4-12
Currents in a pnp transistor. I_C approximately equals I_E and I_B is very much smaller than I_E.

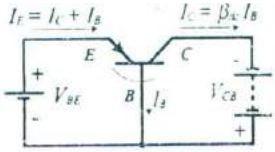


Figure 4-13
Currents in a pnp transistor. I_E is the sum of I_C and I_B. $I_C = \beta_{dc} I_B$, where β_{dc} is typically 25 to 300.



Figure 4-14
Currents in an npn transistor. I_E is the sum of I_C and I_B. $I_C = \beta_{dc} I_B$.

Typical collector and emitter currents for low-power transistors range from 1 mA to 25 mA, and base currents are usually less than 100 μA. High power transistors handle currents of several amps.

Example 4-1

Calculate I_C and I_E for a transistor that has $\alpha_{dc} = 0.98$ and $I_B = 100\mu A$. Also, determine the value of β_{dc} for the transistor.

Solution

Eq. 4-4, $$I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} = \frac{0.98 \times 100\,\mu A}{1 - 0.98}$$

$$= 4.9 \text{ mA}$$

from Eq. 4-2, $$I_E = \frac{I_C}{\alpha_{dc}} = \frac{4.9 \text{ mA}}{0.98}$$

$$= 5 \text{ mA}$$

Eq. 4-6, $$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98}$$

$$= 49$$

Example 4-2

Calculate α_{dc} and β_{dc} for the transistor in Fig. 4-15 if I_C is measured as 1 mA, and I_B is 25 μA. Also, determine the new base current to give $I_C = 5$ mA.

Solution

Eq. 4-5, $$\beta_{dc} = \frac{I_C}{I_B} = \frac{1 \text{ mA}}{25\,\mu A}$$

$$= 40$$

Eq. 4-1, $$I_E = I_C + I_B = 1 \text{ mA} + 25\,\mu A$$

$$= 1.025\,\mu A$$

from Eq. 4-2, $$\alpha_{dc} = \frac{I_C}{I_E} = \frac{1 \text{ mA}}{1.025 \text{ mA}}$$

$$= 0.976$$

Eq. 4-5, $$I_B = \frac{I_C}{\beta_{dc}} = \frac{5 \text{ mA}}{40}$$

$$= 125\,\mu A$$

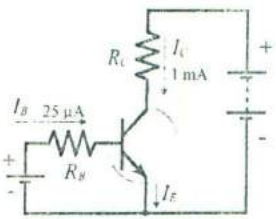


Figure 4-15
Circuit for Example 4-2.

Practise Problems

4-2.1 Determine α_{dc} and I_B for a transistor that has $I_C = 2.5$ mA and $I_E = 2.55$ mA. Also, calculate β_{dc} for the transistor.

4-2.2 A transistor has measured currents of $I_C = 3$ mA and $I_E = 3.03$ mA. Calculate the new current levels when the transistor is replaced with a device that has $\beta_{dc} = 75$. Assume that I_B remains constant.

4-3 Amplification

Current Amplification

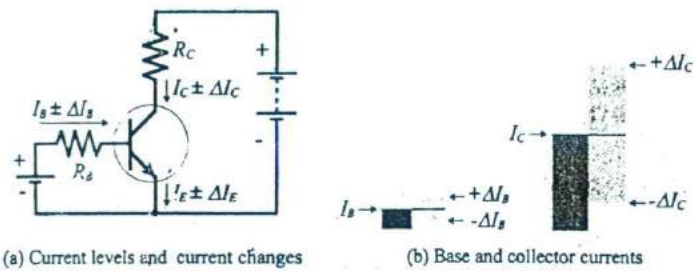
The equations derived in Section 4-2 demonstrate that a transistor can be used for current amplification. A small change in the base current (ΔI_B) produces a large change in collector current (ΔI_C) and a large emitter current change (ΔI_E). [see Fig. 4-16(a) and (b)]. Rewriting Eq. 4-5, the current gain from the base to collector can be stated in terms of current level changes.

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

The increasing and decreasing levels of input and output currents may be defined as alternating quantities. In this case, small (lower-case) letters are used for the subscripts. Thus, I_b is an *ac* base current, I_c is an *ac* collector current, and I_e is an *ac* emitter current. The alternating current gain from base to collector may now be stated as,

$$\beta_{ac} = \frac{I_c}{I_b} \qquad \textbf{(4-7)}$$

As in the case of *dc* current gain, two parameter symbols are available for common-emitter *ac* current gain: β_{ac} and h_{fe}. Either symbol may be used, but, once again, h_{fe} *is the symbol employed on transistor data sheets.*



(a) Current levels and current changes (b) Base and collector currents

Figure 4-16
Increasing and decreasing I_B levels produces much larger changes in I_C and I_E.

Voltage Amplification

Refer to the circuit in Fig. 4-17(a), and assume that the transistor (Q_1) has $\beta_{dc} = 50$. Note that the 0.7 V *dc* voltage source (V_B) forward biases the transistor base-emitter junction. An *ac* signal source (v_i) in series with V_B provides a ±20 mV input voltage. The transistor collector is connected to a 20 V *dc* voltage source (V_{CC}) via the 12 kΩ collector resistor (R_1).

If Q_1 has the I_B/V_{BE} characteristic shown in Fig. 4-17(b), the 0.7 V level of V_B produces a 20 μA base current. This gives,

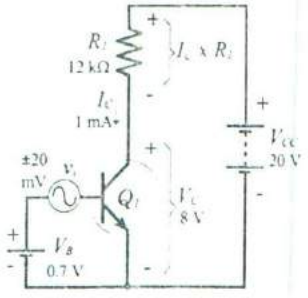
$$I_C = \beta_{dc} I_B = 50 \times 20\ \mu A$$
$$= 1\ mA$$

The *dc* level of the transistor collector voltage can now be

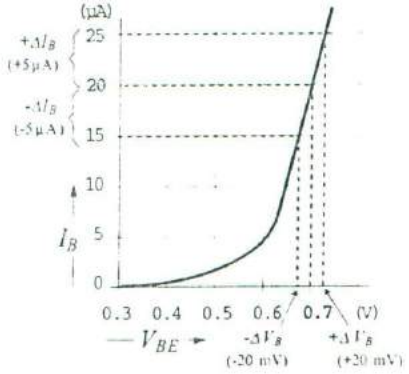
calculated as,

$$V_C = V_{CC} - (I_C R_l) = 20\text{ V} - (1\text{ mA} \times 12\text{ k}\Omega)$$
$$= 8\text{ V}$$

The V_C and I_C levels are shown on Fig. 4-17(a).



(a) Transistor circuit with base bias and signal generator



(b) V_{BE} changes produce I_B changes

Figure 4-17
Increasing and decreasing V_B levels ($\pm\Delta V_B$) produces I_B changes ($\pm\Delta I_B$). This results in I_C changes and (output) collector voltage variations.

While the *ac* input voltage (v_i) is zero, the transistor collector voltage remains at 8 V. When v_i causes a base voltage variation (ΔV_B) of ±20 mV, the base current changes by ±5 μA, as shown in Fig. 4-17(b). The I_B change produces a collector current change.

$$\Delta I_C = \beta_{dc}\,\Delta I_B = 50 \times (\pm 5\ \mu\text{A})$$
$$= \pm 250\ \mu\text{A}$$

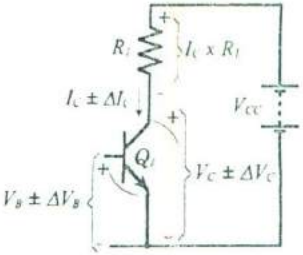
Figure 4-18(a) shows that ΔI_C causes a change in the voltage drop across R_l, and thus produces a variation in the transistor collector voltage.

$$\Delta V_C = \Delta I_C R_l = \pm 250\ \mu\text{A} \times 12\ \text{k}\Omega$$
$$= \pm 3\text{ V}$$

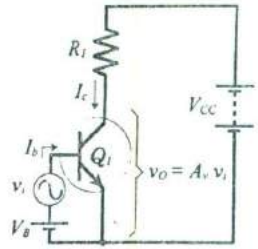
The circuit *ac* input is the base voltage change (ΔV_B), and the *ac* output is the collector voltage change (ΔV_C). Because the output is greater than the input, the circuit has a voltage gain; it is a *voltage amplifier*. The *voltage gain* (A_v) is the ratio of the output voltage to the input voltage.

$$A_v = \frac{\Delta V_C}{\Delta V_B} = \frac{\pm 3\text{ V}}{\pm 20\text{ mV}}$$
$$= 150$$

As already discussed for current changes, the increasing and decreasing levels of voltage can be referred to as *ac* quantities. The *ac* signal voltage (v_i) produces the *ac* base current (I_b), and this generates the *ac* collector current (I_c) which produces the *ac* voltage change across R_l. [see Fig. 4-18(b)]. The equation for *ac* voltage gain is,



(a) ΔI_C changes V_{Rl} and V_C



(b) An *ac* input (v_i) produces an *ac* output (v_o)

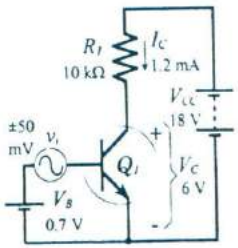
Figure 4-18
I_C changes produce changes in V_C. An ac input (v_i) produces an ac output ($v_o = A_v v_i$).

$$A_v = \frac{v_o}{v_i} \qquad (4\text{-}8)$$

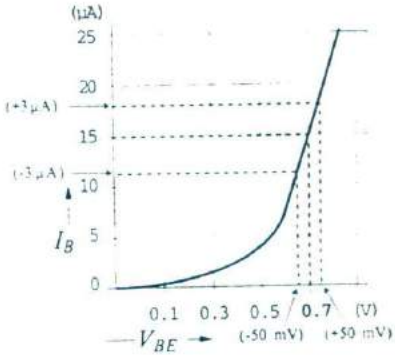
Substituting the *ac* quantities for Fig. 4-17(a) into Eq. 4-8 gives $A_v = 150$ once again.

Example 4-3

Determine the *dc* collector voltage for the circuit in Fig. 4-19(a), if the transistor has the I_B/V_{BE} characteristics shown in Fig. 4-19(b), and $\beta_{dc} = \beta_{ac} = 80$. Also, calculate the circuit voltage gain when v_i is ±50 mV.



(a) Transistor circuit



(b) V_{BE} I_B characteristic for Q_1.

Figure 4-19
Circuit and characteristics for Example 4-3.

Solution

From Fig. 4-19(b), $I_B = 15\ \mu A$ for $V_B = 0.7$ V

$$I_C = \beta_{dc} I_B = 80 \times 15\ \mu A = 1.2\ mA$$

$$V_C = V_{CC} - (I_C R_1) = 18\ V - (1.2\ mA \times 10\ k\Omega) = 6\ V$$

From Fig. 4-18(b), $I_b = \pm 3\ \mu A$ for $v_i = \pm 50$ mV

$$I_c = \beta_{ac} I_b = 80 \times \pm 3\ \mu A = \pm 240\ \mu A$$

$$v_o = I_c R_1 = \pm 240\ \mu A \times 10\ k\Omega = \pm 2.4\ V$$

Eq. 4-9, $$A_v = \frac{V_o}{v_i} = \frac{\pm 2.4\ V}{\pm 50\ mV} = 48$$

Practise Problems

4-3.1 A circuit similar to Fig. 4-17 has $V_{CC} = 15$ V, $R_1 = 5.6$ kΩ, $V_C = 7$ V, and $I_B = 20\ \mu A$. Calculate the *dc* current gain.

4-3.2 A ±50 mV ac input is applied in series with the transistor base in Problem 4-3.1. Assuming that the transistor has the input characteristics in Fig. 4-17(b), calculate the circuit ac voltage gain.

4-4 Common-Base Characteristics

Common-Base Connection

To investigate the characteristics of a diode (a two-terminal device), several levels of forward or reverse bias voltage are applied and the resulting current levels are measured. The characteristics of the device are then derived by plotting the graph of current versus

voltage. Because a transistor is a three-terminal device, there are three possible connection arrangements (*configurations*) for investigating its characteristics. From each of these configurations, three sets of characteristics may be derived.

Figure 4-20 shows a *pnp* transistor with its base terminal common to both the input (*EB*) voltage and the output (*CB*) voltage. The transistor is said to be connected in *common-base* configuration. Voltmeters and ammeters are included to measure the input and output voltages and currents.

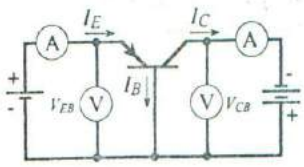


Figure 4-20
Circuit for determining transistor common-base characteristics.

Input Characteristics

To determine the *input characteristics*, the output (*CB*) voltage is maintained constant, and the input (*EB*) voltage is set at several convenient levels. For each level of input voltage, the input current I_E is recorded. I_E is then plotted versus V_{EB} to give the common-base input characteristics shown in Fig. 4-21.

Because the *EB* junction is forward biased, the common-base input characteristics are essentially those of a forward biased *pn*-junction. Figure 4-21 also shows that for a given level of input voltage, more input current flows when higher levels of *CB* voltage are used. This is because larger *CB* (reverse bias) voltages cause the depletion region at the *CB* junction to penetrate deeper into the base of the transistor, thus shortening the distance and reducing the resistance between the *EB* and *CB* depletion regions.

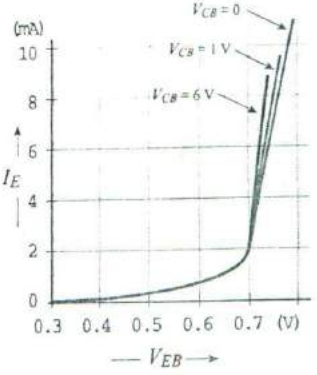


Figure 4-21
The common-base input characteristics for a transistor are the characteristics of a forward-biased pn-junction.

Output Characteristics

The emitter current I_E is held constant at each of several fixed levels. For each fixed level of I_E, the output voltage V_{CB} is adjusted in convenient steps, and the corresponding levels of collector current I_C are recorded. In this way, a table of values is obtained from which a family of output characteristics may be plotted. In Fig. 4-22 the corresponding I_C and V_{CB} levels obtained when I_E was held constant at 1 mA are plotted, and the resultant characteristic is identified as I_E = 1 mA. Similarly, other characteristics are plotted for I_E levels of 2 mA, 3 mA, 4 mA, and 5 mA.

The common-base output characteristics in Fig. 4-22 show that for each fixed level of I_E, I_C is almost equal to I_E and appears to remain constant when V_{CB} is increased. In fact, there is a very small increase in I_C with increasing V_{CB}. This is because the increase in collector-to-base bias voltage (V_{CB}) expands the *CB* depletion region, and thus shortens the distance between the two depletion regions. With I_E held constant, the increase in I_C is so small that it is noticeable only for large variations in V_{CB}.

As illustrated in Fig. 4-22, when V_{CB} is reduced to zero, I_C still flows. Even when the externally applied bias voltage is zero, there is still a barrier voltage existing at the *CB* junction, and this assists the flow of I_C. The charge carriers which constitute I_C are minority carriers as they cross the *CB* junction. Thus, the reverse-bias voltage V_{CB} and the (unbiased) *CB* barrier voltage assist their movement across the junction, (see Fig. 4-12). To stop the flow of charge carriers, the *CB* junction has to be forward biased.

Consequently, as shown in Fig. 4-22, I_C is reduced to zero only when V_{CB} is increased positively.

The region of the graph for the forward-biased *CB* junction is known as the *saturation region*, (see Fig. 4-22). The region in which the junction is reverse biased is named the *active region*, and this is the normal operating region for the transistor.

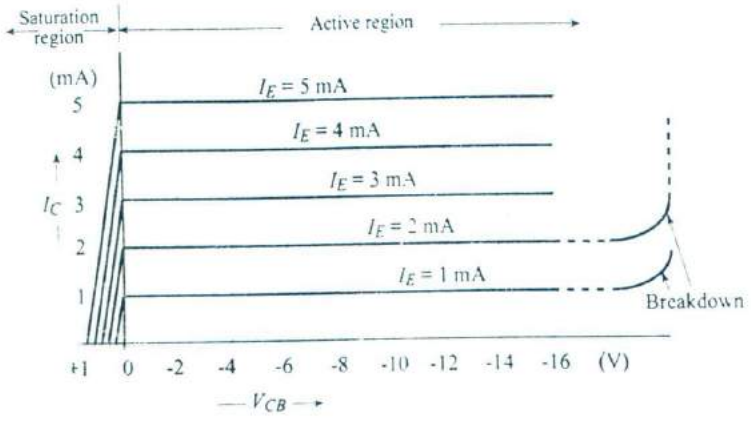


Figure 4-22
The common-base output characteristics (or collector characteristics) for a transistor show that I_C remains substantially constant for each level of I_E.

If the reverse-bias voltage on the *CB* junction is allowed to exceed the maximum safe limit specified by the manufacturer, device breakdown may occur. Breakdown, illustrated by the dashed lines in Fig. 4-22, can be caused by the same effects that make diodes breakdown. (see Section 2-9). Breakdown can also result from the *CB* depletion region penetrating into the base until it makes contact with the *EB* depletion region, (Fig. 4-23). This condition is known as *punch-through*, or *reach-through*, and very large currents can flow when it occurs, possibly destroying the device. The extension of the depletion region is produced by the increase in V_{CB}. So, it is very important to maintain V_{CB} below the maximum safe limit specified by the device manufacturer. Typical maximum V_{CB} levels range from 25 V to 80 V.

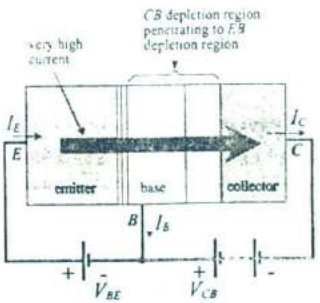


Figure 4-23
Excessive levels of V_{CB} can cause the depletion regions to make contact, resulting in destructive current levels.

Current Gain Characteristics

The *current gain characteristics* (also termed the *forward transfer characteristics*) are a graph of output current (I_C) versus input current (I_E). They are obtained experimentally by use of the circuit in Fig. 4-20. V_{CB} is held constant at a convenient level, and I_C is measured for various levels of I_E. I_C is then plotted versus I_E, and the resultant graph is identified by the V_{CB} level, (see Fig. 4-24).

The *CB* current gain characteristics can be derived from the *CB* output characteristics, as shown in Fig. 4-25. A vertical line is drawn through a selected V_{CB} value, and corresponding levels of I_E and I_C are read along the line. The I_C levels are then plotted versus I_E, and the characteristic is labelled with the V_{CB} used. Because almost all of I_E flows out of the collector terminal as I_C, V_{CB} has only a small effect on the current gain characteristics.

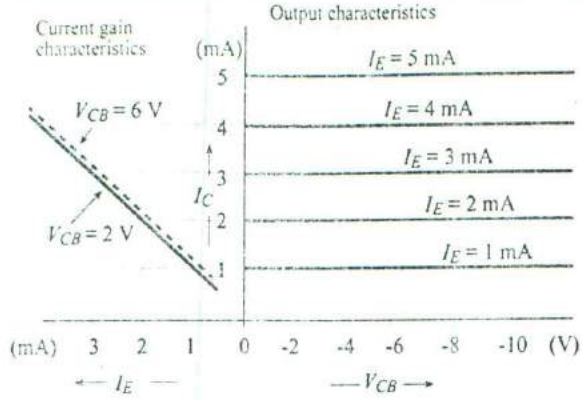


Figure 4-24
The common-base current gain characteristics for a transistor are graphs of output current I_C versus input current I_E.

Example 4-4

Derive the current gain characteristic for V_{CB} = 2 V from the common-base output characteristics in Fig. 4-25.

Solution

Draw a vertical line at V_{CB} = 2 V.
Where the line intersects the characteristics at points A and B, read:

$$I_C \approx 1 \text{ mA for } I_E = 1 \text{ mA}$$

and,

$$I_C \approx 4 \text{ mA for } I_E = 4 \text{ mA}$$

Plot points C and D for the output characteristic at the corresponding levels of I_C and I_E.

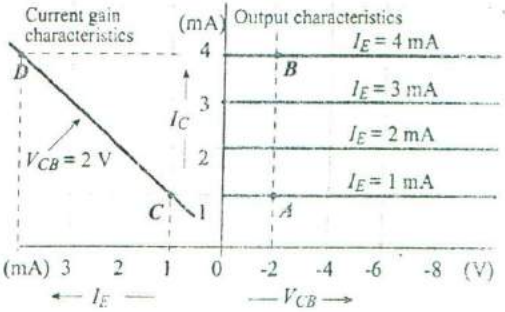


Figure 4-25
Derivation of common-base current gain characteristics from the output characteristics.

Practice Problems

4-4.1 Plot two lines of common-base output characteristics from the following measured quantities:
for I_E = 1.5 mA: (I_C = 1.40 mA when V_{CB} = 0 V)
(I_C = 1.45 mA when V_{CB} = 10 V)
for I_E = 3 mA: (I_C = 2.80 mA when V_{CB} = 0 V)
(I_C = 2.95 mA when V_{CB} = 10 V)
Derive the current gain characteristics for V_{CB} = 5 V from the transistor output characteristics

4-5 Common-Emitter Characteristics

Common-Emitter Circuit

Figure 4-26 shows a circuit for determining transistor *common-emitter* characteristics. The input voltage is applied between the *B* and *E* terminals, and the output is taken at the *C* and *E* terminals. The emitter terminal is common to both input and output. Voltage and current levels are measured as shown.

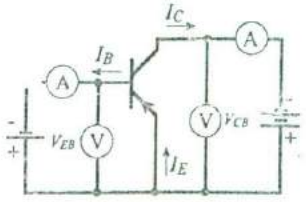


Figure 4-26
Circuit for determining transistor common emitter characteristics.

Input Characteristics

To prepare a table of values for constructing the *common-emitter input characteristics*, V_{CE} is held constant, V_{BE} is set at convenient levels, and the corresponding I_B levels are recorded. I_B is then plotted versus V_{BE}, as shown in Fig. 4-27. It is seen that the common-emitter input characteristics (like the common-base input characteristics) are those of a forward-biased *pn*-junction. It should be remembered that I_B is only a small portion of the total current (I_E) that flows across the forward-biased *BE* junction.

Figure 4-27 also shows that, for a given level of V_{BE}, I_B is reduced when higher V_{CE} levels are employed. This is because higher V_{CE} produces greater depletion region penetration into the base, reducing the distance between the *CB* and *EB* depletion regions. Consequently, more of the charge carriers from the emitter flow across the *CB* junction, and fewer flow out via the base terminal.

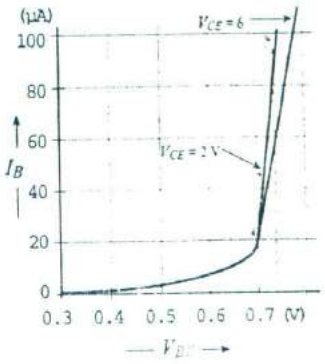


Figure 4-27
The common-emitter input characteristics for a transistor are those of a forward-biased pn-junction.

Output Characteristics

To prepare a table of values for plotting the *common-emitter output characteristics*, I_B is maintained constant at several convenient levels. V_{CE} is adjusted in steps at each I_B level, and the I_C level is recorded at each V_{CE} step. For each I_B level, I_C is plotted versus V_{CE} to give a family of characteristics, as shown in Fig. 4-28.

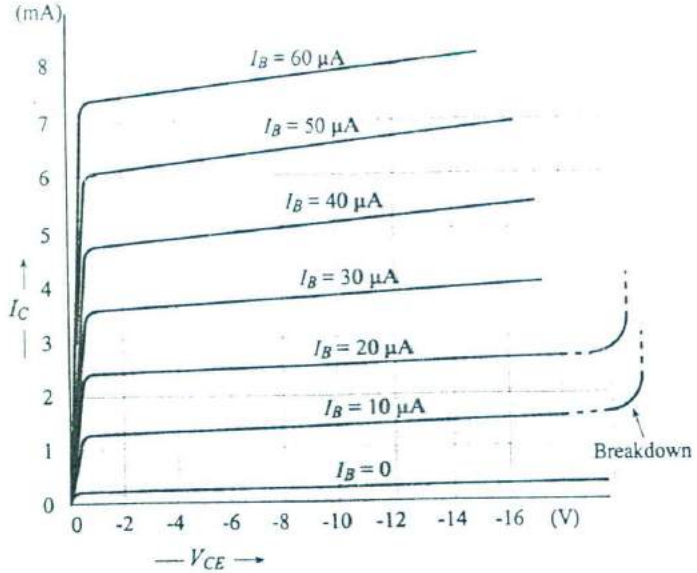
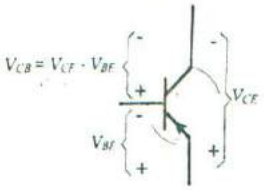


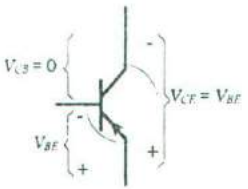
Figure 4-28
The common-emitter output characteristics (or collector characteristics) for a transistor are a plot of I_C versus V_{CE} for various I_B levels.

Because I_E is not held constant (as it is for the common-base output characteristics) the shortening of the distance between the depletion regions (when V_{CB} is increased) draws more charge carriers from the emitter to the collector. Thus, I_C increases to some extent with increasing V_{CE} although I_B is held constant. So, the slopes of the common-emitter output characteristics are much more pronounced than those of the common-base characteristics.

On Fig. 4-28 note that I_C reduces to zero when V_{CE} becomes zero. This is because the horizontal axis voltage is V_{CE}, which equals (V_{CB} + V_{BE}). (see Fig. 4-29). At the *knee* of the characteristic, the *CB* junction voltage (V_{CB}) has been reduced to zero, (because V_{CE} = V_{BE}). Further reduction in V_{CE} causes the *CB* junction to be forward biased. The forward bias repels the minority charge carriers, thus reducing I_C to zero. The dashed lines in Fig. 4-28 show that, if V_{CE} exceeds a maximum safe level, I_C increases rapidly and the device may be destroyed. As for common-base configuration, this is due to *punch-through*.



(a) $V_{CB} = V_{CE} - V_{BE}$



(b) $V_{CB} = 0$ when $V_{CE} = V_{BE}$

Figure 4-29
In a common-emitter circuit, V_{CB} can be reduced to zero, and can be reversed, when V_{CE} is reduced.

Example 4-5

Determine the I_B and I_C levels for a device with the characteristics in Figs. 4-27 and 4-28, when V_{BE} is 0.7 V and V_{CE} is 6 V. Also, calculate the β_{dc} value.

Solution

From Fig. 4-27, at (V_{BE} = 0.7 V and V_{CE} = 6 V): $I_B \approx 20\,\mu A$

From Fig. 4-28, at (V_{CE} = 6 V and I_B = 20 μA): $I_C = 2.5$ mA

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.5\text{ mA}}{20\,\mu\text{A}}$$

$$= 125$$

Current Gain Characteristics

The *common-emitter current gain characteristics* are (output current) I_C plotted versus (input current) I_B for various fixed levels of V_{CE}. Like the common-base current gain characteristics, they can be obtained experimentally, or derived from the output characteristics. To experimentally obtain the table of I_C and I_B values, V_{CE} is held at a selected level, and the base current I_B is adjusted in steps. The corresponding I_C level is recorded at each step of I_B.

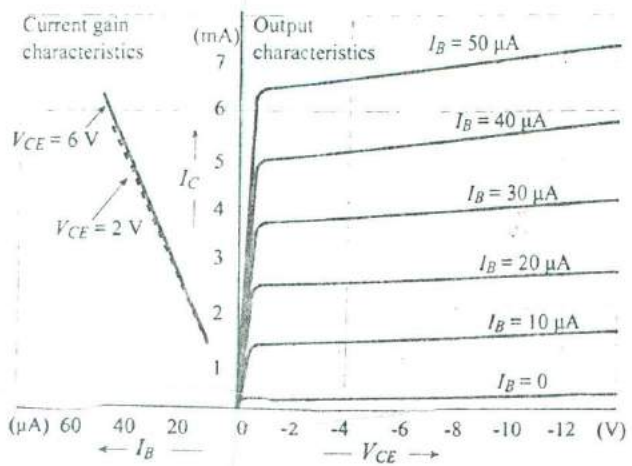


Figure 4-30
The common-emitter current-gain characteristics for a transistor are a plot of I_C versus I_B.

Practise Problems

4-5.1 Plot two lines of common-emitter transistor output characteristics from the following quantities:
for $I_B = 25\ \mu A$: ($I_C = 1.5$ mA when $V_{CE} = 1$ V)
($I_C = 1.75$ mA when $V_{CE} = 12$ V)
for $I_B = 50\ \mu A$: ($I_C = 3$ mA when $V_{CE} = 1$ V)
($I_C = 3.5$ mA when $V_{CE} = 12$ V)
Derive the current gain characteristics for $V_{CE} = 12$ V from the device output characteristics.

4-6 Common-Collector Characteristics

In the circuit arrangement of Fig. 4-31, the collector terminal is common to both input *CB* voltage and output *CE* voltage. Using this circuit, the *common-collector input, output,* and *current gain characteristics* can be determined. The output and current gain characteristics are shown in Fig. 4-32. The common-collector output characteristics are I_E plotted versus V_{CE} for several fixed values of I_B. The common-collector current gain characteristics are I_E plotted versus I_B for several fixed values of V_{CE}.

It will be recalled that the common-emitter output characteristics are I_E plotted against V_{CE}, and that the common-emitter current gain characteristics are I_E plotted against I_B. Because I_C is approximately equal to I_E, the common-collector output and current gain characteristics are practically identical to those of the common-emitter circuit.

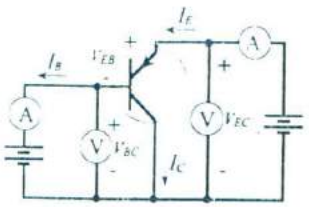


Figure 4-31
Transistor circuit used for determining common-collector characteristics.

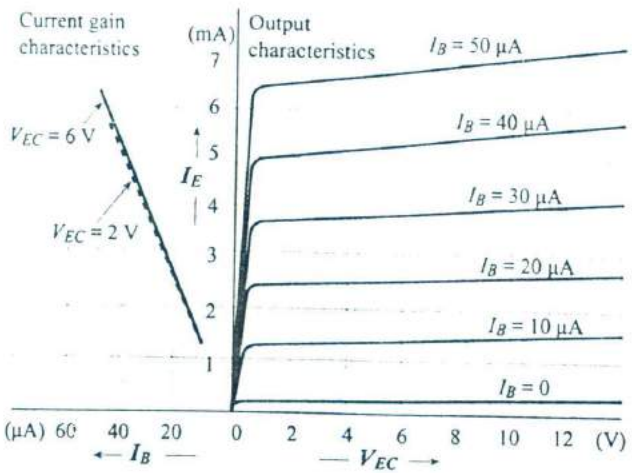


Figure 4-32
The common-collector output and current-gain characteristics are identical to the common-emitter characteristics.

The common-collector input characteristics shown in Fig. 4-33 are quite different from either common-base or common-emitter input characteristics. The difference is due to the fact that the input voltage (V_{BC}) is largely determined by the V_{EC} level.

Referring to Fig. 4-31,

$$V_{EC} = V_{EB} + V_{BC}$$

or,

$$V_{EB} = V_{EC} - V_{BC}$$

Increasing the level of (input voltage) V_{BC} with V_{EC} held constant, reduces the level of V_{EB}, and thus reduces I_B.

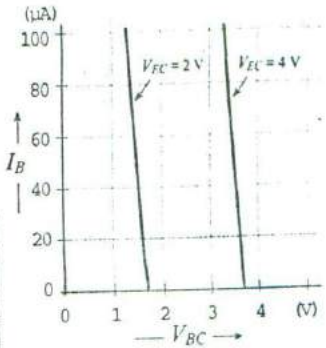


Figure 4-33
The common-collector input characteristics are quite different from input characteristics for common-base and common-emitter connections.

Practise Problems

4-6.1 Referring to the common-collector input characteristics in Fig. 4-33, determine the level of V_{BC} when $I_B = 60\ \mu A$ and $V_{EC} = 2$ V, also when $I_B = 60\ \mu A$ and $V_{EC} = 4$ V.

4-7 Transistor Testing

In-Circuit Testing

A quick test to check if a transistor is operational can be performed while the device is still connected in a circuit. Consider Fig. 4-34, which shows a voltmeter connected to measure the transistor collector voltage (V_C). The V_C measurement is noted, then the base and emitter terminals are temporarily short-circuited, as illustrated. This should turn the transistor *off*, and V_C should jump to approximately the circuit supply voltage (V_{CC}). When the shorting wire is removed, V_C should return to its previous level. If the change in the V_C level does not occur, the transistor is not operational. This may be due to a faulty transistor, or to some other problem in the circuit.

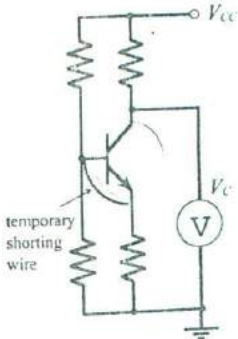


Figure 4-34
Short-circuiting the base and emitter terminals should cause V_C to jump to V_{CC} if the transistor is operating.

Ohmmeter Tests

An ohmmeter may be used for checking the transistor emitter-base and collector-base junctions. As in the case of a diode, the measured resistance of a forward-biased junction depends upon the ohmmeter range. With an analog ohmmeter, a good forward-biased *pn*-junction typically indicates half-scale, (see Fig. 4-35). A good reverse-biased junction gives a very high resistance measurement. Recall from Section 2-8 that the terminal polarity of some multimeters is reversed when used as an ohmmeter. This should be checked with a voltmeter. The measured resistance between the collector and emitter terminals of a good transistor should be very high regardless of the ohmmeter terminal polarity.

A digital ohmmeter may show a resistance of a few megohms when measuring a good forward-biased junction, and an open-circuit indication (*OL*) for a reverse-biased junction, (Fig. 4-36). It should also indicate open-circuit when measuring between the collector and emitter terminals. The diode testing terminals on a digital multimeter may also be used for testing transistor *CB* and *EB* junctions. Some digital multifunction instruments have testing facilities for measuring transistor h_{FE} values.

Characteristic Plotting

A transistor may be rapidly checked by use of a *curve tracer*, (see Fig. 4-37). Two transistor sockets are normally provided to display the characteristics of two devices. A switch permits selection of either socket. The characteristics of a known good transistor should first be displayed. Then, the switch should be operated to display the characteristics of the transistor under investigation.

Transistor characteristics may be plotted by obtaining a table of corresponding levels of current and voltage, as already discussed. A more convenient method of plotting characteristics using an *XY recorder* is illustrated in Fig. 4-38. One power supply is connected to produce base current (I_B) via resistor R_1, and the other provides I_C flow through R_2. The collector and emitter terminals are connected to the horizontal input terminals of the *XY* recorder, and the voltage drop across resistor R_2 provides the vertical input. The base current is set at a several convenient levels, and (at each I_B level) V_{CC} is slowly increased from zero to cause the pen to trace one line of the transistor output characteristics.

A convenient selection for the horizontal and vertical scales of the *XY* recorder is 1 V/cm. If R_2 = 1 kΩ, each 1 V drop across R_2 represents 1 mA of collector current. So, the I_C (vertical) scale on the characteristics is 1 mA/cm, and the V_{CE} scale is 1 V/cm.

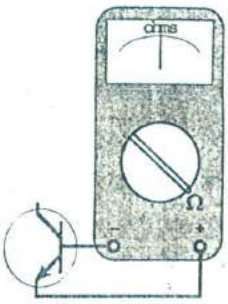


Figure 4-35
Use of an analog ohmmeter for checking the junctions of a transistor.

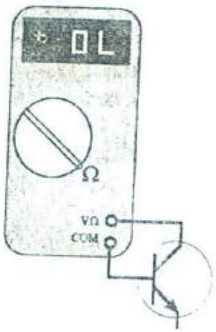


Figure 4-36
Transistor testing by use of a digital ohmmeter.

Example 4-6

The circuit and *XY* recorder in Fig. 4-38 are to be used to plot transistor common-emitter output characteristics to $V_{CE(max)}$ = 10 V and $I_{C(max)}$ = 20 mA. Select V_{CC} and R_2, and determine appropriate V/cm scales for the *XY* recorder. The plotted characteristics are to be approximately 20 cm x 20 cm.

Solution

For $I_{C(max)}$ corresponding to 20 cm,

$$\text{vertical scale} = \frac{I_{C(max)}}{\text{scale length}} = \frac{20\text{ mA}}{20\text{ cm}}$$

$$= 1\text{ mA/cm}$$

Select a vertical scale of 1 V/cm, so that 20 cm represents 20 V and 20 mA.

$$R_2 = \frac{20\text{ V}}{20\text{ mA}}$$

$$= 1\text{ k}\Omega$$

$$V_{CC} = V_{CE(max)} + (I_{C(max)} \times R_2)$$

$$= 10\text{ V} + (20\text{ mA} \times 1\text{ k}\Omega)$$

$$= 30\text{ V}$$

$$\text{horizontal scale} = \frac{V_{CE(max)}}{\text{scale length}} = \frac{10\text{ V}}{20\text{ cm}}$$

$$= 0.5\text{ V/cm}$$

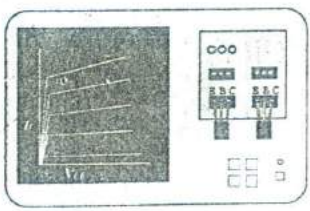


Figure 4-37
A curve tracer can be use to compare the characteristics of a transistor of unknown quality with the characteristics of a known good device.

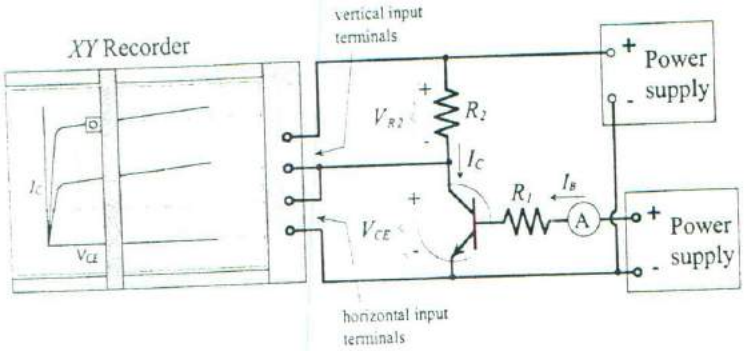


Figure 4-38
Transistor characteristic plotting on an XY recorder. V_{CE} produces horizontal deflection, and V_{R2} causes vertical deflection.

Practise Problems

4-7.1 A transistor with $V_{CE(max)} = 40$ V and $I_C = 100$ mA is to have its common-emitter output characteristics plotted on an *XY*-recorder as in Fig. 4-38. Select an appropriate supply voltage and collector resistance value, and determine suitable *V/cm* scales for the *XY*-recorder to give characteristics approximately 25 cm x 25 cm.

Chapter-4 Review Questions

Section 4-1

4-1 Draw a block diagrams of an unbiased *npn* transistor. Identify each part of the device, and show the depletion regions and barrier voltages. Briefly explain.

4-2 Repeat Question 4-1 for a *pnp* transistor.

4-3 Sketch a correctly-biased *npn* transistor. Show the effect of the bias voltages on the depletion regions and barrier voltages, and show the movement of charge carriers through the transistor. Explain the transistor operation.

4-4 Repeat Question 4-3 for a correctly-biased *pnp* transistor.

4-5 Draw circuit symbols for *npn* and *pnp* transistors. Identify current directions and bias voltage polarities.

Section 4-2

4-6 Draw a sketch to show the various current components in a transistor. Briefly explain the origin of each current. Write an equations relating I_E, I_B, and I_C.

4-7 Write equations for I_C in terms of I_E, and for I_C in terms of I_B. Define α_{dc} and β_{dc}, and state typical values for each.

Section 4-3

4-8 Sketch a circuit diagram to show how a transistor can be used for amplification of direct current changes and alternating signal currents. Briefly explain.

4-9 Draw a circuit diagram to show how a transistor can amplify direct voltage changes and alternating signal voltages. Briefly explain.

Section 4-4

4-10 Explain transistor *common-base* configuration, and sketch a circuit for determining common-base characteristics.

4-11 Sketch typical transistor *common-base* input characteristics and output characteristics. Explain the shape of each set of characteristics.

4-12 Explain transistor *punch-through*, and how it occurs.

4-13 Sketch typical transistor *common-base* current-gain characteristics. Explain the shape of the characteristics.

Section 4-5

4-14 Explain transistor *common-emitter* configuration, and draw a circuit for determining common-emitter characteristics.

4-15 Sketch typical transistor *common-emitter* input and output characteristics. Explain the shape of the characteristics.

4-16 Sketch typical transistor *common-emitter* current-gain characteristics. Explain the shape of the characteristics.

Section 4-6

4-17 Explain transistor *common-collector* configuration, and draw a circuit for determining common-collector characteristics.

4-18 Sketch typical transistor *common-collector* output and current-gain characteristics, and explain the shape of the characteristics.

4-19 Sketch typical transistor *common-collector* input characteristics. Discuss the shape of the characteristics.

Section 4-7

4-20 Describe how a transistor may be quickly tested while still connected in a circuit.

4-21 Discuss how a transistor may be tested by means of an ohmmeter, and by use of a digital multimeter.

4-22 Sketch a diagram to show how an *XY* recorder may be used for plotting transistor characteristics.

Chapter-4 Problems

Section 4-2

4-1 Calculate the values of I_C and I_E for a transistor with α_{dc} = 0.97 and I_B = 50 μA. Also, determine β_{dc} for the device.

4-2 A transistor has measured current levels of I_C = 5.25 mA and

I_B = 100 μA. Calculate I_E, α_{dc}, and β_{dc}, and determine the new I_B level to give I_C = 15 mA.

4-3 Calculate the collector and emitter current levels for a transistor with α_{dc} = 0.99 and I_B = 20 μA.

4-4 The following current measurements were made on a transistor: I_C = 12.42 mA, I_B = 200 μA. Determine I_E, α_{dc}, and β_{dc}. Also, determine the new I_C level when I_B is 150 μA.

4-5 A transistor with measured current levels of I_C = 16 mA and I_E = 16.04 mA is replaced with another transistor that has β_{dc} = 25. Calculate the new level of I_C and I_E, assuming that the base current remains constant.

Section 4-3

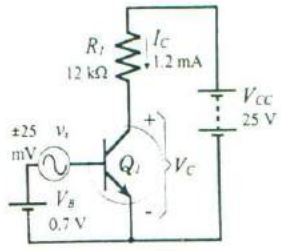
4-6 The transistor in the circuit in Fig. 4-39(a) has the input characteristics in Fig. 4-39(b). If β_{dc} = 50, calculate the collector voltage when V_{BE} = 0.7 V.

4-7 A ±25 mV *ac* input is applied in series with the base of the transistor in Problem 4-6. Calculate the circuit voltage gain.

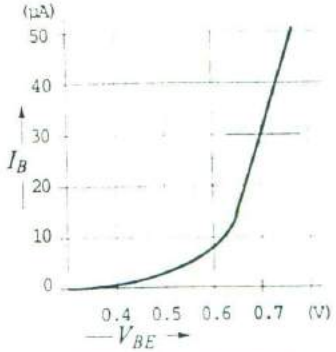
4-8 Determine the new V_{CE} level for the circuit in Fig. 4-39(a) if the transistor V_{BE} is adjusted to 0.75 V.

4-9 Calculate the new voltage gain for the circuit in Fig. 4-39(a) when R_1 is changed to 6.8 kΩ.

4-10 When the transistor in the circuit of Fig. 4-39(a) is changed, V_C is measured as 9 V. Assuming that I_B remains constant at 30 μA, calculate the current gain for the new transistor.



(a) Transistor circuit



(b) V_{BE} I_B characteristic for Q_1

Figure 4-39

Section 4-4

4-11 Derive the *common-base* current gain characteristics for V_{CB} = -5 V from the output characteristics in Fig. 4-40.

4-12 Refer to the *common-base* output characteristics in Fig. 4-22. Derive the current gain characteristics for V_{CB} = -8 V.

4-13 From the *common-base* input characteristics in Fig. 4-21, estimate the level of I_E when V_{EB} = 0.72 V and V_{CB} = 6 V.

Section 4-5

4-14 Derive the current gain characteristics for V_{CE} = 9 V from the *common-emitter* output characteristics in Fig. 4-41.

4-15 From the *common-emitter* input characteristics in Fig. 4-27, estimate the level of I_B when V_{BE} = 0.72 V and V_{CE} = 2 V.

4-16 Refer to the *common-emitter* output characteristics in Fig. 4-28. Derive the current gain characteristics for V_{CE} = 14 V.

4-17 Determine the level of I_C for a transistor with the *common-emitter* output characteristics in Fig. 4-28 when I_B = 60 μA and when I_B = 30 μA, with V_{CE} = 5 V in each case. Also calculate β_{dc}.

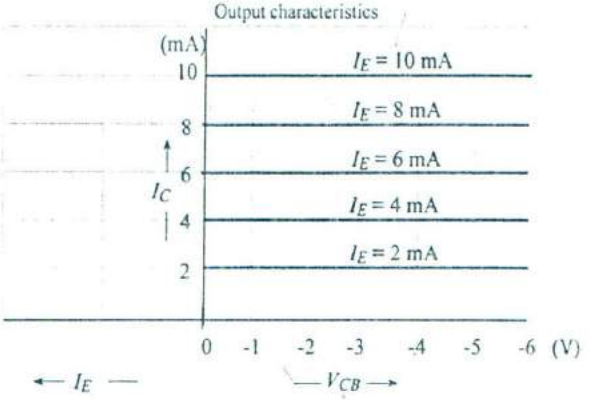


Figure 4-40

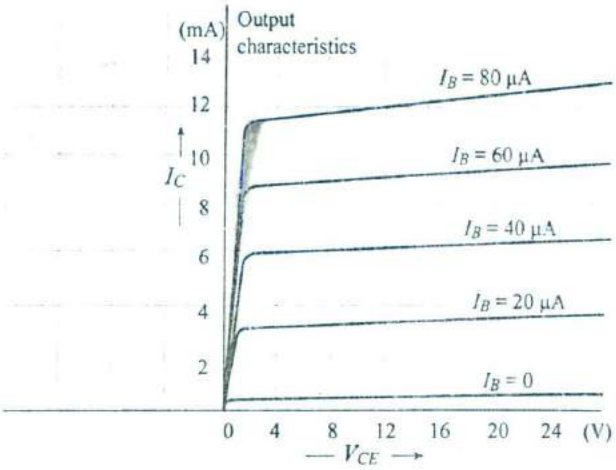


Figure 4-41

Section 4-6

4-18 Refer to the *common-collector* output characteristics in Fig. 4-32. Derive the current gain characteristics for V_{EC} = 10 V.

4-19 Calculate the input voltage (V_{BC}) for the *common-collector* circuit in Fig. 4-31 when V_{EC} = 10 V and V_{EB} = 0.7 V.

4-20 Determine the level of V_{BC} from the *common-collector* input characteristics in Fig. 4-33 when I_B = 20 μA and V_{EC} = 4 V.

Section 4-7

4-21 An *XY* recorder is to be used to plot transistor *common-emitter* output characteristics as in Fig. 4-38. The transistor current and voltage levels are to be $V_{CE(max)}$ = 20 V and $I_{C(max)}$ = 50 mA. Select V_{CC} and resistor R_2, and determine appropriate V/cm scales for the *XY* recorder. The plotted characteristics size is to be approximately 25 cm x 25 cm.

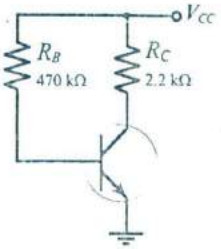
4-22 Sketch a circuit diagram for using an *XY* recorder to determine the *common-emitter* input characteristics for a transistor. Select suitable circuit components and V/cm scales to plot 20 cm x 20 cm characteristics with maximum levels of V_{BE} = 1 V and I_B = 100 μA.

Practise Problem Answers

4-2.1 0.98, 50 μA, 50
4-2.2 2.25 mA, 2.28 mA
4-3.1 71.5
4-3.2 80
4-6.1 1.5 V, 3.5 V
4-7.1 1 V/cm, 250 Ω, 65 V, 1.5 V cm

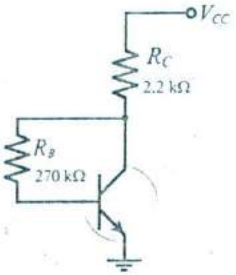
Chapter 5

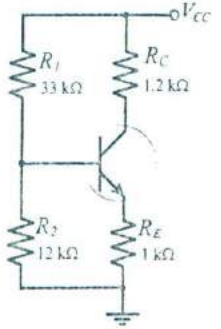
BJT Biasing



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Objectives

You will be able to:

1. *Draw dc load lines for transistor circuits, identify circuit Q-points, and estimate the maximum circuit output voltage variations.*
2. *Sketch base bias, collector-to-base bias, and voltage divider bias circuits, and explain the operation of each circuit.*
3. *Analyze various types of BJT bias circuits to determine circuit voltage and current levels.*
4. *Trouble-shoot non-operational BJT bias circuits.*
5. *Design base bias, collector-to-base bias, and voltage divider bias circuits, and select appropriate standard value components.*
6. *Sketch several unusual types of BJT bias circuit, and explain the operation of each circuit.*
7. *Analyze and design the bias circuit types referred to in item 6.*
8. *Discuss the thermal stability of BJT bias circuits, and determine the effects of I_{CBO} and V_{BE} changes with temperature.*
9. *Sketch bias circuits for direct-coupled and capacitor-coupled switching transistors, and explain the operation of each circuit.*
10. *Analyze and design switching transistor bias circuits.*

Introduction

Transistors used in amplifier circuits must be biased into an *on* state with constant (direct) levels of collector, base, and emitter current, and constant terminal voltages. The levels of I_C and V_{CE} define the transistor *dc operating point*, or *quiescent point*. The circuit that provides this state is known as a *bias circuit*. Ideally, the current and voltage levels in a bias circuit should remain absolutely constant. In practical circuits these quantities are affected by the transistor current gain (h_{FE}) and by temperature changes. The best bias circuits have the greatest stability; they hold the currents and voltages substantially constant regardless of the h_{FE} and temperature variations. The simplest bias circuits are the least costly because they use the smallest number of components, but they are not as stable as more complex circuits.

5-1 DC Load Line and Bias Point

DC Load Line

The *dc load line* for a transistor circuit is a straight line drawn on the transistor output characteristics. For a common-emitter (*CE*) circuit, the load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance (R_C) and a given supply voltage (V_{CC}). The load line shows all corresponding levels of I_C and V_{CE} that can exist in a particular circuit.

Consider the common-emitter circuit in Fig. 5-1. Note that the polarity of the transistor terminal voltages are such that the base-emitter junction is forward biased and the collector-base junction is reverse biased. These are the normal bias polarities for the transistor junctions. The *dc* load line for the circuit in Fig. 5-1 is drawn on the device common-emitter characteristics in Fig. 5-2.

From Fig. 5-1, the collector-emitter voltage is,

V_{CE} = (supply voltage) - (voltage drop across R_C)

or,
$$\mathbf{V_{CE} = V_{CC} - I_C R_C} \qquad \textbf{(5-1)}$$

If the base-emitter voltage (V_{BE}) is zero, the transistor is not conducting and $I_C = 0$. Substituting the V_{CC} and R_C values from Fig. 5-1 into Eq. 5-1,

$$V_{CE} = 20\text{ V} - (0 \times 10\text{ k}\Omega)$$
$$= 20\text{ V}$$

Plot *point A* on the common-emitter characteristics in Fig. 5-2 at $I_C = 0$ and $V_{CE} = 20$ V. This is one point on the dc load line.

Now assume a collector current of 2 mA, and calculate the corresponding collector-emitter voltage level.

$$V_{CE} = 20\text{ V} - (2\text{ mA} \times 10\text{ k}\Omega)$$
$$= 0\text{ V}$$

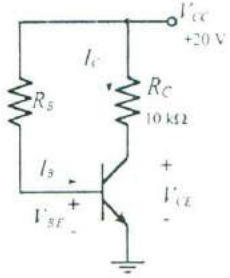


Figure 5-1
Transistor circuit with collector resistor R_C.

Plot *point B* on Fig. 5-2 at $V_{CE} = 0$ and $I_C = 2$ mA. The straight line drawn through *point A* and *point B* is the *dc load line* for $R_C = 10$ kΩ and $V_{CC} = 20$ V. If either of these two quantities is changed, a new load line must be drawn.

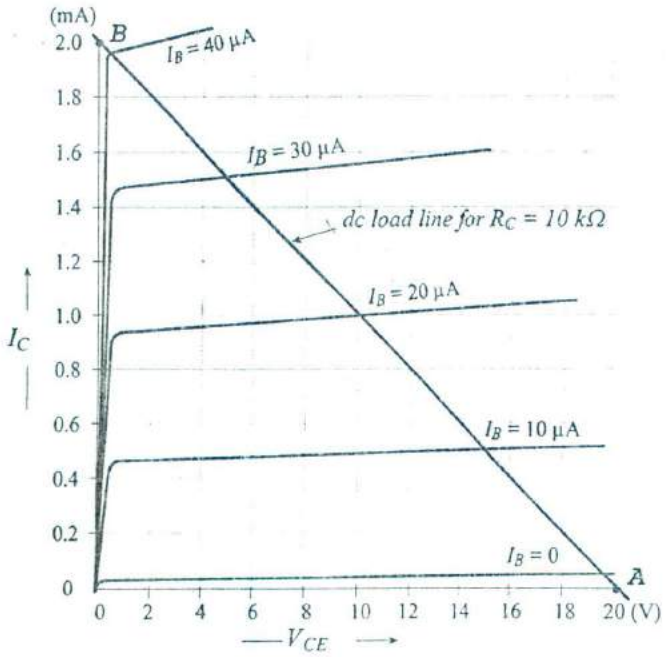


Figure 5-2
DC load line drawn upon transistor common-emitter output characteristics.

As already stated, the *dc* load line represents all corresponding I_C and V_{CE} levels that can exist in the circuit, as represented by Eq. 5-1. For example, a point plotted at $V_{CE} = 16$ V and $I_C = 1.5$ mA on Fig. 5-2 does not appear on the load line. This combination of voltage and current cannot exist in this particular circuit, (Fig. 5-1). Knowing any one of I_B, I_C, or V_{CE}, it is easy to determine the other two from a *dc* load line drawn on the device characteristics.

It is not always necessary to have the device characteristics in order to draw the *dc* load line. A simple graph of I_C versus V_{CE} can be used, as demonstrated in Example 5-1.

Example 5-1

Draw the new *dc* load line for the circuit in Fig. 5-1 when $R_C = 12$ kΩ.

Solution

Prepare a graph for I_C versus V_{CE}, (Fig. 5-3).

when $I_C = 0$,
Eq. 5-1,

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 0$$
$$= 20\text{ V}$$

Plot *point A* on Fig. 5-3 at,

$$I_C = 0 \text{ and } V_{CE} = 20 \text{ V}$$

when $V_{CE} = 0$,
from Eq. 5-1, $0 = V_{CC} - I_C R_C$

giving, $$I_C = \frac{V_{CC}}{R_C} = \frac{20 \text{ V}}{12 \text{ k}\Omega}$$

$$\approx 1.7 \text{ mA}$$

Plot *point B* on Fig. 5-3 at,

$$I_C = 1.7 \text{ mA and } V_{CE} = 0 \text{ V}.$$

Draw the *dc* load line through *points A* and *B*.

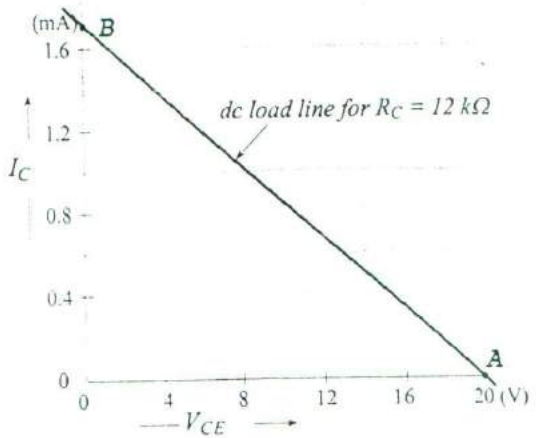


Figure 5-3
DC load line for Example 5-1.

DC Bias Point (Q-Point)

The *dc bias point*, or *quiescent point (Q-point)* (also known as the *dc operating point*), identifies the transistor collector current and collector-emitter voltage when there is no input signal at the base terminal. Thus, it defines the *dc* conditions in the circuit. When a signal is applied to the transistor base, I_B varies according to the instantaneous amplitude of the signal. This causes I_C to vary, and consequently produces a variation in V_{CE}.

Consider the circuit in Fig. 5-4, and the 10 kΩ load line drawn for the circuit in Fig. 5-5. Assume that the bias conditions are as identified by the *Q-point* on the load line,

$$I_B = 20 \text{ μA}, I_C = 1 \text{ mA, and } V_{CE} = 10 \text{ V}$$

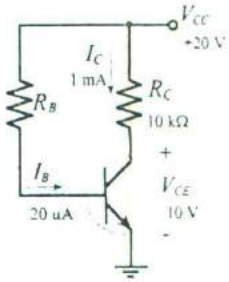


Figure 5-4
Transistor circuit with a bias point (Q-point) at V_{CE} = 10 V and I_C = 1 mA.

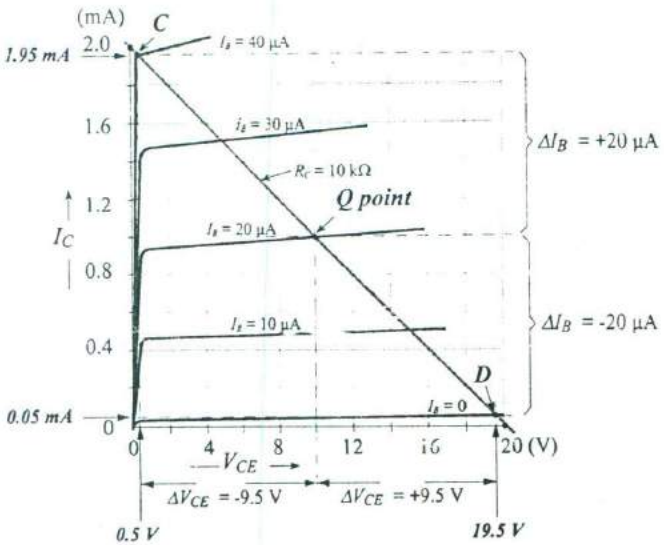


Figure 5-5
DC load line for transistor with a bias point (Q-point) at V_{CE} = 10 V and I_C = 1 mA. The transistor may be biased to any point on the dc load line.

When I_B is increased from 20 μA to 40 μA, I_C becomes approximately 1.95 mA and V_{CE} becomes 0.5 V, as illustrated at point *C* on the load line. The V_{CE} change from the *Q-point* is,

$$\Delta V_{CE} = 10\text{ V} - 0.5\text{ V}$$
$$= 9.5\text{ V}$$

So, increasing I_B by 20 μA (from 20 μA to 40 μA) caused V_{CE} to decrease by 9.5 V, (from 10 V to 0.5 V).

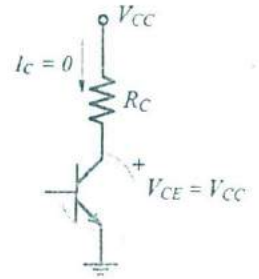
Now look at the effect of decreasing the base current. When I_B is reduced from 20 μA to zero, I_C goes down to approximately 0.05 mA, and V_{CE} goes up to 19.5 V (point *D* on the load line in Fig. 5-5). So, the V_{CE} change is,

$$\Delta V_{CE} = 19.5 - 10\text{ V}$$
$$= 9.5\text{ V}$$

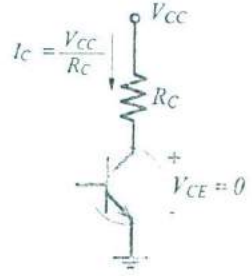
Decreasing I_B by 20 μA (From 20 μA to zero) caused V_{CE} to increase by 9.5 V (from 10 V to 19.5 V). It is seen that with the *Q-point* at I_C = 1 mA and V_{CE} = 10 V, an I_B variation of ±20 μA produces a collector voltage swing of $\Delta V_{CE} = \pm 9.5$ V.

The base current does not have to be varied by the maximum amounts discussed above; it can be increased and decreased by smaller amounts. For example, a base current change of ±10 μA (from the *Q-point* on Fig. 5-5) would produce a collector current change of ±0.5 mA, and a collector-emitter voltage change of ±5 V.

The maximum possible transistor collector-emitter voltage swing for a given circuit can be determined without using the transistor characteristics. For convenience, it may be assumed that I_C can be driven to zero at one extreme and to V_{CC}/R_C at the other extreme, [see Fig. 5-6]. This changes the collector-emitter voltage from $V_{CE} = V_{CC}$ to $V_{CE} = 0$, as illustrated in Fig. 5-7. Thus, with the *Q-point* at the center of the load line, the maximum possible collector voltage swing is seen to be approximately $\pm V_{CC}/2$



(a) $V_{CE} \approx V_{CC}$ when $I_C = 0$



(b) $V_{CE} \approx 0$ when $I_C = V_{CC}/R_C$

Figure 5-6
The collector-emitter voltage of a transistor can range from approximately zero to V_{CC}.

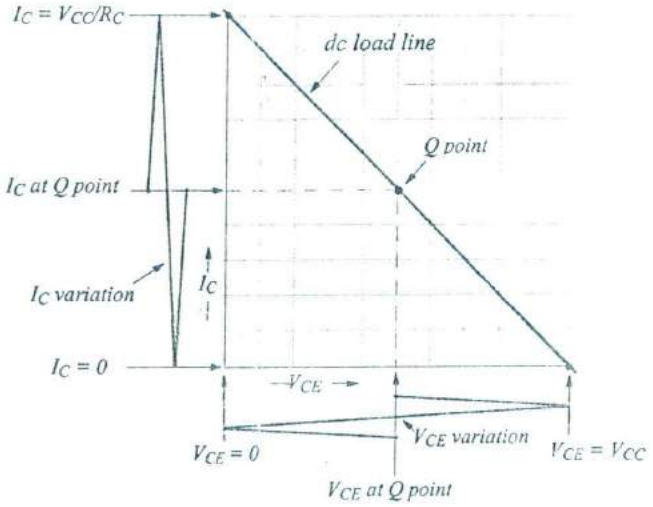
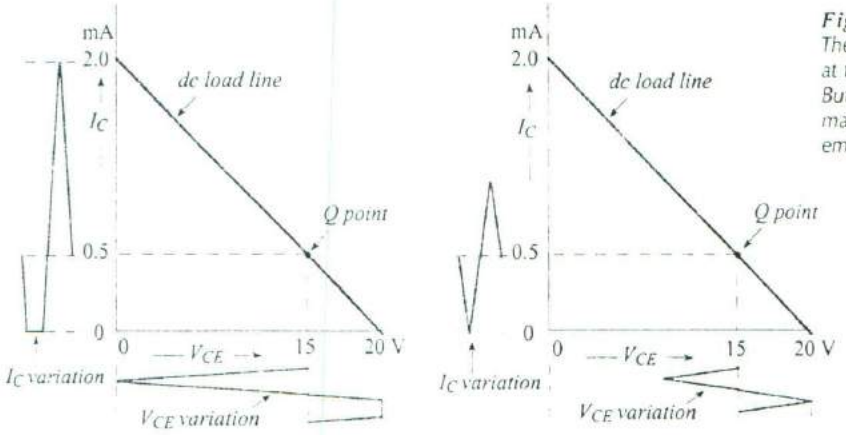


Figure 5-7
Transistor collector-emitter voltage (V_{CE}) ranges from approximately V_{CC} to zero, when I_C goes from zero to V_{CC}/R_C.

Q-point Selection

Suppose that, instead of being biased half way along the load line, the transistor is biased at I_C = 0.5 mA, and V_{CE} = 15 V, as shown in Fig. 5-8(a). Increasing the collector current to 2 mA reduces V_{CE} to zero, giving ΔV_{CE} = -15 V. Reducing I_C to zero increases V_{CE} to V_{CC}, producing ΔV_{CE} = +5 V



(a) Assymmetrical V_{CE} swing (b) Symmetrical V_{CE} swing

Figure 5-8
The Q-point does not have to be at the centre of the dc load line. But, its position determines the maximum symmetrical collector-emitter voltage swing.

When used as an amplifier, the transistor output (collector-emitter) voltage must swing up and down by equal amounts; that is, the output voltage swing must be symmetrical above and below the bias point. So, the asymmetrical V_{CE} swing of -15 V +5 V illustrated in Fig. 5-8(a) is unsuitable. If I_C is driven up and down by ±0.5 mA [see Fig. 5-8(b)], a symmetrical output voltage swing of ±5 V is obtained. This is the maximum symmetrical output voltage swing that can be achieved with the bias point shown in Fig. 5-8.

In many cases circuits are designed to have the *Q-point* at the center of the load line (as in Figs. 5-5 and 5-7) to give the largest possible symmetrical output voltage swing. This is especially true for some large signal amplifiers, (see Chapter 18). Small signal amplifiers (discussed Chapter 12) usually require an output voltage swing not greater than ±1 V. So,

transistors in amplifiers do NOT all have to be biased at the center of the dc load line.

Example 5-2

The transistor circuit in Fig. 5-9 has the collector characteristics shown in Fig. 5-10. Determine the circuit *Q-point* and estimate the maximum symmetrical output voltage swing. Note that V_{CC} = 18 V, R_C = 2.2 kΩ, and I_B = 40 μA.

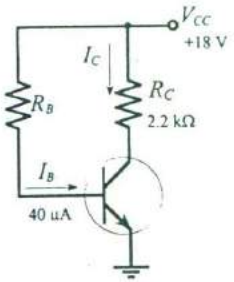


Figure 5-9
Circuit for Example 5-2.

Solution

Eq. 5-1, $V_{CE} = V_{CC} - I_C R_C$

when $I_C = 0$, $V_{CE} = V_{CC} - 0$

$= 18\ V$

Plot *point A* on Fig. 5-10 at,

$I_C = 0$ and $V_{CE} = 18\ V$

when $V_{CE} = 0$, $0 = V_{CC} - I_C R_C$

or, $$I_C = \frac{V_{CC}}{R_C} = \frac{18\ V}{2.2\ k\Omega}$$

$\approx 8.2\ mA$

Plot *point B* on Fig. 5-10 at,

$I_C = 8.2\ mA$ and $V_{CE} = 0\ V$,

Draw the *dc load line* through *points A* and *B*. The *Q-point* is at the intersection of the load line and the $I_B = 40\ \mu A$ characteristic.

The *dc* bias conditions are,

$I_C \approx 4.1\ mA$ and $V_{CE} \approx 9\ V$

The maximum symmetrical output voltage swing is,

$\Delta V_{CE} \approx \pm 9\ V$

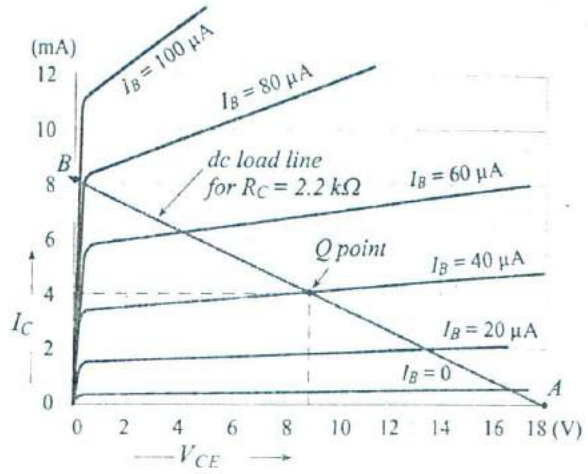


Figure 5-10
Transistor Common-emitter output characteristics and dc load line for Example 5-2.

Effect of Emitter Resistor

Figure 5-11(a) shows a circuit that has a resistor (R_E) in series with the transistor emitter terminal, and the supply voltage connected directly to the collector terminal. In this case R_E is the *dc* load, and Eq. 5-1 is rewritten as,

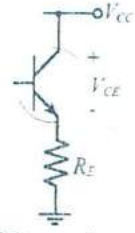
$$V_{CE} = V_{CC} - I_E R_E$$

The *dc* load line is drawn exactly as discussed, with I_E taken as equal to I_C for convenience.

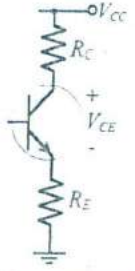
In Fig. 5-11(b) collector and emitter resistors R_C and R_E are both present, and the total *dc* load in series with the transistor is ($R_C + R_E$). For drawing the dc load line, Eq. 5-1 is modified to,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Note that the voltage drop across the emitter resistor is actually ($I_E R_E$), but again for convenience I_E is taken as equal to I_C.



(a) $R_{L(dc)} = R_E$



(b) $R_{L(dc)} = (R_C + R_E)$

Figure 5-11
The transistor dc load is the sum of the resistors in series with the collector and emitter terminals.

Practise Problems

5-1.1 Draw the new *dc* load line and determine the Q point for the circuit in Example 5-2 when the supply voltage is changed to 12 V.

5-1.2 A common-emitter circuit as in Fig. 5-1 has $R_C = 12\,k\Omega$ and $V_{CC} = 15$ V. Draw the *dc* load line on the characteristics in Fig. 5-2. Specify the Q point, and determine the maximum symmetrical output voltage swing if the base current is 10 μA.

5-1.3 A transistor circuit as in Fig. 5-11(b) has $V_{CC} = 12$ V, $R_C = 820\,\Omega$, $R_E = 380\,\Omega$, and $I_B = 60\,\mu$A. Draw the *dc* load line on the characteristics in Fig. 5-10, and determine the maximum symmetrical output voltage swing.

5-2 Base Bias

Circuit Operation and Analysis

The transistor bias arrangement shown in Fig. 5-12 is known as *base bias* and also as *fixed current bias*. The base current is a constant quantity determined by supply voltage V_{CC} and base resistor R_B. Because V_{CC} and R_B are constant quantities, I_B remains fixed at a particular level. Unlike some other bias circuits, the base current in a base bias circuit is not affected by the transistor current gain.

From Fig. 5-12, the voltage drop across R_B is $(V_{CC} - V_{BE})$, and the base current is,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (5\text{-}2)$$

In Eq. 5-2 the base-emitter voltage (V_{BE}) is taken as 0.7 V for a silicon transistor, and as 0.3 V for a germanium device.

The transistor collector current is calculated as,

$$I_C = h_{FE} I_B \qquad (5\text{-}3)$$

The collector current is now used with Eq. 5-1 ($V_{CE} = V_{CC} - I_C R_C$) to calculate the collector-emitter voltage. Thus, when the supply voltage and component values are known, a base bias circuit is easily analysed to determine the circuit current and voltage levels.

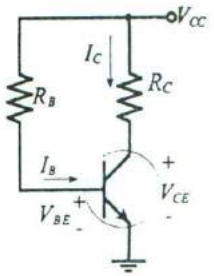


Figure 5-12
Base bias circuit, also known as fixed current bias. The base current remains constant at, $I_B = (V_{CC} - V_{BE})/R_B$.

Example 5-3

The base bias circuit in Fig. 5-13 has $R_B = 470\,k\Omega$, $R_C = 2.2\,k\Omega$, $V_{CC} = 18$ V, and the transistor has $h_{fe} = 100$. Determine I_B, I_C, and V_{CE}.

Solution

Eq. 5-2, $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{470\,k\Omega}$$

$$= 36.8\,\mu\text{A}$$

Eq. 5-3, $I_C = h_{fe} I_B = 100 \times 36.8\,\mu A$
$= 3.68$ mA

Eq. 5-1, $V_{CE} = V_{CC} - I_C R_C = 18\text{ V} - (3.68\text{ mA} \times 2.2\text{ k}\Omega)$
$= 9.9$ V

The circuit conditions are illustrated in Fig. 5-13.

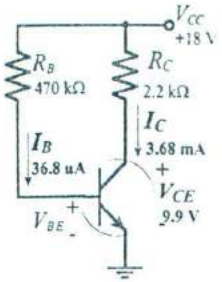


Figure 5-13
Circuit for Example 5-3.

Effect of $h_{FE(max)}$ and $h_{FE(min)}$

When the transistor *dc* current gain is known, it is quite easy to determine the circuit bias conditions exactly as in Example 5-3. However, in practise the precise current gain of each transistor is normally not known. The transistor is usually identified by its type number, and then the maximum and minimum values of current gain can be obtained from the manufacturer's data sheet. In circuit analysis it is sometimes convenient to use a typical h_{FE} value. However, as demonstrated in Example 5-4, $h_{FE(max)}$ and $h_{FE(min)}$ must be used to calculate the range of possible levels of I_C and V_{CE}.

Example 5-4

Calculate the maximum and minimum levels of I_C and V_{CE} for the base bias circuit in Ex. 5-3 when $h_{FE(min)} = 50$ and $h_{FE(max)} = 200$.

Solution

The base current in this circuit is unaffected by h_{fe}, and so (as in Ex. 5-3),

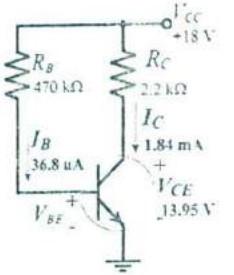
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega}$$
$$= 36.8\,\mu A$$

for $h_{FE(min)}$, $I_C = h_{FE(min)} I_B = 50 \times 36.8\,\mu A$
$= 1.84$ mA

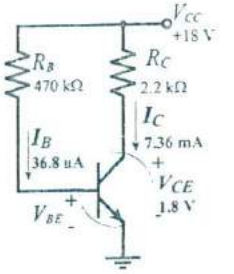
and, $V_{CE} = V_{CC} - I_C R_C = 18\text{ V} - (1.84\text{ mA} \times 2.2\text{ k}\Omega)$
$= 13.95$ V [See Fig. 5-14(a)]

for $h_{FE(max)}$, $I_C = h_{FE(max)} I_B = 200 \times 36.8\,\mu A$
$= 7.36$ mA

and, $V_{CE} = V_{CC} - I_C R_C = 18\text{ V} - (7.36\text{ mA} \times 2.2\text{ k}\Omega)$
$= 1.8$ V [See Fig. 5-14(b)]



(a) Conditions for $h_{FE(min)}$



(b) Conditions for $h_{FE(max)}$

Figure 5-14
Circuit current and voltage levels for $h_{FE(min)}$ and $h_{FE(max)}$ as determined in Example 5-4.

Note that the typical h_{FE} value of 100 used in Ex. 5-3 gives I_C = 3.68 mA and V_{CE} = 9.9 V. But, applying the $h_{FE(min)}$ and $h_{FE(max)}$ values in Example 4-4 results in an I_C range of 1.84 mA to 7.36 mA) and V_{CE} ranging from 1.8 V to 13.95 V. The different I_C and

V_{CE} levels determined in Examples 5-3 and 5-4 are illustrated by the three *Q points* in Fig. 5-15. Transistors of a given type number always have a wide range of h_{FE} values (the h_{FE} *spread*), so

$h_{FE(max)}$ and $h_{FE(min)}$ should always be used for practical circuit analysis.

The base bias circuit is rarely employed because of the uncertainty of the *Q point*. More predictable results can be obtained with other types of bias circuit.

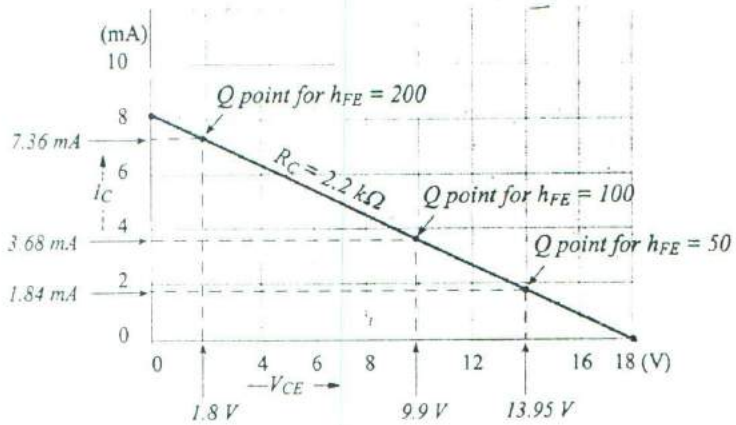
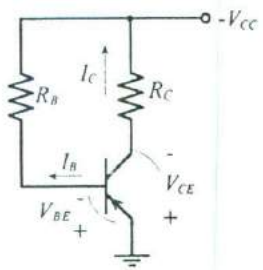


Figure 5-15
The transistor h_{FE} value has a major effect on the Q point for a base bias circuit.

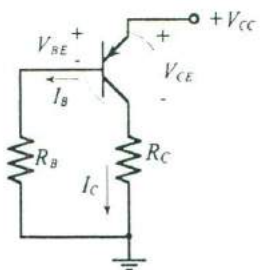
Base Bias Using a pnp Transistor

All of the base bias circuits discussed so far use *npn* transistors. Figure 5-16 shows circuits that use *pnp* transistors. In Fig. 5-16(a) note that the voltage polarities and current directions are reversed compared to *npn* transistor base bias circuits. Because it is normal to show the supply voltage with the positive terminal uppermost, the circuit of Fig. 5-16(a) is redrawn in Fig. 5-16(b). This is the way that the circuit would usually be shown.

Equations 5-1, 5-2, and 5-3 can be applied for analysing *pnp* transistor base bias circuit exactly as for *npn* transistor circuits.



(a) Base bias circuit using an *pnp* transistor



(b) Usual way to show a *pnp* transistor circuit; with the + terminal of the supply uppermost

Figure 5-16
Base bias circuits using pnp transistors.

Practise Problems

5-2.1 If the base bias circuit in Example 5-3 uses a transistor with $h_{FE(min)}$ = 75 and $h_{FE(max)}$ = 250, determine the maximum and minimum levels of I_C and V_{CE}.

5-2.2 A base bias circuit has V_{CC} = 24 V, R_B = 390 kΩ, R_C = 3.3 kΩ, and V_{CE} = 10 V. Calculate the transistor h_{FE} value, and determine the new V_{CE} level when a new transistor is substituted with h_{FE} = 100.

5-3 Collector-to-Base Bias

Circuit Operation and Analysis

The *collector-to-base bias* circuit shown in Fig. 5-17(a) has the base resistor (R_B) connected between the transistor collector and base terminals. As will be demonstrated, this circuit has significantly improved bias stability for h_{FE} changes compared to base bias.

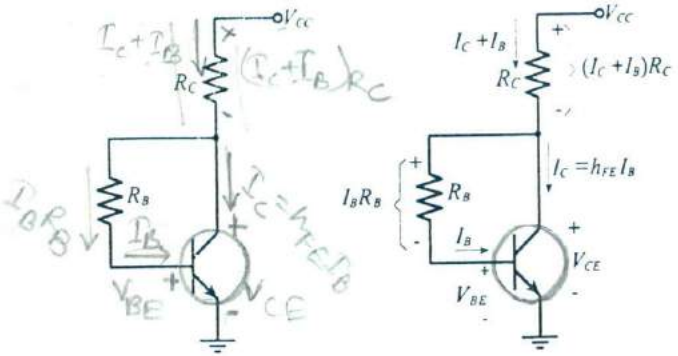
Refer to Fig. 5-17(b) and note that the voltage across R_B is dependent on V_{CE}.

$$V_{CE} = V_{BE} + I_B R_B \tag{5-4}$$

giving,
$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

Also, V_{CE} is dependent on the level of I_C and I_B.

$$V_{CE} = V_{CC} - R_C(I_C + I_B) \tag{5-5}$$



(a) Collector-to-base bias circuit

(b) Circuit currents and voltage drops

Figure 5-17
Collector-to-base bias circuits. Any change in V_{CE} changes I_B. The I_B change causes I_C to change, and this tends to return V_{CE} toward its original level.

If I_C increases above the design level, there is an increased voltage drop across R_C, resulting in a reduction in V_{CE}. The reduced V_{CE} level causes I_B to be lower than its design level, and because $I_C = h_{FE} I_B$, the collector current is also reduced. Thus, an increase in I_C produces a feedback effect that tends to return I_C toward its

original level. Similarly, a reduction in I_C produces an increase in V_{CE} which increases I_B, thus tending to increase I_C back to its original level.

Analysis of this circuit is a little more complicated than base bias analysis. To simplify the process, an equation is first derived for the base current. Substituting for V_{CE} from Eq. 5-4 into Eq. 5-5,

$$V_{BE} + I_B R_B = V_{CC} - R_C(I_C + I_B)$$

Substituting $I_C = h_{FE} I_B$ (from Eq. 5-3) into the above equation,

$$V_{BE} + I_B R_B = V_{CC} - R_C (h_{FE} I_B + I_B)$$

This gives,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{FE} + 1)} \qquad (5\text{-}6)$$

Example 5-5

A collector-to-base bias circuit as in Fig. 5-18 has R_B = 270 kΩ, R_C = 2.2 kΩ, V_{CC} = 18 V, and a transistor with h_{fe} = 100. Analyse the circuit to determine I_B, I_C, and V_{CE}.

Solution

Eq. 5-6,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{fe} + 1)} = \frac{18\text{ V} - 0.7\text{ V}}{270\text{ k}\Omega + 2.2\text{ k}\Omega(100 + 1)}$$
$$= 35.1\ \mu\text{A}$$

Eq. 5-3,
$$I_C = h_{fe} I_B = 100 \times 35.1\ \mu\text{A}$$
$$= 3.51\text{ mA}$$

Eq. 5-5,
$$V_{CE} = V_{CC} - R_C(I_C + I_B)$$
$$= 18\text{ V} - 2.2\text{ k}\Omega(3.51\text{ mA} + 35.1\ \mu\text{A})$$
$$= 10.2\text{ V}$$

The circuit conditions are illustrated in Fig. 5-18.

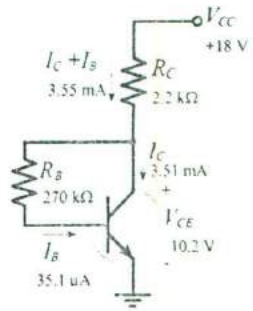


Figure 5-18
Collector-to-base bias circuit for Example 5-5.

Effect of $h_{FE(max)}$ and $h_{FE(min)}$

As discussed for the base bias circuit, transistors of a given type number have a wide range of h_{FE} values, (h_{FE} *spread*). This affects the current and voltage levels in all bias circuits. In the collector-to-base bias circuit, the feedback from the collector to the base reduces the effects of h_{FE} spread. Thus, as demonstrated in Ex. 5-6, collector-to-base bias has greater stability than base bias for a given range of h_{FE} values.

It is important to note that, unlike the situation in a base bias circuit, *the base current in a collector-to-base bias circuit does NOT remain constant* when the transistor h_{FE} value is changed. This is also demonstrated in Example 5-6.

Example 5-6

Calculate the maximum and minimum levels of I_C and V_{CE} for the bias circuit in Ex. 5-5 when $h_{FE(min)} = 50$ and $h_{FE(max)} = 200$.

Solution

for $h_{FE(min)}$,

Eq. 5-6,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{FE} + 1)} = \frac{18\text{ V} - 0.7\text{ V}}{270\text{ k}\Omega + 2.2\text{ k}\Omega(50 + 1)}$$
$$= 42.3\ \mu\text{A}$$

Eq. 5-3,
$$I_C = h_{FE} I_B = 50 \times 42.3\ \mu\text{A}$$
$$= 2.26\text{ mA}$$

Eq. 5-5,
$$V_{CE} = V_{CC} - R_C(I_C + I_B)$$
$$= 18\text{ V} - 2.2\text{ k}\Omega\ (2.26\text{ mA} + 42.3\ \mu\text{A})$$
$$= 12.9\text{ V [see Fig. 5-19(a)]}$$

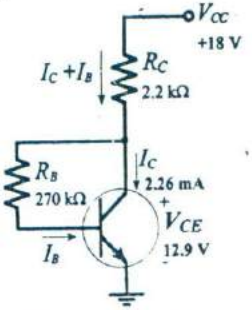
for $h_{FE(max)}$,

Eq. 5-6,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(h_{FE} + 1)} = \frac{18\text{ V} - 0.7\text{ V}}{270\text{ k}\Omega + 2.2\text{ k}\Omega(200 + 1)}$$
$$= 24.3\ \mu\text{A}$$

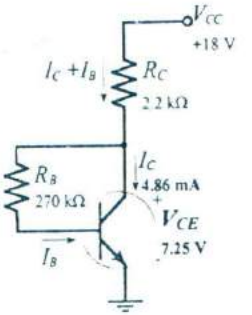
Eq. 5-3,
$$I_C = h_{FE} I_B = 200 \times 24.3\ \mu\text{A}$$
$$= 4.86\text{ mA}$$

Eq. 5-5,
$$V_{CE} = V_{CC} - R_C(I_C + I_B)$$
$$= 18\text{ V} - 2.2\text{ k}\Omega(4.86\text{ mA} + 24.3\ \mu\text{A})$$
$$= 7.25\text{ V [see Fig. 5-19(b)]}$$

The circuit Q *points* are shown in Fig. 5-20.



(a) Conditions for $h_{FE(min)}$



(b) Conditions for $h_{FE(max)}$

Figure 5-19
Circuit conditions for $h_{FE(min)}$ and $h_{FE(max)}$ in the collector-to-base bias circuit analyzed in Ex. 5-6.

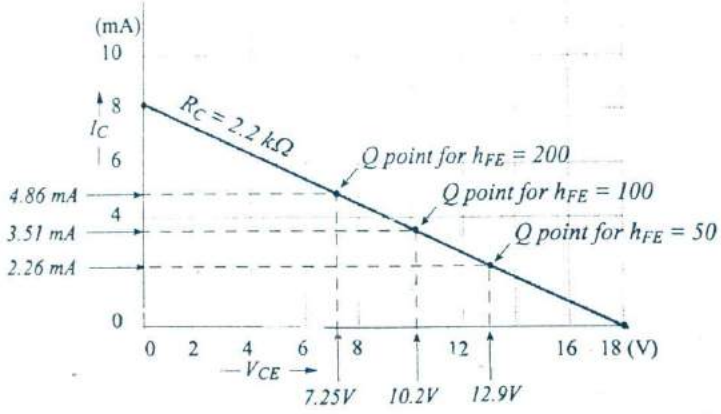


Figure 5-20
Effect of $h_{FE(min)}$ and $h_{FE(max)}$ on the Q point for the collector-to-base bias circuit analyzed in Example 5-6.

As illustrated by the Q points in Fig. 5-20, the typical h_{FE} value used in Ex. 5-5 gives $I_C = 3.51$ mA and $V_{CE} = 10.2$ V. Also, applying the $h_{FE(min)}$ and $h_{FE(max)}$ values produces an I_C range of 2.26 mA to 4.86 mA and V_{CE} levels ranging from 7.25 V to 12.9 V.

Recall that the base bias circuit analysed in Examples 5-3 and 5-4 has the same V_{CC}, R_C and h_{FE} values as used in the collector-to-base bias circuit in Examples 5-5 and 5-6. Comparing the collector-to-base bias circuit Q points in Fig. 5-20 to the base bias circuit Q points Fig. 5-15, it is seen that the Q *points* for the collector-to-base bias circuit are much closer than those for the base bias circuit. The collector-to-base bias circuit clearly has greater stability against h_{FE} spread than the base bias circuit.

Collector-to-base Bias Using a pnp Transistor

A collector-to-base bias circuit using a *pnp* transistor is illustrated in Fig. 5-21. Note that the voltage polarities and current directions are reversed compared to *npn* transistor collector-to-base bias circuit. This circuit can be analysed in exactly the same way as the *npn* transistor circuit.

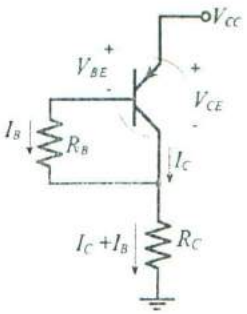


Figure 5-21
Collector-to-base bias circuit using a pnp transistor.

Practise Problems

5-3.1 The collector-to-base bias circuit in Example 5-5 uses a transistor with $h_{FE(min)} = 75$ and $h_{FE(max)} = 250$. Determine the new maximum and minimum levels for I_C and V_{CE}.

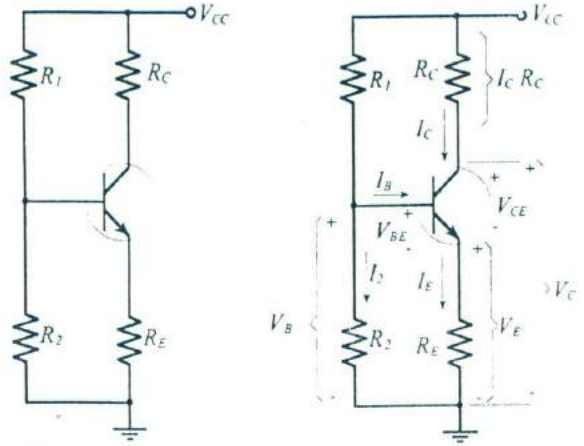
5-3.2 A collector-to-base bias circuit has $V_{CC} = 24$ V, $R_B = 180$ kΩ, $R_C = 3.3$ kΩ, and V_{CE} is measured as 10 V. Calculate the transistor h_{FE} value, and determine the V_{CE} level when a new transistor is substituted with $h_{FE} = 120$.

5-4 Voltage Divider Bias

Circuit Operation

Voltage divider bias, also known as *emitter current bias*, is the most stable of the three basic transistor bias circuits. A voltage divider bias circuit is shown in Fig. 5-22(a), and the current and voltage conditions throughout the circuit are illustrated in Fig. 5-22(b). It is seen that, as well as the collector resistor (R_C), there is an emitter resistor (R_E) connected in series with the transistor. As discussed in Section 5-1, the total *dc* load in series with the transistor is ($R_C + R_E$), and this total resistance must be used when drawing the *dc* load line for the circuit. Resistors R_1 and R_2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage (V_B).

Voltage divider bias circuits are normally designed to have the voltage divider current (I_2) very much larger than the transistor base current (I_B). In this circumstance, V_B is largely unaffected by I_B, so V_B can be assumed to remain constant.



(a) Voltage divider bias circuit

(b) Circuit currents and voltage drops

Figure 5-22
Voltage divider bias circuits. The emitter current remains constant at, $I_E = (V_B - V_{BE})/R_E$.

Referring to Fig. 5-22(b),

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \qquad (5\text{-}7)$$

With V_B constant, the voltage across the emitter resistor is also a constant quantity.

$$V_E = V_B - V_{BE} \qquad (5\text{-}8)$$

This means that the emitter current is constant.

$$I_E = \frac{V_B - V_{BE}}{R_E} \qquad (5\text{-}9)$$

The collector current is approximately equal to the emitter current, so I_C is held at a constant level.

Again referring to Fig. 5-22(b), the transistor collector voltage is,

$$V_C = V_{CC} - (I_C R_C) \qquad (5\text{-}10)$$

The collector-emitter voltage is,

$$V_{CE} = V_C - V_E \qquad (5\text{-}11)$$

V_{CE} can also be determined as,

$$V_{CE} \approx V_{CC} - I_C(R_C + R_E) \qquad (5\text{-}12)$$

Clearly, with I_C and I_E constant, the transistor collector-emitter voltage remains at a constant level.

It should be noted that the transistor h_{FE} value is not involved in any of the above equations.

Approximate Circuit Analysis

If the transistor base current is assumed to be much smaller than the voltage divider current, as discussed above, the circuit currents and voltages can be readily determined by the use of Equations 5-7 through 5-12. Example 5-7 demonstrates the process.

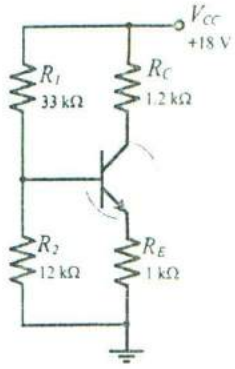


Figure 5-23
Voltage divider bias circuit for Example 5-7.

Example 5-7

Analyse the voltage divider bias in circuit in Fig. 5-23 to determine the emitter voltage, collector voltage, and collector-emitter voltage.

Solution

Eq. 5-7,
$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{18\text{ V} \times 12\text{ k}\Omega}{33\text{ k}\Omega + 12\text{ k}\Omega}$$
$$= 4.8\text{ V}$$

Eq. 5-8,
$$V_E = V_B - V_{BE} = 4.8\text{ V} - 0.7\text{ V}$$
$$= 4.1\text{ V}$$

Eq. 5-9,
$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4.8\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega}$$
$$= 4.1\text{ mA}$$
$$I_C \approx I_E = 4.1\text{ mA}$$

Eq. 5-10,
$$V_C = V_{CC} - (I_C R_C) = 18\text{ V} - (4.1\text{ mA} \times 1.2\text{ k}\Omega)$$
$$= 13.1\text{ V}$$

Eq. 5-11,
$$V_{CE} = V_C - V_E = 13.1\text{ V} - 4.1\text{ V}$$
$$= 9\text{ V}$$

The circuit conditions are illustrated in Fig. 5-24.

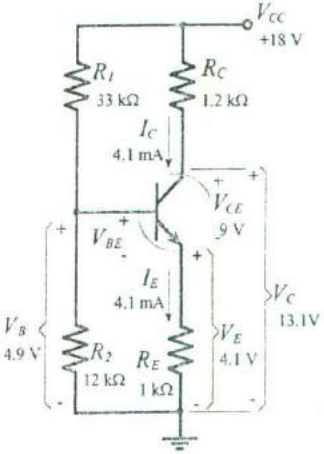


Figure 5-24
Voltage and current conditions for the circuit in Example 5-7.

Precise Circuit Analysis

To precisely analyse a voltage divider bias circuit, the voltage divider must be replaced with its *Thevenin equivalent circuit* (V_T in series with R_T) as illustrated in Fig. 5-25. From Figure 5-25(a),

$$V_T = \frac{V_{CC} \times R_2}{R_1 + R_2} \qquad (5\text{-}13)$$

and R_T is calculated as R_1 in parallel with R_2,

$$R_T = R_1 || R_2 \qquad (5\text{-}14)$$

Referring to Fig. 5-25(b), an equation may be written for the voltage drops around the base-emitter circuit;

$$V_T = I_B R_T + V_{BE} + R_E(I_B + I_C)$$

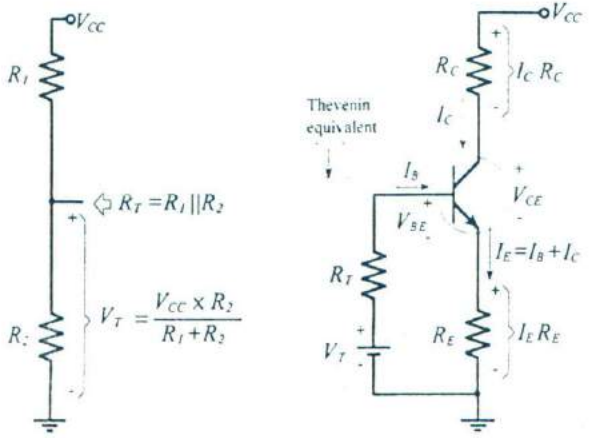
Substituting $I_C = h_{FE} I_B$,

$$V_T = I_B R_T + V_{BE} + R_E I_B(1 + h_{FE})$$

giving,

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})} \qquad \textbf{(5-15)}$$

Once I_B has been determined, I_C can be calculated using the appropriate h_{FE} value, and the transistor terminal voltages can then be calculated. The effects of the maximum and minimum h_{FE} values can also be investigated.



(a) Determining the *Thevenin equivalent circuit* for the voltage divider

(b) Voltage divider bias with *Thevenin equivalent circuit* of the voltage divider

Figure 5-25
For precise analysis of a voltage divider bias circuit, the voltage divider is replaced with its Thevenin equivalent circuit.

Example 5-8

Accurately analyse the voltage divider bias circuit in Example 5-7 to determine I_C, V_E, V_C, and V_{CE} when the transistor $h_{fe} = 100$.

Solution

Eq. 5-13,
$$V_T = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{18\text{ V} \times 12\text{ k}\Omega}{33\text{ k}\Omega + 12\text{ k}\Omega}$$
$$= 4.8\text{ V}$$

Eq. 5-14,
$$R_T = R_1 \| R_2 = 33\text{ k}\Omega \| 12\text{ k}\Omega$$
$$= 8.8\text{ k}\Omega$$

Eq. 5-15,
$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{fE})} = \frac{4.8\text{ V} - 0.7\text{ V}}{8.8\text{ k}\Omega + 1\text{ k}\Omega(1 + 100)}$$
$$= 37.3\ \mu\text{A}$$
$$I_C = h_{fE} I_B = 100 \times 37.3\ \mu\text{A}$$
$$= 3.73\text{ mA}$$

$$I_E = I_B + I_C = 37.3\,\mu A + 3.73\text{ mA}$$
$$= 3.77\text{ mA}$$

$$V_E = I_E R_E = 3.77\text{ mA} \times 1\text{ k}\Omega$$
$$= 3.77\text{ V}$$

Eq. 5-10,
$$V_C = V_{CC} - (I_C R_C) = 18\text{ V} - (3.73\text{ mA} \times 1.2\text{ k}\Omega)$$
$$= 13.52\text{ V}$$

Eq. 5-11,
$$V_{CE} = V_C - V_E = 13.52\text{ V} - 3.77\text{ V}$$
$$= 9.75\text{ V (See Fig. 5-26)}$$

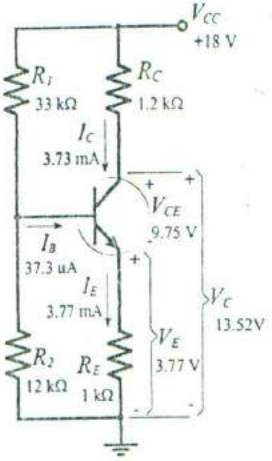


Figure 5-26
Voltage and current levels for the for the voltage divider bias circuit in Example 5-8.

Example 5-9

Accurately analyse the voltage divider bias circuit in Examples 5-7 and 5-8 for the conditions of $h_{FE(min)} = 50$.

Solution

From Ex. 5-8,
$$V_T = 4.8\text{ V and } R_T = 8.8\text{ k}\Omega$$

Eq. 5-15,
$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})} = \frac{4.8\text{ V} - 0.7\text{ V}}{8.8\text{ k}\Omega + 1\text{ k}\Omega(1 + 50)}$$
$$= 68.6\,\mu A$$

$$I_C = h_{FE} I_B = 50 \times 68.6\,\mu A$$
$$= 3.43\text{ mA}$$

$$I_E = I_B + I_C = 68.6\,\mu A + 3.43\text{ mA}$$
$$= 3.5\text{ mA}$$

$$V_E = I_E R_E = 3.5\text{ mA} \times 1\text{ k}\Omega$$
$$= 3.5\text{ V}$$

Eq. 5-10,
$$V_C = V_{CC} - (I_C R_C) = 18\text{ V} - (3.43\text{ mA} \times 1.2\text{ k}\Omega)$$
$$= 13.9\text{ V}$$

Eq. 5-11,
$$V_{CE} = V_C - V_E = 13.9\text{ V} - 3.5\text{ V}$$
$$= 10.4\text{ V [see Fig. 5-27(a)]}$$

Example 5-10

Accurately analyse the voltage divider bias circuit in Examples 5-7, 5-8 and 5-9 for the condition of $h_{FE(max)} = 200$.

Solution

From Ex. 5-8,
$$V_T = 4.8\text{ V and } R_T = 8.8\text{ k}\Omega$$

Eq. 5-15,
$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})} = \frac{4.8\text{ V} - 0.7\text{ V}}{8.8\text{ k}\Omega + 1\text{ k}\Omega(1 + 200)}$$
$$= 19.5\,\mu A$$

$$I_C = h_{FE} I_B = 200 \times 19.5\ \mu A$$
$$= 3.9\ mA$$

$$I_E = I_B + I_C = 19.5\ \mu A + 3.9\ mA$$
$$= 3.92\ mA$$

$$V_E = I_E R_E = 3.92\ mA \times 1\ k\Omega$$
$$= 3.92\ V$$

Eq. 5-10,
$$V_C = V_{CC} - (I_C R_C)$$
$$= 18\ V - (3.9\ mA \times 1.2\ k\Omega)$$
$$= 13.3\ V$$

Eq. 5-11,
$$V_{CE} = V_C - V_E = 13.3\ V - 3.92\ V$$
$$= 9.4\ V\ [\text{see Fig. 5-27(b)}]$$

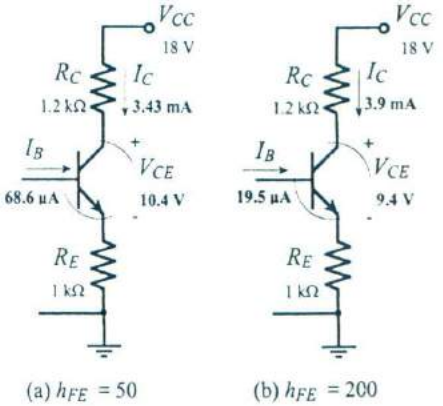


Figure 5-27
Voltage and current conditions produced by $h_{FE(max)}$ and $h_{FE(min)}$ in the voltage divider bias circuit in Examples 5-9 and 5-10.

The maximum and minimum h_{FE} values used in Example 5-9 gives I_C = (3.43 mA to 3.91 mA) and V_{CE} = (9.4 V to 10.4 V), while the typical h_{FE} value of 100 used in Example 5-8 gives I_C = 3.73 mA and V_{CE} = 9.75 V. The I_C and V_{CE} levels determined in Examples 5-8 and 5-9 are shown in Fig. 5-27, and are illustrated by the *Q points* in Fig. 5-28. Note that the analysis using the highest h_{FE} value gives results that are closest to those from the approximate analysis in Example 5-7. This is because the approximate analysis assumes that I_B is very much smaller than the voltage divider current, and the highest h_{FE} gives the lowest I_B level.

For most practical purposes, precise analysis of voltage divider bias circuits is unnecessary. The approximate analysis method gives quite satisfactory results.

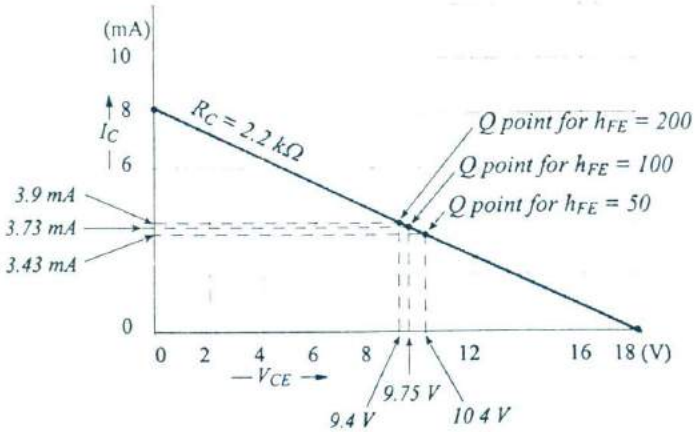


Figure 5-28
Effect of three different h_{FE} values on the Q point for the voltage divider bias circuit analyzed in Examples 5-8, 5-9, and 5-10.

Voltage Divider Bias Using a pnp Transistor

A voltage divider bias circuit using a *pnp* transistor is shown in Fig. 5-29. Note that the positions of the collector and emitter resistors are reversed compared to the *npn* transistor circuit. Also, note that the base voltage (V_B) in Fig. 5-29 is the voltage drop across resistor R_1, *not* that across R_2. As in the case of other circuits using *pnp* transistors, the current directions and voltage polarities are the reverse of those in *npn* transistor circuits. Apart from these differences, a *pnp* transistor voltage divider bias circuit is analysed in exactly the same way as an *npn* transistor circuit.

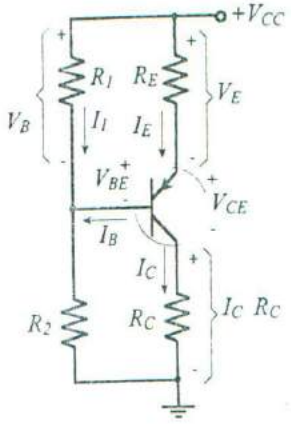


Figure 5-29
Voltage divider bias using a pnp transistor.

Practise Problems

5-4.1 A voltage divider bias circuit (as in Fig. 5-23) has V_{CC} = 24 V, R_1 = 180 kΩ, R_2 = 56 kΩ, R_E = 4.7 kΩ, R_C = 8.2 kΩ. Calculate the approximate levels of I_C, V_E, V_C, and V_{CE}.

5-4.2 The circuit in Practise Problem 5-4.1 uses a transistor with $h_{FE(min)}$ = 75 and $h_{FE(max)}$ = 250. Accurately analyse the circuit to determine the maximum and minimum levels of V_{CE}.

5-4.3 The voltage divider bias circuit in Fig. 5-29 has V_{CC} = 20 V, R_1 = 33 kΩ, R_2 = 100 kΩ, R_E = 3.9 kΩ, R_C = 6.8 kΩ. Calculate the approximate levels of V_E and V_C.

5-5 *Comparison of Basic Bias Circuits*

When comparing the performance of the three basic bias circuits, it must be recalled that transistor manufacturers specify maximum and minimum h_{FE} values for each transistor type number at various levels of collector current. Normally, the current gain of each individual transistor is not known, so that (as already stated) *the specified maximum and minimum values of h_{FE} must be used when analysing (or designing) a transistor bias circuit.* It is completely impractical to use some kind of average h_{FE} value.

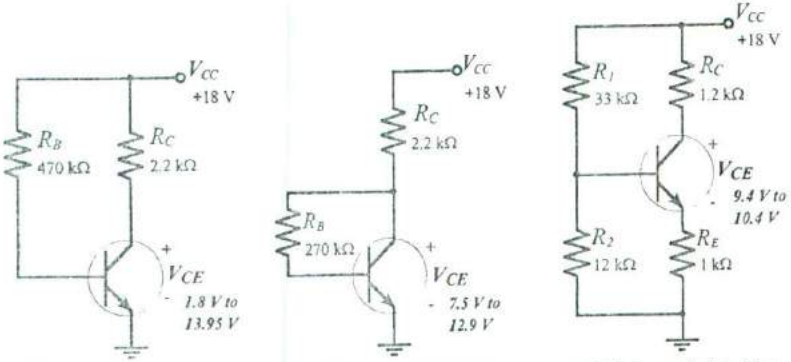


Figure 5-30
Comparison of similar base bias, collector-to-base bias, and voltage divider bias circuits.

Consider the three basic bias circuits reproduced in Fig. 5-30. Each circuit uses an 18 V supply and has a 2.2 kΩ (total) load resistance. The circuits were analysed in Examples 5-4, 5-6, 5-9, and 5-10 to determine the I_C and V_{CE} levels for $h_{FE(min)} = 50$ and $h_{FE(max)} = 200$. The calculated V_{CE} levels are indicated on each circuit and listed in Table 5-1. The Q point ranges are also illustrated in Fig. 5-31.

Table 5-1 *V_{CE} maximum and minimum levels for similar bias circuits.*

	Base bias	Collector-to-base bias	Voltage divider bias
$V_{CE(min)}$	1.8 V	7.25 V	9.4 V
$V_{CE(max)}$	13.75 V	12.9 V	10.4 V

To put these results in the most practical terms, suppose that a base bias circuit is employed as part of a complex electronics system, and that its V_{CE} level is measured as 10 V. If the transistor fails and has to be replaced with another (same type number) device with an h_{FE} range of 50 to 200, the new V_{CE} level could be anywhere from 1.8 V to 13.95 V. This would normally be unacceptable. A collector-to-base bias circuit in the same circumstance would have a V_{CE} ranging from 7.25 V to 12.9 V when the transistor is replaced. For a voltage divider bias circuit in this situation, the measurable V_{CE} range with a new transistor would be 9.4 V to 10.4 V.

Clearly, collector-to-base bias gives more predictable bias conditions than base bias. Voltage divider bias gives the most predictable bias conditions, because it has the greatest stability against h_{FE} spread.

Because of its excellent stability, voltage divider bias is almost always preferable. Collector-to-base bias, or some variation of it, is used in many circuits. Its one major advantage is that the feedback from the collector prevents the transistor from going into *saturation* (see Section 5-10). Base bias is most often used in switching circuits. This is also explained in Section 5-10.

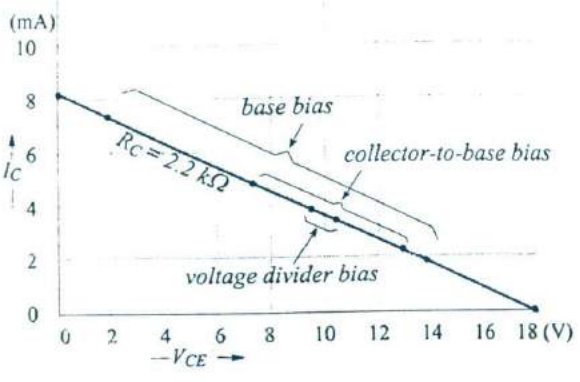


Figure 5-31
Q point ranges for the similar base bias, collector-to-base bias, and voltage divider bias circuits illustrated in Fig. 5-30.

5-6 Trouble-Shooting BJT Bias Circuits

Voltage Measurement

When a bias circuit is constructed in a laboratory situation, the supply voltage (V_{CC}) and the voltage levels at the transistor terminals (V_C, V_B, and V_E) should be measured with respect to the ground or negative supply terminal, as illustrated in Fig. 5-32. When the measured voltages are not as expected, the circuit must be further investigated to locate the fault.

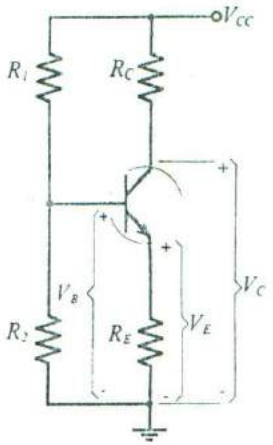


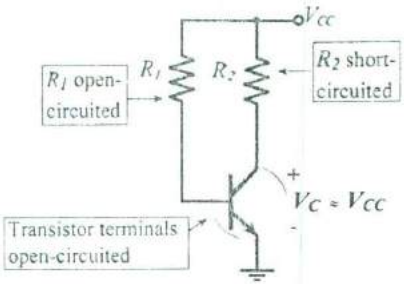
Figure 5-32
When testing a bias circuit, all voltage levels should first be measured with respect to the ground or negative supply terminal.

Common Errors

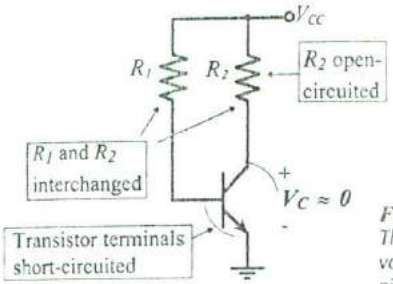
The following is a list of errors that commonly occur with both experienced and inexperienced individuals:

- Power supply not switched *on*.
- Power supply current limiter control incorrectly set.
- Cables incorrectly connected to the power supply.
- Volt-Ohm-Milliammeter (*VOM*) function incorrectly selected.
- Wrong *VOM* terminals used.
- Incorrect component connections.
- Incorrect resistor values.
- Resistors in the wrong places.

Obviously, it is important to correctly connect the cables to the power supply, and to switch the power supply *on*. However, with many things to think about, people often neglect basic items. Similarly, it is just too easy to connect the *VOM* cables to the wrong terminals, or to select the wrong function. With plug-in-type breadboards, the sockets are so small and close together that incorrect connections often occur. These items should all be checked before looking for other circuit faults. Care should also be taken when selecting resistors. For example, a 100 Ω resistor used instead of a 100 kΩ resistor can have serious consequences.



(a) Collector voltage equal to supply voltage



(b) Collector voltage equal to zero

Figure 5-33
The measured transistor terminal voltage on a base bias circuit can give an indication of possible circuit faults.

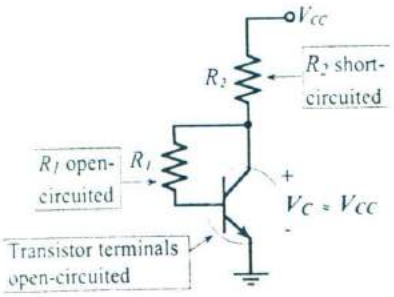
Base Bias

Figure 5-33 illustrates typical error sources in a base biased circuit. Normal voltage levels in a base bias circuit are $V_{BE} \approx 0.7$ V, and V_C anywhere in the range of 2 V to (V_{CC} - 2 V). If $V_C = V_{CC}$, as in Fig. 5-33(a), R_1 or one of its connecting leads might be open-circuited, or the transistor may have an open-circuited junction. Alternatively,

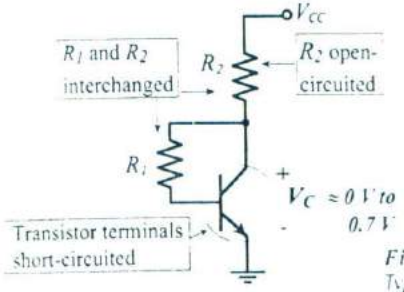
R_2 might be shorted. When $V_C \approx 0$, as in Fig. 5-33(b), R_1 and R_2 could be in the wrong places; that is, the high-value and low-value resistors might be interchanged. Other possibilities are that R_2 is open-circuited, or the transistor *CE* terminals are short-circuited.

Collector-to-Base Bias

Some reasons for incorrect voltage levels in a collector-to-base bias circuit are illustrated in Fig. 5-34. These are similar to those discussed for the base bias circuit. When V_C equals V_{CC}, either resistor R_1 or one of the transistor terminals is likely to be open-circuited, [Fig 5-34(a)]. If V_C is in the range of 0 V to 0.7 V, R_1 and R_2 might be interchanged, the device terminals might be short-circuited, or R_2 might be open-circuited, [Fig 5-34(b)].



(a) Collector voltage equal to supply voltage

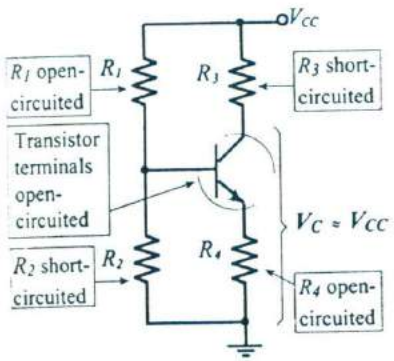


(b) Collector voltage equal to zero to 0.7 V

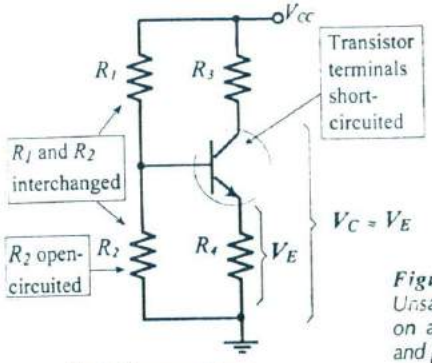
Figure 5-34
Typical incorrect terminal voltages in a collector-to-base bias circuit, and probable circuit faults.

Voltage Divider Bias

Figure 5-35 shows unsuitable measured voltages and probable errors in a voltage divider bias circuit. If V_C equals V_{CC}, either R_1 or R_4 might be open-circuited. Alternatively, R_2 or R_3 might be short-circuited, [Fig. 5-35(a)], or the transistor terminals might be open-circuited. When V_C approximately equals V_E, R_2 might be open-circuited, or R_1 and R_2 might be interchanged, [Fig. 5-35(b)]. Alternatively, the transistor terminals might be short-circuited.



(a) Collector voltage equal to supply voltage



(b) Collector voltage equal to emitter voltage

Figure 5-35
Unsatisfactory measured voltages on a voltage divider bias circuit, and probable circuit faults.

5-7 Bias Circuit Design

Bias circuit design can be amazingly simple. Usually, it is just a matter of determining the required voltage across each resistor and the appropriate current levels. Then, the resistor values are calculated by application of Ohm's law.

Designs usually begin with specification of the supply voltage and the required levels of I_C and V_{CE}. The resistor values are calculated to meet these requirements, and standard value resistors are selected. (See Appendix 2-1.) Usually, resistors with a tolerance of ±10% are used wherever possible. These are less expensive than ±5% and ±1% components.

Base Bias Circuit Design

A base bias circuit is very easily designed by application of Equations 5-1 and 5-2. This is illustrated in Fig. 5-36 and demonstrated in Example 5-11.

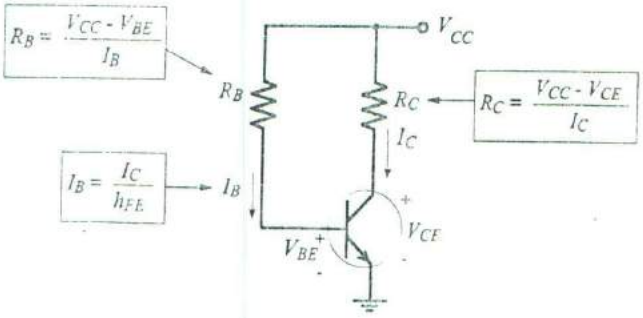


Figure 5-36
Base bias circuit design.

Example 5-11

Design a base bias circuit (as in Fig. 5-36) to have $V_{CE} = 5$ V and $I_C = 5$ mA. The supply voltage is 15 V, and the transistor has $h_{FE} = 100$.

Solution

From Eq. 5-1,

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{15\text{ V} - 5\text{ V}}{5\text{ mA}}$$

$$= 2\text{ k}\Omega \text{ (use 1.8 k}\Omega \text{ or 2.2 k}\Omega \text{ standard value)}$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{5\text{ mA}}{100}$$

$$= 50\,\mu\text{A}$$

From Eq. 5-2,

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15\text{ V} - 0.7\text{ V}}{50\,\mu\text{A}}$$

$$= 286\text{ k}\Omega \text{ (use 270 k}\Omega \text{ or 330 k}\Omega \text{ standard value)}$$

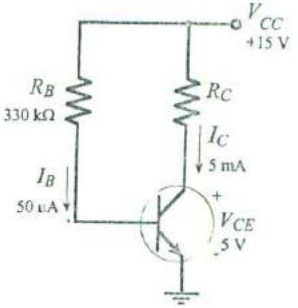


Figure 5-37
Base bias circuit designed in Example 5-11.

When selecting the standard value resistors, a decision must be made whether to select the next smaller resistance value or the next larger value. In general, it is best to select the resistance value that tends to increase the transistor collector-emitter voltage, thus keeping V_{CE} from approaching zero. In Example 5-11, selecting R_C = 1.8 kΩ (instead of 2.2 kΩ) gives the smallest voltage drop across R_C, and results in a larger V_{CE} than the (5 V) design value. Selecting R_B = 330 kΩ (instead of 270 kΩ) gives the lowest level of I_B, and consequently keeps I_C at a minimum, to produce the largest level of V_{CE}.

After design, the circuit should be analysed using the selected standard-value components and the maximum and minimum h_{FE} values for the transistor, (see Section 5-2).

Collector-to-Base Bias Circuit Design

The design procedure for a collector-to-base bias circuit is similar to that for base bias, with the exception that the voltage and current levels are different for calculating R_B and R_C. In collector-to-base bias, the voltage across R_B is $(V_C - V_{BE})$ and the current through R_C is $(I_B + I_C)$. The design equations are shown in Fig. 5-38, and the design procedure is demonstrated in Example 5-12.

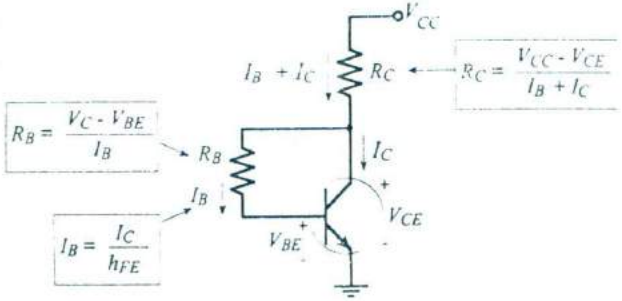


Figure 5-38
Collector-to-base bias circuit design.

Example 5-12

Design a collector-to-base bias circuit (as in Fig. 5-38) to have V_{CE} = 5 V and I_C = 5 mA when the supply voltage is 15 V and the transistor h_{fe} is 100.

Solution

$$I_B = \frac{I_C}{h_{fe}} = \frac{5\text{ mA}}{100}$$

$$= 50\,\mu\text{A}$$

From Eq. 5-5,

$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B} = \frac{15\text{ V} - 5\text{ V}}{5\text{ mA} + 50\,\mu\text{A}}$$

$$= 1.98\text{ k}\Omega\text{ (use 1.8 k}\Omega\text{ or 2.2 k}\Omega\text{ standard value)}$$

From Eq. 5-4,

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{5\text{ V} - 0.7\text{ V}}{50\,\mu\text{A}}$$

$$= 86\text{ k}\Omega \text{ (use 82 k}\Omega \text{ or 100 k}\Omega \text{ standard value)}$$

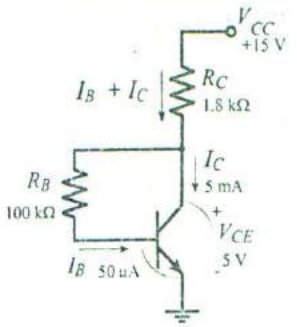


Figure 5-39
Collector-to-base bias circuit designed in Example 5-12.

Once again decisions must be made (in Example 5-12) about selecting the next larger or the next smaller standard value resistors. As in the case of the base bias circuit in Example 5-11, selection of the smaller value for R_C and the larger value for R_B tends to produce a larger V_{CE} than the specified level. The design should be analysed using the selected standard-value components and the transistor $h_{FE(max)}$ and $h_{FE(min)}$ values.

Voltage Divider Bias Circuit Design

When designing a voltage divider bias circuit the voltage divider current (I_2 in Fig. 5-40) should be selected much larger than the transistor base current (I_B). This makes the base voltage (V_B) a stable quantity largely unaffected by the transistor h_{FE} value. However, a high level of I_2 results in small resistance values for R_1 and R_2, and (as explained in Chapter 12) this gives the circuit an undesirable low input impedance.

A rule-of-thumb approach to selection of I_2 is to use a voltage divider current approximately equal to one-tenth of the transistor collector current.

$$I_2 = \frac{I_C}{10} \qquad \textbf{(5-16)}$$

As can be easily demonstrated, this gives reasonably large values for R_1 and R_2 while still keeping I_2 much larger than I_B.

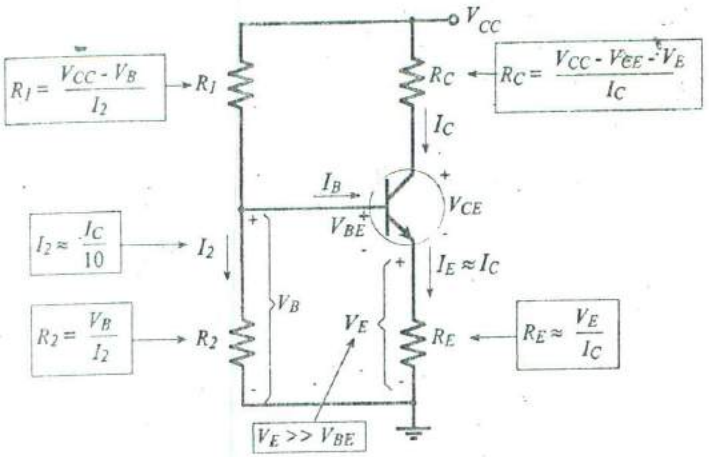


Figure 5-40
Voltage divider bias circuit design.

If V_E is not specified, it should be selected much larger than the transistor V_{BE}.

$$V_E >> V_{BE}$$

This is because V_{BE} can vary from transistor to transistor, and it can also change with temperature increase or decrease. Making V_E very much larger than V_{BE} minimises the effect of V_{BE} changes on the circuit bias conditions. Typically, as another rule-of-thumb, V_E is selected as 5 V regardless of the supply voltage. When V_{CC} is low (for example, 9 V), V_E can be as low as 3 V.

Figure 5-40 shows the equations used for calculating each resistor value, and Example 5-13 demonstrates the design procedure.

Example 5-13

Design the voltage divider bias circuit in Fig. 5-41 to have $V_{CE} = V_E = 5$ V and $I_C = 5$ mA when the supply voltage is 15 V. Assume the transistor h_{FE} is 100.

Solution

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{5\text{ V}}{5\text{ mA}}$$

$$= 1\text{ k}\Omega \text{ (standard value)}$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{15\text{ V} - 5\text{ V} - 5\text{ V}}{5\text{ mA}}$$

$$= 1\text{ k}\Omega \text{ (standard value)}$$

Eq. 5-16, $$I_2 = \frac{I_C}{10} = \frac{5\text{ mA}}{10}$$

$$= 500\,\mu\text{A}$$

From Eq. 5-8, $$V_B = V_E + V_{BE} = 5\text{ V} + 0.7\text{ V}$$

$$= 5.7\text{ V}$$

$$R_2 = \frac{V_B}{I_2} = \frac{5.7\text{ V}}{500\,\mu\text{A}}$$

$$= 11.4\text{ k}\Omega \text{ (use 12 k}\Omega \text{ standard value)}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{15\text{ V} - 5.7\text{ V}}{500\,\mu\text{A}}$$

$$= 18.6\text{ k}\Omega \text{ (use 18 k}\Omega \text{ standard value)}$$

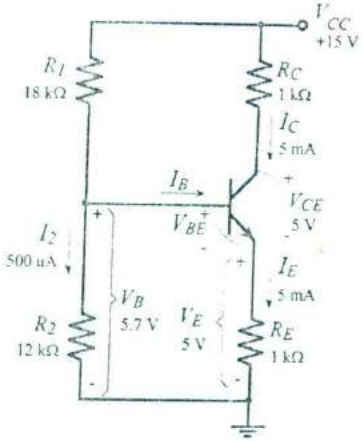


Figure 5-41
Voltage divider bias circuit designed in Example 5-13.

The calculated resistor values in Example 5-13 are conveniently close to standard values. When this is not the case, some thought must be put into deciding whether to select higher or lower standard value. As explained for the other bias circuits, it is best to select the resistance value that tend to increase the transistor

collector-emitter voltage, in order to keep V_{CE} from approaching zero. As with all bias circuit designs, the designed circuit should be analysed using the standard value components and the transistor $h_{FE(max)}$ and $h_{FE(min)}$ values.

Designing with Standard Resistor Values

In all circuit designs a suitable standard resistor should normally be selected when each resistor value is calculated, instead of first completing the design. Then, the new resistor voltage drop or current level should be determined before calculating the next component value. This is demonstrated in Example 5-14.

Example 5-14

Design the voltage divider bias circuit in Fig. 5-42 to operate from a 12 V supply. The bias conditions are to be $V_{CE} = 3$ V, $V_E = 5$ V and $I_C = 1$ mA.

Solution

$$R_4 = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{5\text{ V}}{1\text{ mA}}$$

$= 5\text{ k}\Omega$ (use a 4.7 kΩ standard value)

With $I_C = 1$ mA and $R_4 = 4.7$ kΩ, V_E becomes,

$$V_E = I_C R_4 = 1\text{ mA} \times 4.7\text{ k}\Omega$$

$= 4.7$ V

and,

$$V_C = V_E + V_{CE} = 4.7\text{ V} + 3\text{ V}$$

$= 7.7$ V

$$V_{R3} = V_{CC} - V_C = 12\text{ V} - 7.7\text{ V}$$

$= 4.3$ V

$$R_3 = \frac{V_{R3}}{I_C} = \frac{4.3\text{ V}}{1\text{ mA}}$$

$= 4.3\text{ k}\Omega$ (use a 3.9 kΩ standard value to reduce V_{R3} and increase V_{CE}.)

$$V_B = V_E + V_{BE} = 4.7\text{ V} + 0.7\text{ V}$$

$= 5.4$ V

Eq. 5-16,

$$I_2 = \frac{I_C}{10} = \frac{1\text{ mA}}{10}$$

$= 100\ \mu\text{A}$

$$R_2 = \frac{V_B}{I_2} = \frac{5.4\text{ V}}{100\ \mu\text{A}}$$

$= 54\text{ k}\Omega$ (use 56 kΩ standard value)

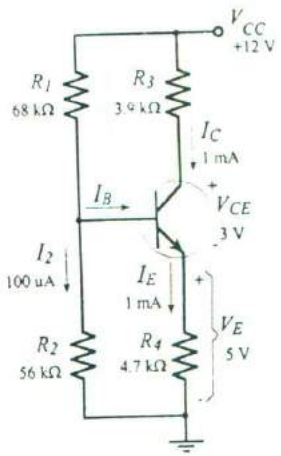


Figure 5-42
Voltage divider bias circuit for Example 5-14.

With $R_2 = 56\ \text{k}\Omega$ and $V_B = 5.4\ \text{V}$, I_2 becomes,

$$I_2 = \frac{V_B}{R_2} = \frac{5.4\ \text{V}}{56\ \text{k}\Omega}$$
$$= 96.4\ \mu\text{A}$$
$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{12\ \text{V} - 5.4\ \text{V}}{96.4\ \mu\text{A}}$$
$$= 68.5\ \text{k}\Omega \text{ (use 68 k}\Omega \text{ standard value)}$$

Practise Problems

5-7.1 A base bias circuit is to be designed to have $V_{CE} = 4$ V and $I_C = 3$ mA. The supply voltage is 12 V and the transistor h_{fe} is 125.

5-7.2 Design a collector-to-base bias circuit to have $V_{CE} = 4$ V and $I_C = 2$ mA. The supply voltage is 18 V and the transistor h_{fe} is 90.

5-7.3 Design a voltage divider bias circuit to have $V_{CE} = V_E = 6$ V and $I_C = 1.5$ mA. The supply voltage is 24 V and the transistor h_{fe} is 80.

5-7.4 Design a voltage divider bias circuit to have $V_{CE} = 7$ V, $V_E = 6$ V and $I_C = 2$ mA. The supply voltage is 20 V.

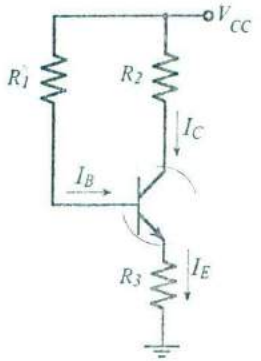


Figure 5-43
A base bias circuit with an emitter resistor has essentially the same stability as a similar base bias circuit.

5-8 More Bias Circuits

Base Bias with Emitter Resistor

The bias circuit shown in Fig. 5-43 is the usual base bias arrangement with the addition of an emitter resistor. Analysis reveals that this circuit has essentially the same stability characteristics as a similar base bias circuit. The only advantage of the emitter resistor in this case is that it gives the circuit a higher *input resistance* (see Section 6-5). An emitter resistor could also be employed with collector-to-base bias, and this would also produce a higher input resistance without significantly altering the circuit stability.

Voltage Divider and Collector-to-Base Combination

Figure 5-44 shows a voltage divider bias circuit with resistor R_1 connected to the transistor collector instead of to the supply. Thus, the circuit combines collector-to-base bias with voltage divider bias. An analysis of the circuit shows that this combination produces even greater bias stability than voltage divider bias alone.

The design procedure for this circuit is similar to voltage divider bias design, except that for calculating the resistances of R_1 and R_3, the voltage across R_1 is $(V_C - V_B)$ instead of $(V_{CC} - V_B)$, and the current through R_3 is $(I_C + I_2)$.

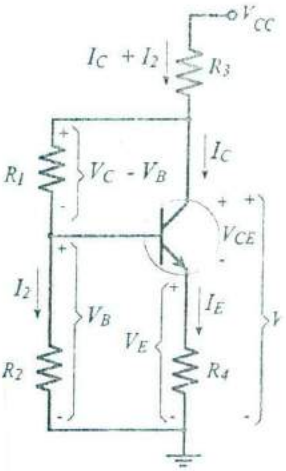


Figure 5-44
A combination of voltage divider bias and collector-to-base bias has excellent stability.

Example 5-15

Design the bias circuit in Fig. 5-44 to operate from an 18 V supply. The bias conditions are to be $V_{CE} = 9$ V, $V_E = 4$ V and $I_C = 4$ mA.

Solution

$$R_4 = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{4\text{ V}}{4\text{ mA}}$$
$$= 1\text{ k}\Omega \text{ (standard value)}$$

$$V_B = V_E + V_{BE} = 4\text{ V} + 0.7\text{ V}$$
$$= 4.7\text{ V}$$

Eq. 5-16, $$I_2 = \frac{I_C}{10} = \frac{4\text{ mA}}{10}$$
$$= 400\,\mu\text{A}$$

$$R_2 = \frac{V_B}{I_2} = \frac{4.7\text{ V}}{400\,\mu\text{A}}$$
$$= 11.8\text{ k}\Omega \text{ (use 12 k}\Omega \text{ standard value)}$$

With $R_2 = 12$ kΩ, I_2 becomes,

$$I_2 = \frac{V_B}{R_2} = \frac{4.7\text{ V}}{12\text{ k}\Omega}$$
$$= 392\,\mu\text{A}$$

$$R_1 = \frac{V_C - V_B}{I_2} = \frac{(9\text{ V} + 4\text{ V}) - 4.7\text{ V}}{392\,\mu\text{A}}$$
$$= 21.2\text{ k}\Omega \text{ (use 22 k}\Omega \text{ standard value)}$$

$$V_{R3} = V_{CC} - V_C = 18\text{ V} - (9\text{ V} + 4\text{ V})$$
$$= 5\text{ V}$$

$$R_3 = \frac{V_{R3}}{I_C + I_2} = \frac{5\text{ V}}{4\text{ mA} + 392\,\mu\text{A}}$$
$$= 1.14\text{ k}\Omega \text{ (use a 1.2 k}\Omega \text{ standard value)}$$

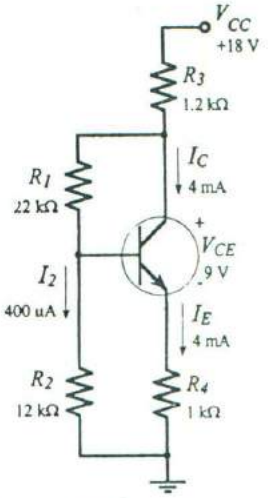


Figure 5-45
Circuit designed in Example 5-15.

Emitter Current Bias

The *emitter current bias* circuit in Fig. 5-46(a) uses a *plus and minus* voltage supply ($+V_{CC}$ and $-V_{EE}$) and has the transistor base grounded via resistor R_1. This is similar to voltage divider bias, in fact, as illustrated in Fig. 5-46(b), a voltage divider (R_1 and R_2) could be used to provide V_B instead of grounding the base via R_1.

So long as there is very little voltage drop across base resistor R_1, in Fig. 5-46(a), this circuit (like voltage divider bias), has excellent bias stability. Normally, R_1 is selected to have a voltage drop much smaller than the transistor base-emitter voltage:

$$I_{B(max)} R_1 << V_{BE}$$

A reasonable rule-of-thumb to use is,

$$I_{B(max)} R_1 \approx \frac{V_{BE}}{10} \qquad (5\text{-}17)$$

This mean that the transistor base voltage can be treated as ground level, and the voltage at the emitter terminal is always V_{BE} below ground, [see Fig. 5-46(a)]. So, the voltage across R_E is a constant quantity:

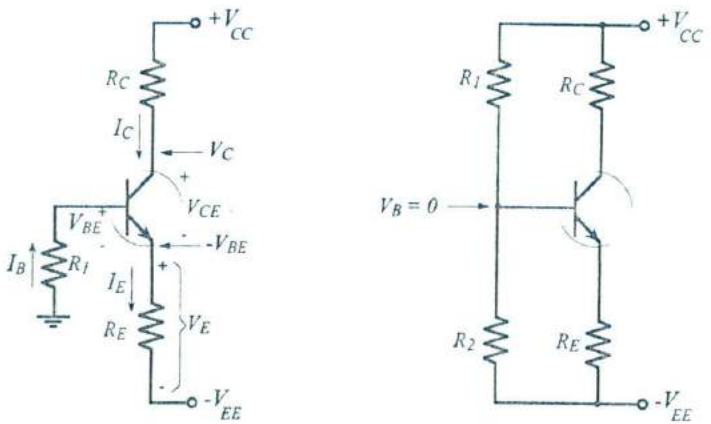
$$V_E = V_{EE} - V_{BE}$$

The transistor collector voltage is,

$$V_C = V_{CC} - V_{RC}$$

and, as illustrated, the collector-emitter voltage is,

$$V_{CE} = V_C + V_{BE}$$



(a) Emitter current bias circuit

(b) Voltage divider equivalent of emitter current bias circuit

Figure 5-46
Emitter current bias using a plus-minus supply voltage is similar to voltage divider bias.

Example 5-16

Design the bias circuit in Fig. 5-47(a) to operate from a ±9 V supply. The bias conditions are to be V_C = 5 V and I_C = 1 mA, and the transistor has h_{fE} = 70

Solution

$$V_E = V_{EE} - V_{BE} = 9\text{ V} - 0.7\text{ V}$$
$$= 8.3\text{ V}$$

$$R_3 = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{8.3\text{ V}}{1\text{ mA}}$$
$$= 8.3\text{ k}\Omega \text{ (use } 8.2\text{ k}\Omega \text{ standard value)}$$

New level of I_E,

$$I_E = \frac{V_E}{R_3} = \frac{8.3\text{ V}}{8.2\text{ k}\Omega}$$
$$= 1.01\text{ mA}$$

$$V_{R2} = V_{CC} - V_C = 9\text{ V} - 5\text{ V}$$
$$= 4\text{ V}$$

$$R_2 = \frac{V_{R2}}{I_C} \approx \frac{V_{R2}}{I_E} = \frac{4\text{ V}}{1.01\text{ mA}}$$
$$= 3.96\text{ k}\Omega \text{ (use } 3.9\text{ k}\Omega \text{ standard value)}$$

$$I_B = \frac{I_C}{h_{fE}} = \frac{1\text{ mA}}{70}$$
$$= 14.3\,\mu\text{A}$$

$$V_{R1} \approx \frac{V_{BE}}{10} = \frac{0.7\text{ V}}{10}$$
$$= 70\text{ mV}$$

$$R_1 = \frac{V_{R1}}{I_B} \approx \frac{70\text{ mV}}{14.3\,\mu\text{A}}$$
$$= 4.9\text{ k}\Omega \text{ (use } 4.7\text{ k}\Omega \text{ standard value)}$$

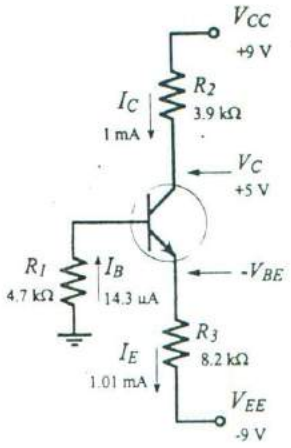


Figure 5-47
Emitter current bias circuit designed in Example 5-16.

The circuit in Fig. 5-47 can be quickly analysed almost by just looking at it. The transistor emitter terminal is 0.7 V below ground, and the voltage across R_E is,

$$V_E = 9\text{ V} - 0.7\text{ V} = 8.3\text{ V}$$

This gives,

$$I_E \approx \frac{V_E}{R_E} = \frac{8.3\text{ V}}{8.2\text{ k}\Omega}$$
$$\approx 1\text{ mA}$$

and,

$$V_C = V_{CC} - V_{RC} = 9\text{ V} - (1\text{ mA} \times 4.7\text{ k}\Omega)$$
$$= 4.3\text{ V}$$

Note that, as in the case of voltage divider bias, the transistor h_{FE} value is not used in the approximate circuit analysis. For accurate analysis, the same approach as used for voltage divider bias must be employed; the voltage source at the transistor base must be replaced with its Thevenin equivalent circuit.

Practise Problems

5-8.1 Design the bias circuit in Fig. 5-43 to have $V_C = 4$ V, $V_E = 5$ V and $I_C = 1.5$ mA. The supply voltage is 18 V and the transistor h_{FE} is 70.

5-8.2 A bias circuit that combines voltage divider and cathode-to-base bias (as in Fig. 5-44) is to have $V_{CE} = 5$ V and $I_C = 2$ mA. Design the circuit using $V_{CC} = 15$ V.

5-8.3 Design an emitter current bias circuit [as in Fig. 5-46 (a)] to have $V_C = 6$ V and $I_C = 3$ mA. The supply voltage is ±10 V and the transistor h_{fE} is 120.

5-9 *Thermal Stability of Bias Circuits*

V_{BE} and I_{CBO} Variations

Many transistor circuits are required to operate over a wide temperature range. So, another aspect of bias circuit stability is *thermal stability*, or how stable I_C and V_{CE} remain when the circuit temperature changes.

Measures to deal with the effects of h_{FE} variations have already been discussed. These apply whether the different h_{FE} values are due to temperature changes or to h_{FE} differences from one transistor to another.

The base-emitter voltage (V_{BE}) and the collector-base reverse saturation current (I_{CBO}) are the two temperature-sensitive quantities that largely determine the thermal stability of a transistor circuit, [see Fig. 5-48(a)]. The base-emitter and collector-base *pn*-junctions have the temperature characteristics discussed in Section 1-6. For a silicon transistor, V_{BE} changes by approximately -1.8 mV/°C, and I_{CBO} approximately doubles for every 10°C rise in temperature. These effects are illustrated by the characteristics in Fig. 5-48(b) and (c).

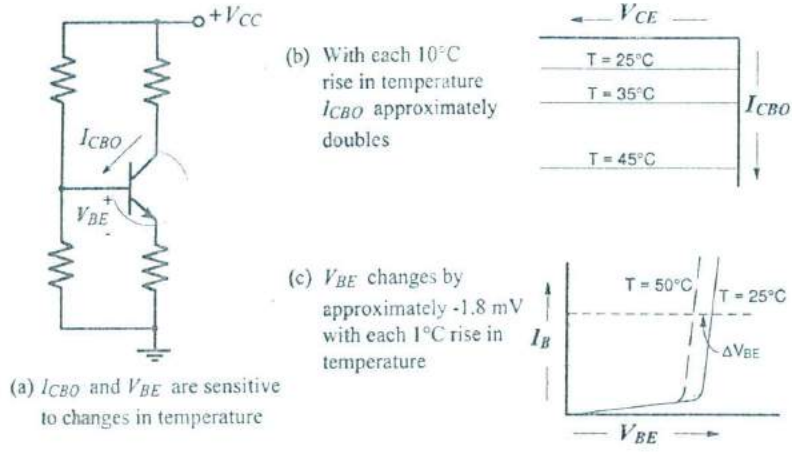


Figure 5-48
Transistor collector-base leakage current (I_{CBO}) and base-emitter voltage (V_{BE}) can be seriously affected by temperature change.

An increase in I_{CBO} causes I_C to be larger, and the I_C increase raises the collector-base junction temperature. This, in turn, results in a further increase in I_{CBO}. The effect is cumulative, so that the end result might be a substantial collector current increase. This could produce a significant shift in the circuit Q-point, or in the worst case, I_C *might keep on increasing until the transistor collector-base junction overheats and burns out.* This effect is known as *thermal runaway*. Measures taken to avoid thermal runaway are similar to those required for good bias stability against h_{FE} spread.

Changes in V_{BE} may also produce significant changes in I_C and consequently in the circuit Q-point. However, because of the possibility of thermal runaway, I_{CBO} changes are the most important. The thermal stability of a bias circuit is assessed by calculating a stability factor.

Stability Factor

The *stability factor* (S) of a circuit is the ratio of the change in collector current to the change in collector-base leakage current.

$$S = \frac{\Delta I_C}{\Delta I_{CBO}}$$

or,
$$\Delta I_C = S \times \Delta I_{CBO} \qquad (5\text{-}18)$$

The value of S depends on the circuit configuration and on the resistor values. The minimum values of S is 1. This means that if I_{CBO} increases by 1 μA I_C will increase by 1 μA. If a circuit has an S of 50, then $\Delta I_C = 50 \times \Delta I_{CBO}$. A stability factor of 50 (or larger) is considered poor, while a factor of 10 or less is considered good.

An equation for the stability factor of a bias circuit can be derived by writing an equation for the circuit I_C and investigating the effect of I_{CBO} change. The stability factors for the three basic bias circuit types (reproduced in Fig. 5-49) can be shown to be:

For base bias,

$$S = 1 + h_{FE} \qquad (5\text{-}19)$$

For collector-to-base bias,

$$S = \frac{1 + h_{FE}}{1 + h_{FE} R_C/(R_C + R_B)} \qquad (5\text{-}20)$$

For voltage divider bias,

$$S = \frac{1 + h_{FE}}{1 + h_{FE} R_E/(R_E + R_1||R_2)} \qquad (5\text{-}21)$$

The change in I_{CBO} over a given temperature range can be calculated by recalling that I_{CBO} doubles for every 10°C increase in temperature. The temperature change (ΔT) is divided by 10 to give the number of 10°C changes (n). If the starting level of collector-base leakage current is $I_{CBO(1)}$, the new level is,

$$I_{CBO(2)} = I_{CBO(1)} \times 2^n \qquad (5\text{-}22)$$

The I_{CBO} change and the circuit stability factor can be used to determine the change in I_C. (Eq. 5-18). Then the resulting V_{CE} change can be investigated.

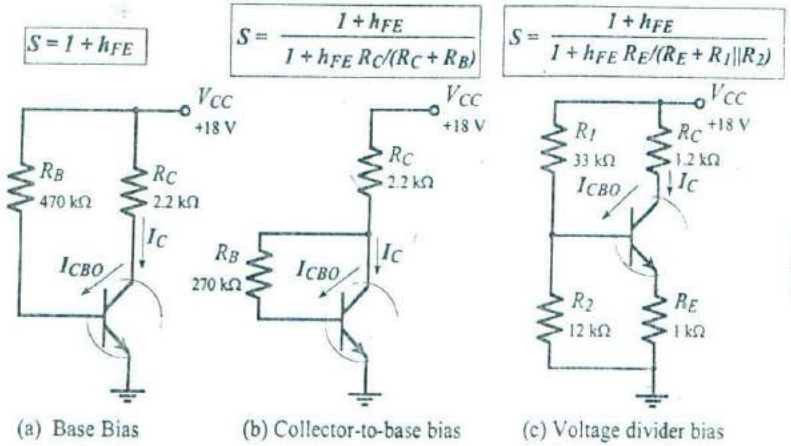


Figure 5-49
Stability factor equations for the three basic bias circuits.

Example 5-17

Calculate the stability factors for the three bias circuits shown in Fig. 5-49, if each circuit uses a transistor with $h_{FE} = 100$. Note that these are the bias circuits analysed in Examples 5-4, 5-6, and 5-8.

Solution

For base bias,

Eq. 5-19, $$S = 1 + h_{FE} = 1 + 100$$
$$= 101$$

For collector-to-base bias,

Eq. 5-20, $$S = \frac{1 + h_{FE}}{1 + h_{FE} R_C/(R_C + R_B)}$$
$$= \frac{1 + 100}{1 + [100 \times 2.2\ \text{k}\Omega/(2.2\ \text{k}\Omega + 270\ \text{k}\Omega)]}$$
$$\approx 56$$

For voltage divider bias,

Eq. 5-21, $$S = \frac{1 + h_{FE}}{1 + h_{FE} R_E/(R_E + R_1 \| R_2)}$$
$$= \frac{1 + 100}{1 + [100 \times 1\ \text{k}\Omega/(1\ \text{k}\Omega + 33\ \text{k}\Omega \| 12\ \text{k}\Omega)]}$$
$$= 8.2$$

Example 5-18

Determine the I_C change produced in each bias circuit referred to in Example 5-17 when the circuit temperature increases from 25°C to 105°C, and I_{CBO} = 15 nA at 25°C. The circuits are reproduced in Fig. 5-50.

Solution

$$\Delta T = 105°C - 25°C$$
$$= 80°C$$

or, ΔT in 10°C steps $= \dfrac{80°C}{10°C}$
$$= 8$$

Eq. 5-22, $I_{CBO(2)} = I_{CBO(1)} \times 2^n = 15\ nA \times 2^8$
$$= 3.84\ \mu A$$

$$\Delta I_{CBO} = I_{CBO(2)} - I_{CBO(1)} = 3.84\ \mu A - 15\ nA$$
$$\approx 3.83\ \mu A$$

For base bias,

Eq. 5-18, $\Delta I_C = S \times \Delta I_{CBO} = 101 \times 3.83\ \mu A$
$$\approx 386\ \mu A$$

For collector-to-base bias,

Eq. 5-18, $\Delta I_C = S \times \Delta I_{CBO} = 56 \times 3.83\ \mu A$
$$= 214\ \mu A$$

For voltage divider bias,

Eq. 5-18, $\Delta I_C = S \times \Delta I_{CBO} = 8.2 \times 3.83\ \mu A$
$$= 31.4\ \mu A$$

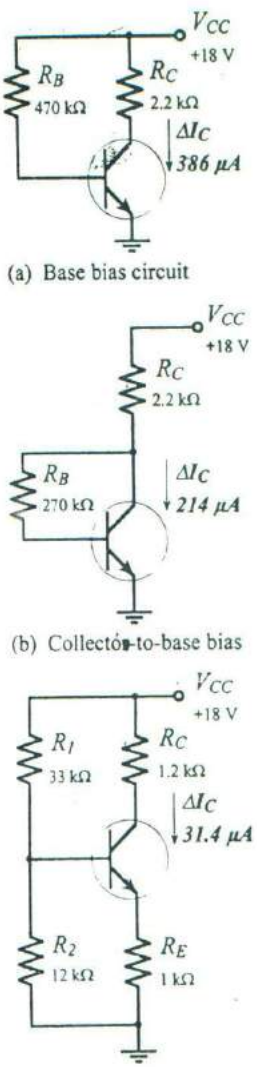


Figure 5-50
Effect of temperature change from 25°C to 105°C on bias circuits, as determined in Example 5-18.

The collector current changes produced by the increase in I_{CBO} (as calculated in Examples 5-17 and 5-18) are small compared to the effects of transistor h_{FE} spread. However, many transistors have higher levels of I_{CBO} (at 25°C) than the 15 nA used in Example 5-18, (some have lower levels). It is important to note that the bias circuit that offers the best thermal stability is also the one that gives the best stability against h_{FE} spread — voltage divider bias.

Effect of V_{BE} Changes

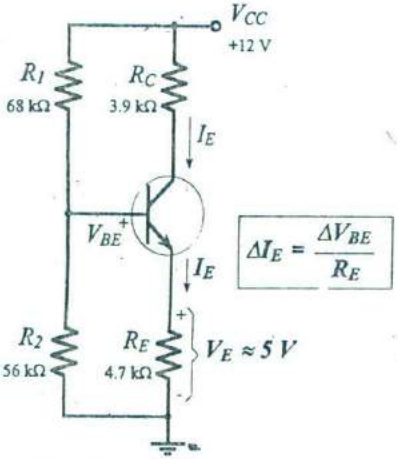
Consider the voltage divider bias circuits in Fig. 5-51(a) and (b), which each have V_{CC} = 12 V and I_C = 1 mA. From Eq. 5-9,

$$I_C \approx I_E = \frac{V_B - V_{BE}}{R_E}$$

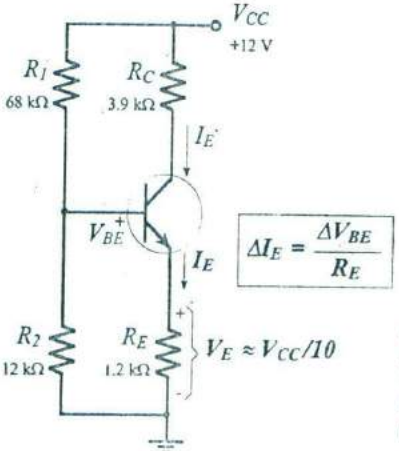
Assuming that V_B remains substantially constant, an equation for I_C change with V_{BE} change can be written:

$$\Delta I_C \approx \Delta I_E = \frac{\Delta V_{BE}}{R_E} \qquad \textbf{(5-23)}$$

As discussed in Section 5-7, the emitter resistor voltage should typically be selected as 5 V, ($V_E >> V_{BE}$). This is to ensure that I_C is not significantly affected by changes in V_{BE}. Thus, the circuit in Fig. 5-51(a) (with $V_E \approx 5$ V) has greater stability against V_{BE} changes than the one in Fig. 5-51(b) which was designed for $V_E = V_{CC}/10$, ($V_E = 1.2$ V). This is demonstrated in Example 5-19.



(a) Circuit designed for $V_E \approx 5$ V



(b) Circuit designed for $V_E \approx V_{CC}/10$

Figure 5-51
A voltage divider bias circuit with $V_E \approx 5$ V is less affected by temperature change than one with $V_E \approx 1$ V.

Example 5-19

Determine the I_C change produced in each of the two circuits in Fig. 5-51 by the effect of V_{BE} changes over a temperature range of 25°C to 125°C.

Solution

$$\Delta T = 125°C - 25°C$$
$$= 100°C$$

$$\Delta V_{BE} = \Delta T \times (1.8\ mV/°C) = 100°C \times 1.8\ mV$$
$$= 180\ mV$$

For Fig. 5-51 (a),

$$\Delta I_C \approx \Delta I_E = \frac{\Delta V_{BE}}{R_E} = \frac{180\ mV}{4.7\ k\Omega}$$
$$= 38\ \mu A$$

For Fig. 5-51 (b),

$$\Delta I_C \approx \Delta I_E = \frac{\Delta V_{BE}}{R_E} = \frac{180\ mV}{1.2\ k\Omega}$$
$$= 150\ \mu A$$

Diode Compensation

The use of a diode to compensate for V_{BE} changes is illustrated in Fig. 5-52. In this case,

$$V_B = V_{R2} + V_{D1}$$

and,

$$I_C \approx I_E = \frac{V_{R2} + V_{D1} - V_{BE}}{R_E} \qquad \textbf{(5-24)}$$

When V_{BE} changes by ΔV_{BE}, the diode voltage changes by an approximately equal amount (ΔV_{D1}). ΔV_{BE} and ΔV_{D1} tend to cancel each other, leaving I_C largely constant at,

$$I_C \approx I_E = \frac{V_{R2}}{R_E}$$

Base bias and collector-to-base bias are less affected by V_{BE} changes than voltage divider bias. This can easily be demonstrated by considering the equations for the base current in each case.

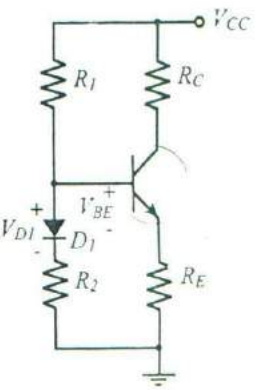


Figure 5-52
A diode can be used to compensate for V_{BE} changes in a voltage divider bias circuit.

Practise Problems

5-9.1 Calculate the stability factor for the bias circuits designed in Practise Problems 5-7.1, 5-7.2, and 5-7.3.

5-9.2 The circuit temperature of each of the bias circuits in Practise Problem 5-9.1 increases from 25°C to 125°C. Calculate the collector current change in each circuit if the transistor I_{CBO} = 10 nA at 25°C.

5-9.3 Calculate the I_C change produced by ΔV_{BE} in the circuit designed in Example 5-14 when the temperature changes from -35°C to +100°C.

5-10 Biasing Transistor Switching Circuits

Direct-Coupled Switching Circuit

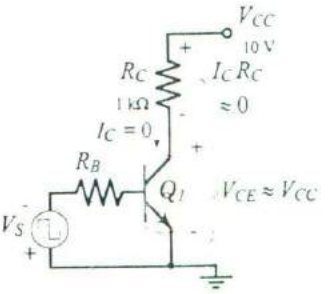
When a transistor is used as a switch, it is either biased *off* to I_C = 0, or biased *on* to its maximum collector current level. Figure 5-53 illustrates the two conditions. Note that the circuit in Fig. 5-53 is termed a *direct-coupled* switching circuit, because the signal source is directly connected to the circuit. In Fig. 5-53(a) the negative polarity of the base input voltage (V_S) biases the transistor (Q_1) *off*. In this case, the only current flowing is the collector base leakage current (I_{CBO}) which is normally so small that it can be neglected. The transistor collector-emitter voltage is,

$$V_{CE} = V_{CC} - (I_C R_C)$$

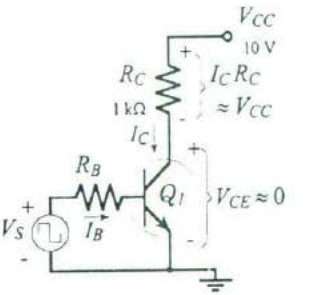
With Q_1 *off* [Fig. 5-53(a)],

$$V_{CE} \approx V_{CC}$$

In Fig. 5-53(b) V_S is positive, and it biases Q_1 on to the maximum possible I_C level. The collector current is limited only by the



(a) *OFF*-biased transistor



(b) *ON*-biased transistor

Figure 5-53
Direct-coupled transistor switching circuit. When V_B is zero or negative, $I_C = 0$ and $V_{CE} \approx V_{CC}$. When V_B is positive, I_B flows driving the transistor into saturation.

collector supply voltage (V_{CC}) and the collector resistor (R_C). So,

$$I_C R_C \approx V_{CC} \qquad \textbf{(5-25)}$$

and, $$V_{CE} = V_{CC} - (I_C R_C) \approx 0$$

Now consider Fig. 5-54, which shows the output characteristics and *dc* load line for the switching circuit in Fig. 5-53. The load line is drawn by the usual process of plotting point *A* at ($I_C = 0$ and $V_{CE} = V_{CC}$), and point *B* at ($V_{CE} = 0$ and $I_C = V_{CC}/R_C$), [see Section 5-1].

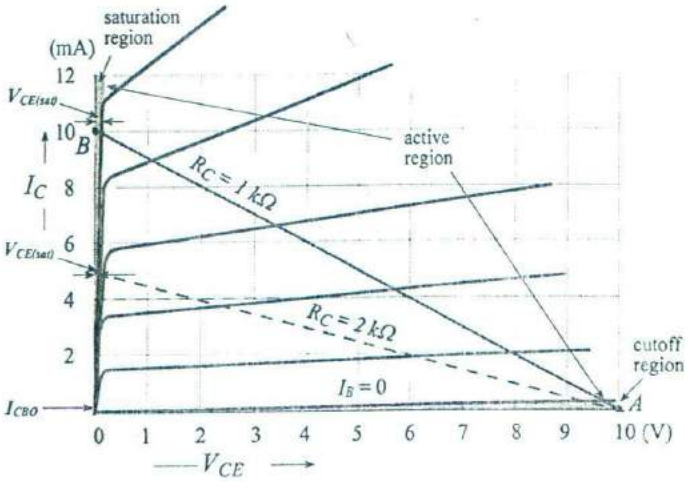


Figure 5-54
DC load line for a transistor switching circuit. When ON, the transistor is operating in the saturation region. When OFF, it is in the cutoff region.

The 1 kΩ load line shows that, when $I_B = 0$, I_C is close to zero at,

$$I_C = I_{CBO}$$

At this point the transistor is said to be *cut off*. The region of the characteristics below $I_B = 0$ is termed the *cutoff region*. When I_C is at its maximum level, the transistor is said to be *saturated*, and the collector-emitter voltage is the *saturation voltage* ($V_{CE(sat)}$).

$$V_{CE} = V_{CE(sat)}$$

The region of the transistor characteristics at $V_{CE(sat)}$ is termed the *saturation region*. The region between saturation and cutoff is the *active region*, which is where a transistor is normally biased for amplification. From the load line, it is seen that $V_{CE(sat)}$ is dependent upon the I_C level. For the 2 kΩ load line shown dashed in Fig. 5-54, $V_{CE(sat)}$ is smaller than for $R_C = 1$ kΩ.

Returning to Fig. 5-53(b), it is seen that I_B is a constant quantity,

$$I_B = \frac{V_S - V_{BE}}{R_B} \qquad \textbf{(5-26)}$$

Also, the level of I_C depends upon I_B.

$$I_C = h_{FE} \times I_B$$

The collector current can be determined from Eq. 5-25 (which assumes that $V_{CE(sat)} = 0$), and the base current can be calculated from Eq. 5-26. Then, the minimum required current gain for the transistor is,

$$h_{FE(1)} = \frac{I_C}{I_B} \qquad \textbf{(5-27)}$$

If the transistor h_{FE} value is less than the calculated $h_{FE(1)}$ value, I_C will be lower than the level required for transistor saturation. If the actual h_{FE} of the transistor is greater than the calculated $h_{FE(1)}$, I_C tends to be greater than the current level required to saturate the transistor. However, I_C cannot exceed V_{CC}/R_C. Consequently, an h_{FE} value larger than $h_{FE(1)}$ will adjust down to $h_{FE(1)}$. An h_{FE} value lower than $h_{FE(1)}$ cannot adjust up. So, to ensure that the transistor in a switching circuit saturates, it must have an h_{FE} value equal to or greater than the calculated $h_{FE(1)}$ for the circuit.

$V_{CE(sat)}$ is typically 0.2 V for a low-current silicon transistor, while V_{BE} is typically 0.7 V. Consider the circuit in Fig. 5-53(b) once again. If $V_{BE} = 0.7$ V and $V_{CE(sat)} = 0.2$ V, the transistor base is 0.5 V more positive than the collector,(see Fig. 5-55). This means that the collector-base junction, which is usually reverse biased, is forward biased when the transistor is in saturation. With the collector-base junction forward biased, fewer charge carriers from the emitter are drawn across to the collector, and the device current gain is lower than normal.

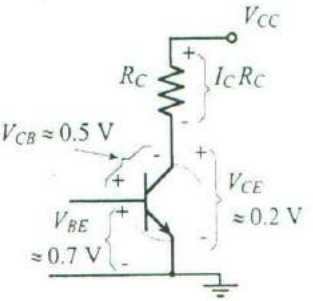


Figure 5-55
When a transistor is in saturation, the CB junction is forward biased.

Example 5-20

Calculate the minimum h_{fe} for the transistor in the circuit in Fig. 5-56 when $V_{CC} = 10$ V, $R_C = 1$ kΩ, $R_B = 6.8$ kΩ, and $V_S = 5$ V. Also, determine the transistor V_{CE} level when $h_{fe} = 10$.

Solution

$h_{FE(1)}$ calculation

From Eq. 5-25,

$$I_C \approx \frac{V_{CC}}{R_C} = \frac{10\text{ V}}{1\text{ k}\Omega}$$

$$= 10\text{ mA}$$

Eq. 5-26,

$$I_B = \frac{V_S - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{6.8\text{ k}\Omega}$$

$$= 632\ \mu\text{A}$$

Eq. 5-27,

$$h_{FE(1)} = \frac{I_C}{I_B} = \frac{10\text{ mA}}{632\ \mu\text{A}}$$

$$= 15.8$$

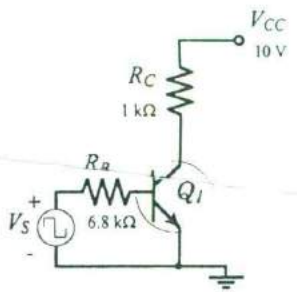


Figure 5-56
Direct-coupled switching circuit for Example 5-20.

When $h_{FE} = 10$,

$$I_C = h_{FE} I_B = 10 \times 632\ \mu A$$
$$= 6.32\ mA$$
$$V_{CE} = V_{CC} - (I_C R_C) = 10\ V - (6.32\ mA \times 1\ k\Omega)$$
$$= 3.68\ V$$

Capacitor-Coupled Switching Circuit

The base bias circuit in Fig. 5-57 is similar to circuits of that type that have already been considered, with the exception that the transistor is biased into saturation. Although too unpredictable for biasing amplifier circuits, base bias is quite satisfactory for switching circuits. The transistor in Fig. 5-57 is in a normally-*on* state with $V_{CE} = V_{CE(sat)}$. The *capacitor-coupled* (pulse waveform) input turns the device *off*, giving $V_{CE} = V_{CC}$.

The transistor base current is,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (5\text{-}28)$$

The collector current can be determined From Eq. 5-25, and then the minimum required h_{FE} value can be calculated from Eq. 5-27.

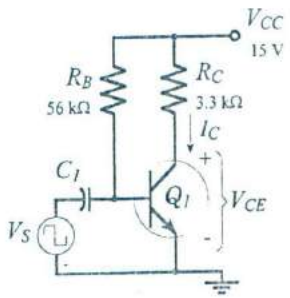


Figure 5-57
Capacitor-coupled switching circuit with the transistor biased ON into saturation.

Example 5-21

A new transistor is to be substituted in place of Q_1 in the circuit in Fig. 5-57. Calculate the minimum required h_{FE} for the transistor.

Solution

From Eq. 5-25,

$$I_C \approx \frac{V_{CC}}{R_C} = \frac{15\ V}{3.3\ k\Omega}$$
$$= 4.55\ mA$$

Eq. 5-28,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\ V - 0.7\ V}{56\ k\Omega}$$
$$= 255\ \mu A$$

Eq. 5-27,

$$h_{FE(1)} = \frac{I_C}{I_B} = \frac{4.55\ mA}{255\ \mu A}$$
$$= 17.8$$

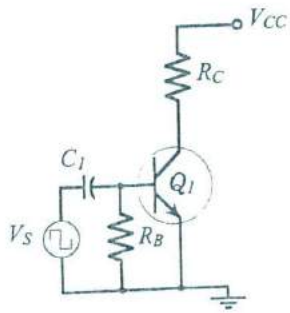


Figure 5-58
Capacitor-coupled switching circuit with the transistor biased OFF.

Another type of capacitor-coupled switching circuit is illustrated in Fig. 5-58. In this case, resistor R_B keeps the transistor base-emitter voltage at zero, to ensure that the device is in a normally-*off* state. The capacitor-coupled input voltage biases the transistor *on* into saturation.

Switching Circuit Design

The resistance of R_C for any one of the switching circuits discussed can be calculated by using the specified V_{CC} and I_C levels with Eq. 5-25. The transistor $h_{FE(min)}$ value can be used with I_C to determine the minimum I_B level required for transistor saturation. However, concern about the actual transistor current gain can be avoided by using an h_{FE} value of 10. It is very unlikely that the transistor will have an $h_{FE(min)}$ less than 10, so a circuit designed in this way will work with virtually any low-current transistor.

The resistance of R_B for the direct-coupled circuit in Fig. 5-53 is calculated from Eq. 5-26. For the normally-*on* capacitor-coupled circuit in Fig. 5-57, Eq. 5-28 is used for determining the R_B value.

A different approach must be taken for calculating a suitable resistance for R_B in the normally-*off* capacitor-coupled circuit in Fig. 5-58. The current that flows through R_B when the transistor is *off*, and the allowable voltage drop across R_B must be considered, (see Fig. 5-59). The resistor current is the collector-base leakage current (I_{CBO}), and the maximum voltage drop produced by I_{CBO} must be much smaller than the normal transistor V_{BE} level when the device is *on*. I_{CBO} at maximum transistor temperature is unlikely to exceed 5 μA, and a V_{RB} of 0.1 V will normally keep the transistor biased *off*. So, a maximum resistance value for R_B is,

$$R_B = \frac{0.1\text{ V}}{5\ \mu\text{A}} = 20\ \text{k}\Omega$$

Typically, an R_B value of 22 kΩ or lower is suitable for keeping the transistor biased *off*.

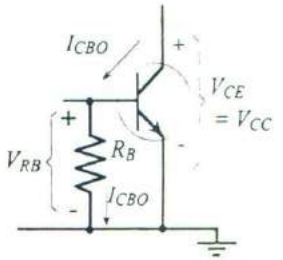


Figure 5-59
A voltage drop is produced across R_B by the collector-base leakage current (I_{CBO}).

Example 5-22

The circuit in Fig. 5-60 uses V_{CC} = 12 V, the collector current is to be approximately 1.5 mA, and V_S = +5 V. Determine suitable resistances for R_B and R_C.

Solution

From Eq. 5-25,

$$R_C \approx \frac{V_{CC}}{I_C} = \frac{12\text{ V}}{1.5\text{ mA}}$$

$$= 8\ \text{k}\Omega\ \text{(use 8.2 k}\Omega\ \text{standard value)}$$

From Eq. 5-27,

$$I_B = \frac{I_C}{h_{FE(min)}} = \frac{1.5\text{ mA}}{10}$$

$$= 150\ \mu\text{A}$$

From Eq. 5-26,

$$R_B = \frac{V_S - V_{BE}}{I_B} = \frac{5\text{ V} - 0.7\text{ V}}{150\ \mu\text{A}}$$

$$= 28.6\ \text{k}\Omega\ \text{(Use 27 k}\Omega\ \text{to ensure that } I_B \text{ is larger than required for saturation)}$$

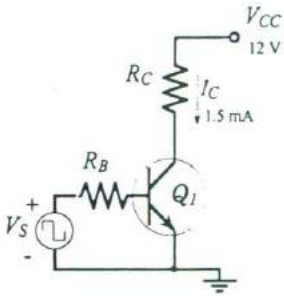


Figure 5-60
Direct-coupled switching circuit for Example 5-22.

Example 5-23

Determine suitable resistor values for the capacitor-coupled switching circuit in Fig. 5-61.

Solution

From Eq. 5-25,

$$R_C \approx \frac{V_{CC}}{I_C} = \frac{9\text{ V}}{2\text{ mA}}$$

$$= 4.5\text{ k}\Omega \text{ (use 4.7 k}\Omega \text{ standard value)}$$

From Eq. 5-27,

$$I_B = \frac{I_C}{h_{FE(min)}} = \frac{2\text{ mA}}{10}$$

$$= 200\,\mu\text{A}$$

From Eq. 5-28,

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{9\text{ V} - 0.7\text{ V}}{200\,\mu\text{A}}$$

$$= 41.5\text{ k}\Omega \text{ (Use 39 k}\Omega)$$

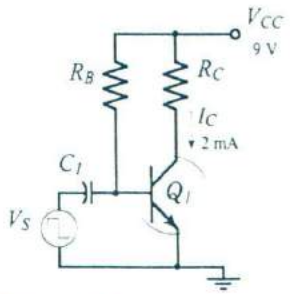


Figure 5-61
Capacitor-coupled switching circuit for Example 5-23.

Practise Problems

5-10.1 A direct-coupled transistor switching circuit as in Fig. 5-56 has V_{CC} = 15 V, V_S = 9 V, R_C = 3.3 kΩ, and R_B = 22 kΩ. Calculate the minimum h_{FE} for the transistor.

5-10.2 A normally-*on* capacitor-coupled switching circuit (as in Fig. 5-57) uses a transistor with $h_{FE(min)}$ = 25. The supply voltage is 12 V and R_C = 4.7 kΩ. Determine a suitable resistance for R_B.

5-10.3 A direct-coupled transistor switching circuit has V_{CC} = 5 V and V_S = 3 V. Calculate suitable resistances for R_C and R_B to give I_C = 2.5 mA.

Chapter-5 Review Questions

Section 5-1

5-1 Identify the components that constitute the *dc* load in a *BJT* bias circuit. Explain the procedure for drawing the *dc* load line on the transistor *CE* output characteristics.

5-2 Explain the selection of a *Q*-point for a transistor bias circuit, and discuss the limitations on the output voltage swing.

Section 5-2

5-3 Sketch a base bias circuit, (a) using an *npn* transistor, (b) using a *pnp* transistor. In each case show the polarity of V_{CC}, V_{BE}, and V_{CE}. Also, show the direction of I_C and I_B.

5-4 Explain the operation of the base bias circuits drawn for Question 5-3, and write equations for I_B, I_C, and V_{CE}.

Section 5-3

5-5 Sketch a collector-to-base bias circuit using an *npn* transistor. Show the polarity of V_{CC}, V_{BE}, and V_{CE}. Also, identify the direction of I_C and I_B.

5-6 Explain the operation of the collector-to-base bias circuit drawn for Question 5-5. Write equations for I_B, I_C, and V_{CE}.

5-7 Sketch a collector-to-base bias circuit that uses a *pnp* transistor. Show all voltage polarities and current directions, and discuss the circuit operation.

Section 5-4

5-8 Sketch a voltage divider bias circuit using an *npn* transistor. Show all voltage polarities and current directions.

5-9 Explain the operation of the voltage divider bias circuit drawn for Question 5-8, and write approximate equations for V_B, I_E, I_C, and V_{CE}.

5-10 Explain the procedure for precise analysis of a voltage divider bias circuit.

5-11 Sketch a voltage divider bias circuit using an *pnp* transistor. Show all voltage polarities and current directions, and discuss the circuit operation.

Section 5-5

5-12 Compare base bias, collector-to-base bias, and voltage divider bias with regard to stability of the transistor collector voltage with spread in h_{FE} value. Discuss the advantages and disadvantages of the three types of bias circuit.

Section 5-6

5-13 List common errors involved in constructing and testing a transistor bias circuit.

5-14 Suggest possible errors in a base bias circuit, (a) when $V_C \approx V_{CC}$, (b) when $V_C \approx 0$.

5-15 Suggest possible errors in a collector-to-base bias circuit, (a) when $V_C \approx V_{CC}$, (b) when $V_C \approx 0$.

5-16 Suggest possible errors in a voltage divider bias circuit, (a) when $V_C \approx V_{CC}$, (b) when $V_C \approx V_E$.

Section 5-7

5-17 Write the equations for calculating R_B and R_C for a base bias circuit.

5-18 Write equations for calculating R_B and R_C for a collector-to-base bias circuit.

5-19 For a voltage divider bias circuit, write equations for calculating R_E and R_C, and the voltage divider resistors.

Section 5-8

5-20 Sketch a base bias circuit that uses an emitter resistor with an *npn* transistor. Briefly discuss the circuit operation.

5-21 Sketch an *npn* transistor bias circuit that uses a combination of voltage divider bias and collector-to-base bias. Show all voltage polarities and current directions, and explain the circuit operation.

5-22 Repeat Question 5-21 for a circuit that uses a *pnp* transistor.

5-23 Sketch an emitter current bias circuit using a plus and minus supply. Explain the circuit operation and compare it to voltage divider bias.

Section 5-9

5-24 Discuss the thermal stability of transistor bias circuit with regard to I_{CBO} and V_{BE}. State approximations for the variation in V_{BE} and I_{CBO} with temperature changes.

5-25 Define the stability factor (S) for a transistor bias circuit. Compare the three basic bias circuits with regard to thermal stability.

5-26 Show how a voltage divider bias circuit may be compensated for V_{BE} changes with temperature. Derive an equation for I_C.

Section 5-10

5-27 Draw a direct-coupled transistor switching circuit that may be turned *on* or *off* by application of an input voltage. Explain the circuit operation.

5-28 Sketch the typical output characteristics and *dc* load line for a transistor used as a switch. Identify the regions of the characteristics and briefly explain.

5-29 Sketch the circuit of a capacitor-coupled transistor switch biased in, (a) a normally-*on* condition, (b) a normally-*off* condition. Explain the operation of each circuit.

Chapter-5 Problems

Section 5-1

5-1 Plot the *dc* load line for the transistor circuit in Fig. 5-62 on the output characteristics shown in Fig. 5-63, (a) with V_{CC} = 15 V and R_C = 7.5 kΩ, (b) with V_{CC} = 12 V and R_C = 8 kΩ. Specify the Q-point in each case if I_B = 20 μA.

5-2 A circuit with the configuration and characteristics in Figs 5-62 and 5-63 has V_{CC} = 10 V, R_C = 1.7 kΩ, and I_B = 10 μA. Draw the *dc* load line, and specify the circuit Q-point.

5-3 Determine the maximum symmetrical output voltage swing for each of the two circuits in Problem 5-1.

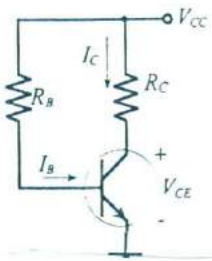


Figure 5-62
Circuit for Problem 5-1.

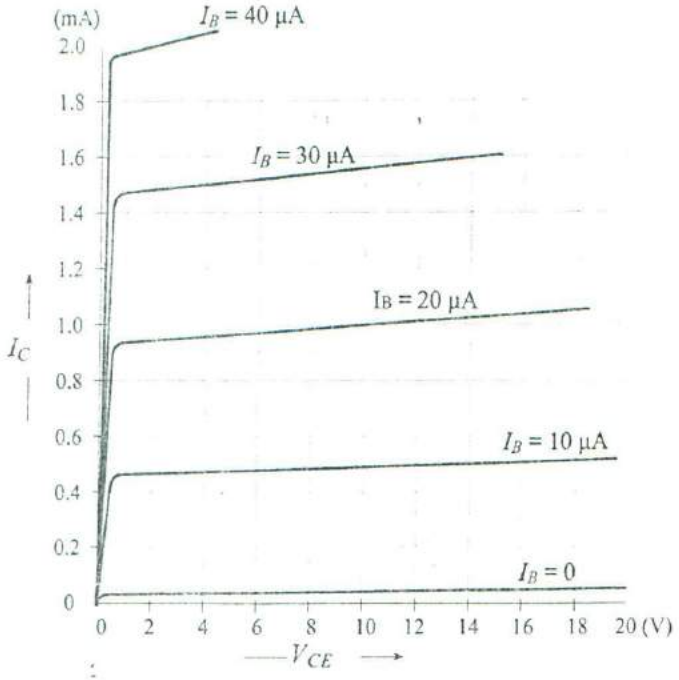


Figure 5-63
Transistor characteristics for Problem 5-1.

5-4 Determine the maximum symmetrical output voltage swing for the circuit in Problem 5-2.

5-5 Using the transistor characteristics in Fig. 5-63, draw the *dc* load line for the circuit in Fig. 5-64. Determine I_C for the circuit when $I_B = 10\ \mu A$, and calculate V_{RC}, V_{RE}, and V_{CE}.

5-6 A circuit with the characteristics in Fig. 5-10 has $V_{CC} = 7.5$ V, $R_C = 1.2\ k\Omega$, and $I_B = 40\ \mu A$. Draw the *dc* load line, specify the circuit *Q*-point, and determine the upper and lower limits of V_{CE}.

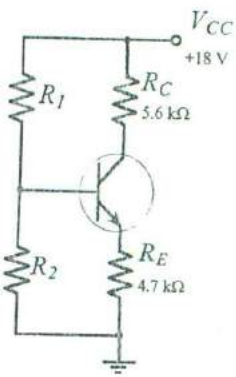


Figure 5-64
Circuit for Problem 5-5.

Section 5-2

5-7 A base bias circuit (as in Fig. 5-62) has $V_{CC} = 15$ V, $R_C = 1.8\ k\Omega$, and $R_B = 120\ k\Omega$. Assuming $V_{BE} = 0.7$ V and $h_{FE} = 50$, determine I_C and V_{CE}.

5-8 Determine the maximum and minimum I_C and V_{CE} levels for the circuit in Problem 5-7 when the transistor used has $h_{FE(max)} = 60$ and $h_{FE(min)} = 20$.

5-9 A base bias circuit has $V_{CC} = 20$ V, $R_C = 5.6\ k\Omega$, $R_B = 270\ k\Omega$, and $V_{CE} = 10$ V. Determine the transistor h_{FE} value, and calculate the new V_{CE} level when a transistor with $h_{FE} = 40$ is substituted.

5-10 A base bias circuit with $V_{CC} = 12$ V, $R_C = 3.9\ k\Omega$, and $R_B = 330\ k\Omega$ has a measured V_{CE} of 3 V. Determine the transistor h_{FE} value.

Section 5-3

5-11 A collector-to-base bias circuit (as in Fig. 5-65) has $V_{CC} = 15$ V, $R_C = 1.8$ kΩ, $R_B = 39$ kΩ, and $h_{FE} = 50$. Determine the I_C and V_{CE} levels.

5-12 Calculate the maximum and minimum levels of I_C and V_{CE} for the circuit in Problem 5-11 when the transistor used has $h_{FE(max)} = 60$ and $h_{FE(min)} = 20$.

5-13 A collector-to-base bias circuit has $V_{CC} = 15$ V, $R_C = 5.6$ kΩ, $R_B = 82$ kΩ, and $V_{CE} = 5$ V. Determine the transistor h_{FE} value, and calculate the new V_{CE} level when a transistor with $h_{FE} = 50$ is substituted.

5-14 Determine the new I_C and V_{CE} levels for the circuit in Problem 5-11 when the supply voltage is changed to 20 V.

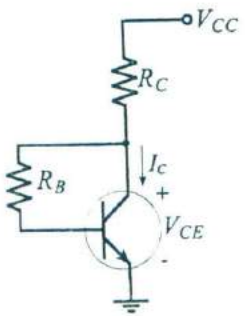


Figure 5-65
Circuit for Problem 5-11.

Section 5-4

5-15 The voltage divider bias circuit in Fig. 5-66, has $V_{CC} = 15$ V, $R_1 = 6.8$ kΩ, $R_2 = 3.3$ kΩ, $R_3 = 900$ Ω, $R_4 = 900$ Ω, and $h_{FE} = 50$. Analyze the circuit approximately to determine the levels of I_C and V_{CE}.

5-16 Precisely analyze the circuit in Problem 5-15 to determine the maximum and minimum levels of I_C and V_{CE} when $h_{FE(max)} = 60$ and $h_{FE(min)} = 20$.

5-17 A voltage divider bias circuit with a 25 V supply has $R_C = 4.7$ kΩ, $R_E = 3.3$ kΩ, $R_1 = 33$ kΩ, $R_2 = 12$ kΩ, and $h_{FE} = 50$. Use the approximate analysis method to calculate the V_{CE} level.

5-18 Precisely analyze the circuit in Problem 5-17 to determine the levels of I_C and V_{CE} when the transistor has $h_{FE} = 60$.

5-19 A transistor circuit using voltage divider bias has the following components: $R_C = 2.2$ kΩ, $R_E = 3.3$ kΩ, $R_1 = 6.8$ kΩ, $R_2 = 4.7$ kΩ. The supply voltage is $V_{CC} = 15$ V. Analyze the circuit approximately to determine V_{CE}.

5-20 A voltage divider bias circuit has $V_{CC} = 15$ V, $R_C = 2.7$ kΩ, $R_E = 2.2$ kΩ, $R_1 = 22$ kΩ, $R_2 = 12$ kΩ. Calculate the V_{CE} level.

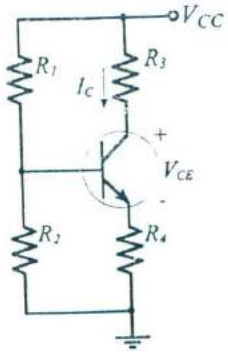


Figure 5-66
Circuit for Problem 5-15.

Section 5-5

5-21 Using the transistor characteristics in Fig. 5-10, plot the *dc* load line and maximum and minimum *Q*-points for the circuits in Problems 5-8, 5-12, 5-16.

Section 5-6

5-22 Analyze the circuit in Problem 5-7 to investigate the effect of interchanging the base and collector resistors.

5-23 Analyze the circuit in Problem 5-11 to investigate the effect of interchanging the base and collector resistors.

5-24 Analyze the circuit in Problem 5-15 to investigate the effect of interchanging the voltage divider resistors.

Section 5-7

5-25 A base bias circuit with V_{CC} = 18 V uses a transistor with the characteristics in Fig. 5-63. The circuit is to have V_{CE} = 9 V and I_C = 2 mA. Plot the Q-point, draw the *dc* load line, and determine the required resistance for R_C.

5-26 A base bias circuit with a 12 V supply uses a transistor with h_{FE} = 70. Design the circuit to have I_C = 2 mA and V_{CE} = 9 V.

5-27 Analyze the circuit designed for Problem 5-26 to determine the maximum and minimum levels of V_{CE} when the transistor type used has $h_{FE(min)}$ = 30 and $h_{FE(max)}$ = 200.

5-28 A base bias circuit has V_{CC} = 20 V, R_C = 6.8 kΩ, and the transistor h_{FE} = 120. Calculate the required base resistance value to give V_{CE} = 5 V.

5-29 Design a collector-to-base bias circuit to have I_C = 3.5 mA and V_{CE} = 12 V. The supply voltage is V_{CC} = 20 V, and the transistor h_{FE} = 80.

5-30 Analyze the circuit designed for Problem 5-29 to determine the maximum and minimum levels of V_{CE} when the transistor type used has $h_{FE(min)}$ = 20 and $h_{FE(max)}$ = 100.

5-31 A collector-to-base bias circuit is to have I_C = 3 mA and V_{CE} = 10 V. The supply voltage is V_{CC} = 25 V, and the transistor h_{FE} = 80. Calculate suitable resistor values.

5-32 A collector-to-base bias circuit has V_{CC} = 30 V, R_C = 8.2 kΩ, and the transistor h_{FE} = 100. Calculate the required base resistance value to give V_{CE} = 7 V.

5-33 Design a voltage divider bias circuit to have V_{CE} = 10 V and I_C = 1 mA. The supply is V_{CC} = 30 V.

5-34 Precisely analyze the circuit designed for Problem 5-33 to determine the maximum and minimum levels of V_{CE} when the transistor type used has $h_{FE(min)}$ = 40 and $h_{FE(max)}$ = 80.

5-35 A voltage divider bias circuit with V_{CC} = 20 V and R_C = 6 kΩ uses a transistor with h_{FE} = 80. Calculate suitable resistor values to give V_{CE} = 8 V.

5-36 Design a voltage divider bias circuit using a 2N3906 transistor. The supply voltage is 22 V, the collector current is to be 10 mA, and the collector-emitter voltage is to be 4 V.

5-37 Precisely analyze the circuit in Problem 5-35 to determine the levels of V_{CE} and I_C.

5-38 Design a voltage divider bias circuit to have V_{CE} = 4 V, V_E = 5 V, and I_C = 1.3 mA. the supply is V_{CC} = 18 V.

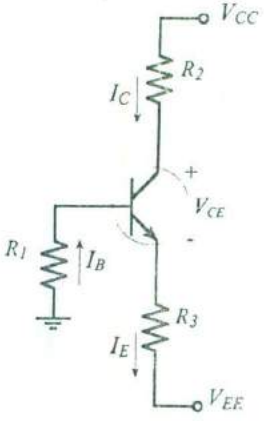


Figure 5-67
Emitter current bias circuit for Problem 5-39.

Section 5-8

5-39 Design an emitter current bias circuit (as in Fig. 5-67) to have V_{CE} = 6 V and I_C = 10 mA. The supply is V_{CC} = ±18 V and the transistor has h_{FE} = 100.

5-40 Precisely analyze the circuit in Problem 5-39 to determine the levels of V_{CE} and I_C.

5-41 An emitter current bias circuit has a 10 kΩ emitter resistor and $V_{CC} = \pm 20$ V. Calculate suitable base and collector resistor values to give $V_{CE} = 8$ V when $h_{FE} = 75$.

5-42 Determine suitable resistor values for the circuit in Fig. 5-68.

5-43 A circuit employing collector-to-base bias and voltage divider bias as in Fig. 5-68 uses a 30 V supply. Design the circuit to have $V_{CE} = 10$ V and $I_C = 10$ mA.

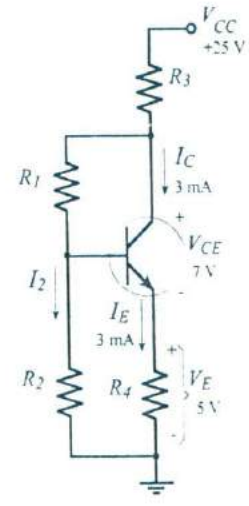


Figure 5-68
Circuit for Problem 5-42.

Section 5-9

5-44 Determine the stability factors for the circuit in Problems 5-7, 5-11, and 5-15.

5-45 Calculate the I_C changes produced in each of the circuits referred to in Problem 5-44 when the circuit temperature changes from 25°C to 75°C. The transistor collector-base leakage current is specified as 25 nA at 25°C.

5-46 The voltage divider bias circuit in Problems 5-33 and 5-34 is to have a maximum I_C change of 15 μA due to change in I_{CBO} when the circuit temperature increases from 25°C to 35°C. Determine the maximum acceptable level of I_{CBO} for the transistor at 25°C.

5-47 Determine the I_C change produced in the circuits designed in Problems 5-33, 5-35, and 5-39 by the effect of transistor V_{BE} changes over a temperature range of 25°C to 75°C.

5-48 A voltage divider bias circuit is to have a maximum I_C change of 50 μA due to change in V_{BE} when the circuit temperature increases from 25°C to 75°C. Determine the minimum acceptable emitter resistance value.

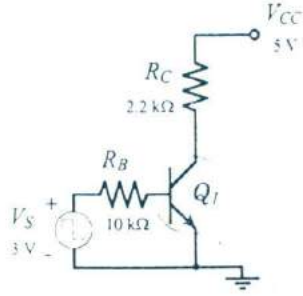


Figure 5-69
Circuit for Problem 5-49.

Section 5-10

5-49 Calculate $h_{FE(min)}$ for the transistor in the direct-coupled switching circuit in Fig. 5-69.

5-50 The normally-*on* capacitor-coupled switching circuit in Fig. 5-70 uses a transistor with $h_{FE(min)} = 40$. Determine a suitable resistance for R_B.

5-51 A direct-coupled transistor switching circuit (as in Fig. 5-69) with $V_{CC} = 9$ V and $V_S = 6$ V is to have $I_C = 5$ mA. Calculate suitable resistances for R_C and R_B.

5-52 A direct-coupled transistor switching circuit has $V_{CC} = 9$ V and $V_S = 1.6$ V. The resistor values are $R_C = 2.7$ kΩ and $R_B = 4.7$ kΩ. Calculate the minimum transistor h_{FE} value for saturation. Will the transistor be saturated if R_C is changed to 1 kΩ, and $h_{FE} = 40$?

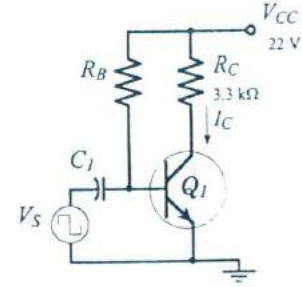


Figure 5-70
Circuit for Problem 5-50.

5-53 The normally-*off* capacitor-coupled switching circuit in Fig. 5-71 uses a transistor with $h_{FE(min)} = 40$. Determine suitable resistances for R_B and R_C.

5-54 A normally-*on* capacitor-coupled switching circuit has $V_{CC} = 12$ V and $R_C = 3.9$ kΩ. Determine a suitable resistance for R_B.

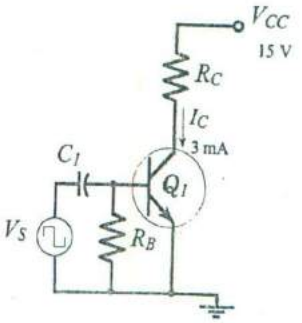


Figure 5-71
Circuit for Problem 5-53.

Practise Problem Answers

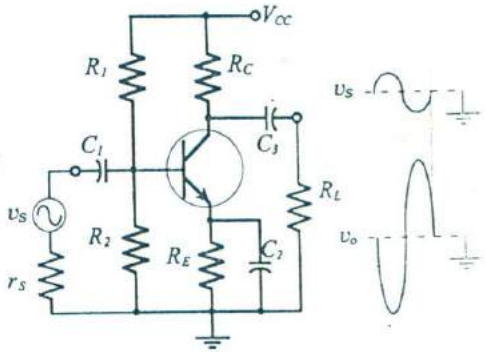
5-1.1 Q-point (40 μA, 4 V, 3.6 mA)
5-1.2 Q-point (10 μA, 0.5 mA, 9 V), $\Delta V_o = \pm 6$ V
5-1.3 Q-point (g0 μA, 6.25 mA, 4.5 V), $\Delta V_o \approx \pm 4.5$ V
5-2.1 (9.2 mA, 2.76 mA), (11.93 V, 0 V)
5-2.2 71, 4.3 V
5-3.1 (5.26 mA, 2.97 mA), (11.38 V, 6.38 V)
5-3.2 81, 7.93 V
5-4.1 1.06 mA, 15.3 V, 10.3 V
5-4.2 11.8 V, 10.7 V
5-4.3 4.26 V, 12.7 V
5-7.1 470 kΩ, 2.7 kΩ
5-7.2 150 kΩ, 6.8 kΩ
5-7.3 100 kΩ, 39 kΩ, 8.2 kΩ, 3.9 kΩ
5-7.4 (56 kΩ + 5.6 kΩ), 27 kΩ, 3.9 kΩ, 2.7 kΩ
5-8.1 (560 kΩ + 15 kΩ), 5.6 kΩ, 3.3 kΩ
5-8.2 22 kΩ, 27 kΩ, 2.7 kΩ, 2.2 kΩ
5-8.3 2.7 kΩ, 1.2 kΩ, 3.3 kΩ
5-9.1 126, 18.6, 7.5
5-9.2 1.29 mA, 190 μA, 76.5 μA
5-9.3 51.7 μA
5-10.1 12.1
5-10.2 100 kΩ
5-10.3 2.2 kΩ, 8.2 kΩ

Chapter 6

AC Analysis of BJT Circuits

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Objectives

You will be able to:

1. Explain the need for coupling and bypass capacitors in transistor circuits, and draw ac equivalents for circuits containing capacitors.
2. Draw ac load lines for basic transistor circuits.
3. Sketch and explain transistor r-parameter and h-parameter models.
4. Show how h-parameters can be derived from device characteristics.
5. Convert between CE, CC, and CB h-parameters, and between h-parameters and r-parameters.
6. Sketch h-parameter circuits for various CE, CC, and CB transistor circuits.
7. Analyze various CE, CC, and CB transistor circuits to determine input resistance, output resistance, voltage gain, current gain, and power gain.
8. Compare the performance of CE, CC, and CB circuits.

Introduction

A transistor circuit used as an *ac* amplifier normally has the signal source capacitor-coupled to the circuit input terminal. A load resistor at the output is also usually capacitor-coupled to the circuit. Capacitor-coupling ensures that the source and load do not affect the *dc* bias conditions in the circuit. An *ac* load line can be drawn on the transistor output characteristics to study the *ac* performance of a circuit. All transistor circuits, however complicated, are based on one of the three basic circuits configurations — common-emitter, common-collector, or common-base. The three basic circuits have different input impedances, output impedances, and voltage gains, and these are most easily determined by the use of *h*-parameters. Multistage transistor circuit can also be analyzed by application of *h*-parameters.

6-1 Coupling and Bypassing Capacitors

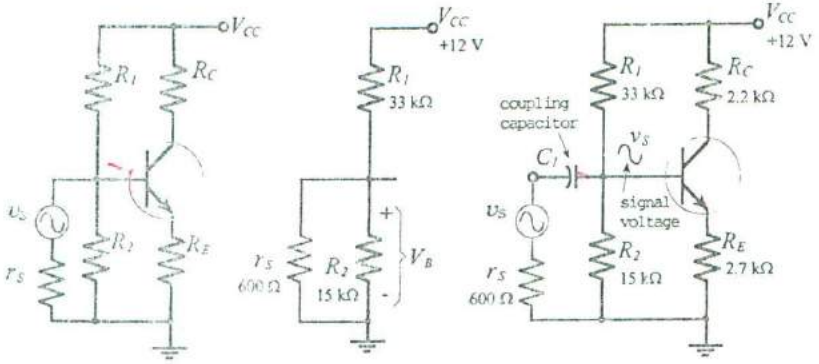
Coupling Capacitors

To use a transistor circuit to amplify or otherwise process an *ac* signal, the signal source must be connected to the circuit input. If the source is directly connected to the input, as illustrated in Fig. 6-1(a), the circuit bias conditions will be altered. Figure 6-1(b) shows that the signal source resistance (r_S) is in parallel with voltage-divider resistor R_2 when the signal is directly connected to the circuit. Thus, the bias voltage is altered to,

$$V_B = \frac{V_{CC} \times (r_S \| R_2)}{R_1 + (r_S \| R_2)}$$

instead of,

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$



(a) Signal source incorrectly *direct-coupled* to the circuit

(b) V_B is altered by the *dc-coupled* signal source

(c) Signal source *capacitor-coupled* to the circuit

Figure 6-1
AC input signals must be capacitor-coupled to the input terminal of a transistor circuit. Direct coupling would alter the circuit bias conditions.

Figure 6-1(c) shows the use of capacitor C_1 to couple the signal source to the circuit input. Because C_1 is an open-circuit to direct currents, r_S does not affect the level of V_B. Capacitor C_1 behaves as a short-circuit for the *ac* signals, so that the signal voltage (v_S) appears at the transistor base, as illustrated. In this case, the signal is said to be *ac coupled* to the circuit input, and C_1 is referred to as a *coupling-capacitor*. Input coupling capacitors are normally used with all types of bias circuits, otherwise the circuit bias conditions will be altered.

A coupling capacitor is usually required at the output of a transistor circuit (as well as at the input) to couple to a load resistor, or to another amplification stage. Figures 6-2(a) and (b) show the effect of directly coupling a load (R_L) to the circuit output. The supply voltage at the transistor collector terminal is reduced from V_{CC} to,

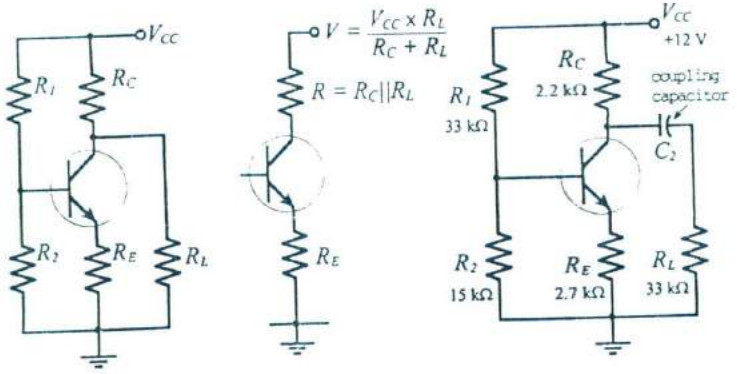
$$V = \frac{V_{CC} \times R_L}{R_C + R_L}$$

and the collector resistance becomes,

$$R = R_C || R_L$$

This has the effect of altering the circuit *dc* load line and *Q*-point.

The use of an output coupling capacitor (C_2) is illustrated in Fig. 6-2(c). Like the input coupling capacitor, C_2 offers a *dc* open-circuit and behaves as an *ac* short-circuit. Thus, it passes the output waveform to the load without affecting the circuit bias conditions.



(a) Load resistor incorrectly direct-coupled to the circuit

(b) The collector voltage is altered by the direct-coupled load

(c) Load resistor *capacitor-coupled* to the circuit

Figure 6-2
Output loads must be capacitor-coupled to the output terminal of a transistor circuit. Direct coupling will alter the circuit bias conditions.

Example 6-1

Calculate the base bias voltage for the circuit in Fig. 6-1(c) when no signal source is present, and when the signal source is directly connected as in Fig. 6-1(a).

Solution

With no signal source,

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{12\text{ V} \times 15\text{ k}\Omega}{33\text{ k}\Omega + 15\text{ k}\Omega}$$

$$= 3.75\text{ V}$$

With the signal source directly connected,

$$V_B = \frac{V_{CC} \times (r_S \| R_2)}{R_1 + (r_S \| R_2)} = \frac{12\text{ V} \times (600\ \Omega \| 15\text{ k}\Omega)}{33\text{ k}\Omega + (600\ \Omega \| 15\text{ k}\Omega)}$$

$$= 0.21\text{ V}$$

AC Degeneration

In the discussion on collector-to-base bias, it was explained that an increase in I_B would produce a decrease in V_{CE}, and this would tend to cancel the original increase in I_B. This, of course, is an effect that produces good bias stability, however, this same reaction occurs when an *ac* signal is applied to the circuit input for amplification. The voltage change at the transistor collector (produced by the *ac* input) is fed back to the base where it tends to partially cancel the signal. The effect is termed *ac degeneration*, and it can result in a very low voltage gain.

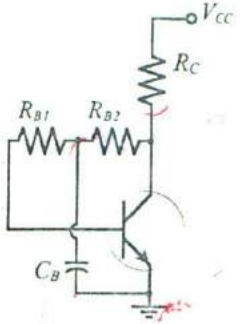
Figure 6-3(a) shows how *ac* degeneration is eliminated in collector-to-base bias circuits. R_B is replaced with two approximately equal resistors (R_{B1} and R_{B2}), which add up to R_B. A *bypass capacitor* (C_B) is connected from the junction of R_{B1} and R_{B2} to the ground terminal, as illustrated. Capacitor C_B offers a short-circuit to *ac* signals, so that there is no feedback from the transistor collector to the base. Figure 6-3(b) shows that, when C_B is replaced with a short-circuit, R_{B1} and R_{B2} appear in parallel with the circuit input and output respectively. Because they are large-value resistors, they do not affect the circuit voltage gain.

Emitter Bypassing

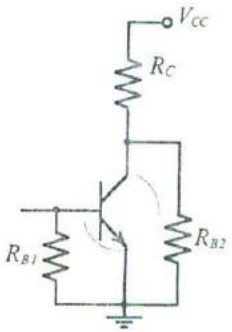
Voltage divider bias circuits also suffer *ac* degeneration because of the presence of the emitter resistor (R_E). In this case, the *ac* signal voltage is developed across R_E and the transistor *BE* junction in series, instead of just across the *BE* junction alone. The problem is eliminated by the *emitter bypass* capacitor (C_E) illustrated in Fig. 6-4, which provides an *ac* short-circuit across R_E.

Capacitor polarity

Bypass capacitors are usually polarized (electrolytic-type), and coupling capacitors can also be polarized, so it is very important that capacitors are correctly connected. As discussed in Section 3-3, *incorrectly connected polarized capacitors can* ***explode!*** Also, electrolytic capacitors tend to have a high leakage current when incorrectly connected, so even if they do not explode, *they can affect circuit bias conditions.* The positive terminal must be connected to the more positive of the two circuit points where the capacitor is installed.



(a) Bypass capacitor used with collector-to-base bias



(b) The bypass capacitor is an *ac* short-circuit

Figure 6-3
A collector-to-base bias circuit must use two resistors for R_B with the junction of the two ac grounded via a capacitor. This is necessary to eliminate ac degeneration.

The capacitor positive terminal is represented by the straight line on the capacitor symbol, or is identified by the plus sign on the alternative capacitor symbol, (see Fig 6-4). The transistor emitter terminal in Fig. 6-4 is more positive than ground level, as illustrated. Consequently, the positive terminal of the emitter bypass capacitor is connected at the transistor emitter, and the negative terminal goes to ground.

Figure 6-5 shows a circuit with correctly-connected coupling and bypass capacitors. The *dc* voltage level at the right side of C_1 is +0.7 V, and the left side is grounded via the signal source. So, the polarity is *plus* on the right, *minus* on the left. The voltage at the junction of resistors R_{B1} and R_{B2} is +3.2 V. consequently, the positive terminal of C_2 must be connected at that point, and C_2 negative terminal is grounded. Output coupling capacitor C_3 has its left side at +5.7 V, and the right side is grounded via R_L, requiring the capacitor to be connected as illustrated.

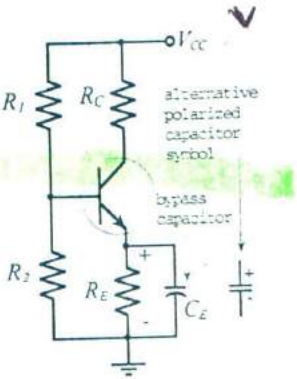


Figure 6-4
A resistor connected in series with the transistor emitter must be ac short-circuited by means of a bypass capacitor to ensure maximum amplification.

Practise Problems

6-1.1 Calculate the transistor collector voltage for the circuit in Fig. 6-2(c) with C_2 present, and with R_L directly connected.

6-2 AC Load Lines

AC Equivalent Circuits

Capacitors behave as short-circuits to *ac* signals, so in the *ac equivalent circuit* for a transistor circuit all capacitors must be replaced with short-circuits. Power supplies also behave as *ac* short-circuits, because the *dc* supply voltage is not affected by *ac* signals. Also, all power supplies have large-value capacitors at the output terminals, and these will offer short-circuits to *ac* signals. Substituting short-circuits in place of the power supply and all capacitors in the circuit in Fig. 6-6(a) gives the *ac* equivalent circuit in Fig. 6-6(b). If R_L is present, as shown, it appears in parallel with R_C in the *ac* equivalent circuit.

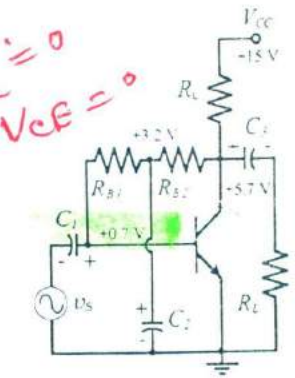
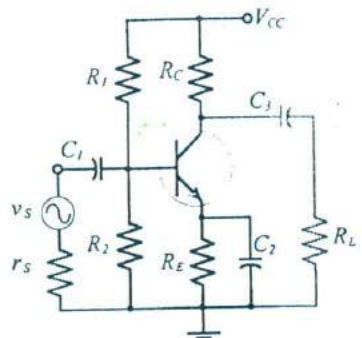
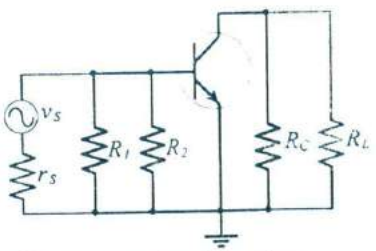


Figure 6-5
Polarized capacitors must be correctly connected, to avoid high leakage current and the possibility of capacitor explosion.



(a) Circuit with coupling and bypass capacitors



(b) Power supply and capacitors behave as *ac* short-circuits

Figure 6-6
Voltage divider bias circuit with coupling and bypass capacitors, and the ac equivalent circuit

Once the *ac* equivalent circuit is drawn, the circuit *ac* performance can be investigated by drawing an *ac* load line, and by substituting a transistor model in place of the device.

AC Load Lines

The *dc* load for the circuit in Fig. 6-6(a) is $(R_C + R_E)$, consequently, the *dc* load line is drawn (as discussed in Section 5-1) for a total resistance of $(R_C + R_E)$. Because the emitter resistor is capacitor bypassed in Fig. 6-6(a), resistor R_E is not part of the circuit *ac* load. If external load R_L were not present, the circuit *ac* load would simply be R_C. With R_L capacitor-coupled to the circuit output, the ac load is $R_C \| R_L$. An *ac load line* may now be drawn to represent the circuit *ac* performance.

When there is no input signal, the transistor voltage and current conditions are exactly as indicated by the *Q*-point on the *dc* load line. An *ac* signal causes the transistor voltage and current levels to vary above and below the *Q*-point. Therefore, the *Q*-point is common to both the *ac* and *dc* load lines. Starting from the *Q*-point, another point is found on the *ac* load line by taking a convenient collector current change (usually $\Delta I_C = I_{CQ}$) and calculating the corresponding collector-emitter voltage change (ΔV_{CE}), (see Fig. 6-8). As demonstrated in Ex. 6-2, *point C* is plotted by measuring ΔI_C and ΔV_{CE} from the *Q*-point. The *ac* load line is then drawn through points *C* and *Q*, as illustrated.

Example 6-2

Draw the *dc* and *ac* load lines for the transistor circuit in Fig. 6-7, using the transistor common-emitter characteristics in Fig. 6-8.

Solution

dc load line,

$$R_{L(dc)} = R_C + R_E = 2.2\ \text{k}\Omega + 2.7\ \text{k}\Omega$$
$$= 4.9\ \text{k}\Omega$$

The equation for V_{CE} *is,*

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 20\ \text{V}$

Plot point A at, $I_C = 0$ *and* $V_{CE} = 20\ \text{V}$

When $V_{CE} = 0$, $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{20\ \text{V}}{4.9\ \text{k}\Omega}$

$$= 4.08\ \text{mA}$$

Plot point B at, $I_C = 4.08\ \text{mA}$ *and* $V_{CE} = 0$

Draw the dc load line through points A and B.

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{20\ \text{V} \times 8.2\ \text{k}\Omega}{18\ \text{k}\Omega + 8.2\ \text{k}\Omega}$$
$$= 6.3\ \text{V}$$

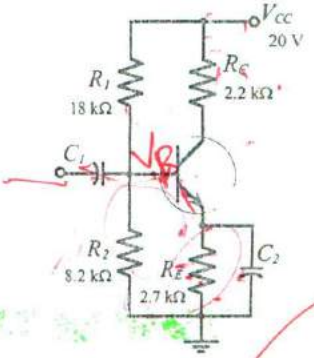


Figure 6-7
Voltage divider bias circuit with a bypassed emitter resistor. The dc load is $(R_C + R_E)$, *and the ac load is* R_C *when there is no capacitor-coupled load.*

$$V_E = V_B - V_{BE} = 6.3\text{ V} - 0.7\text{ V}$$
$$= 5.6\text{ V}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{5.6\text{ V}}{2.7\text{ k}\Omega}$$
$$= 2.07\text{ mA}$$

Mark the Q-point on the dc load line at

$$I_C = 2.07\text{ mA}.$$

ac load line,
when there is no external R_L,

$$R_{L(ac)} = R_C = 2.2\text{ k}\Omega$$

When I_C changes by $\Delta I_C = 2.07$ mA,

$$\Delta V_{CE} = \Delta I_C \times R_C$$
$$= 2.07\text{ mA} \times 2.2\text{ k}\Omega$$
$$= 4.55\text{ V}$$

Plot point C at, $\Delta I_C = 2.07$ mA and $\Delta V_{CE} = 4.55$ V from the Q point.
Draw the ac load line through points C and Q.

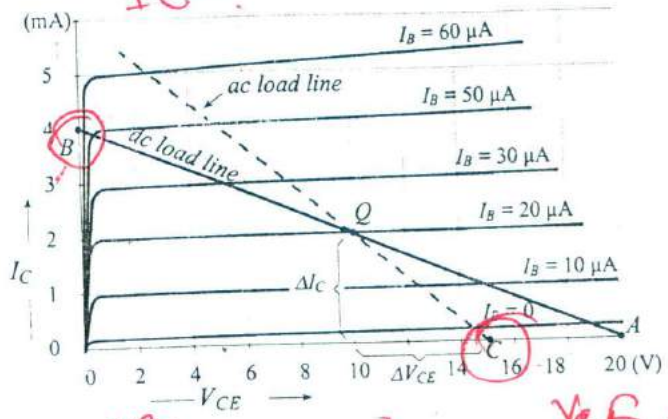


Figure 6-8
The ac load line for a transistor circuit is drawn through the Q-point.

The Output Voltage Swing

In Section 5-1 it is explained that the maximum symmetrical output voltage swing ($\pm V_{o(max)}$) from a common-emitter circuit depends upon the *Q*-point position on the *dc* load line. In the case of a circuit with a bypassed emitter resistor or a capacitor-coupled load, the maximum symmetrical output swing depends upon the *Q*-point position on the *ac* load line. For the ac load line shown in Fig. 6-10.

$$V_{o(max)} \approx \pm 4.5\text{ V}$$

Practise Problems

6-2.1 Draw the new ac load line for the transistor circuit in Ex. 6-2, when a 5.6 kΩ external load is capacitor-coupled to the circuit output. Also, determine the new maximum possible symmetrical output voltage swing.

6-3 Transistor Models and Parameters

T-Equivalent Circuit

Because a transistor consists of two *pn*-junctions with a common centre block, it should be possible to use two *pn*-junction diodes as the transistor model. Figure 6-9 shows the *ac* equivalent circuit for a transistor connected in common-base configuration. Resistor r_e represents the *BE* junction resistance, r_c represents the *CB* junction resistance, and r_b represents the resistance of the base region which is common to both junctions. Junction capacitances C_{BE} and C_{BC} are also included.

If the transistor equivalent circuit is simply left as a combination of resistances and capacitances, it could not account for the fact that most of the emitter current flows out of the collector terminal as collector current. To represent this, a current generator is included in parallel with r_c and C_{BC}. The current generator is given the value αI_e, where $\alpha = I_c/I_e$.

The complete circuit is known as the *T-equivalent circuit*, or the *r-parameter equivalent circuit*. The equivalent circuit can be arranged in common-emitter or common-collector configuration. The currents in Fig. 6-9 are designated I_b, I_c, and I_e (instead of I_B, I_C, and I_E) to indicate that they are *ac* quantities rather than *dc*. The circuit parameters r_c, r_b, r_e, and α, are also *ac* quantities.

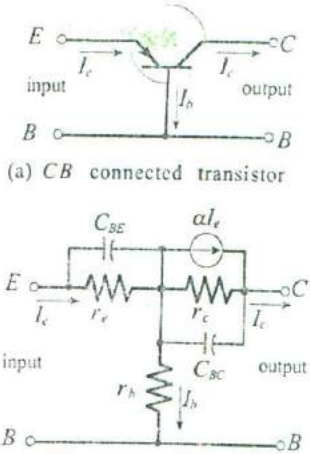


Figure 6-9
The T-equivalent circuit, or r-parameter circuit for a transistor is essentially a combination of two pn-junction equivalent circuits.

r-Parameters

Referring to Fig. 6-9, r_e represents the *ac* resistance of the forward-biased *BE* junction, so it has a low resistance value, (typically 25 Ω). The resistance of the reverse-biased *CB* junction (r_c) is high, (typically 100 kΩ to 1 MΩ). The base region resistance (r_b) depends upon the doping density of the base material. Usually, r_b ranges from 100 Ω to 300 Ω.

C_{BE} is the capacitance of a forward-biased *pn*-junction, and C_{BC} is that of a reverse-biased junction, (see Section 2-6). At medium and low frequencies the junction capacitances may be neglected. Instead of the current generator (αI_e) in parallel with r_c, a voltage generator ($\alpha I_e r_c$) may be used in series with r_c. Two transistor *r*-parameter models are shown in Fig. 6-10.

Determination of r_e

Because r_e is the *ac* resistance of the *BJT* forward-biased base-emitter junction, it can be determined from a plot of I_E versus V_{BE}. As illustrated in Fig. 6-11,

$$r_e = \frac{\Delta V_{BE}}{\Delta I_E} \qquad (6\text{-}1)$$

This is similar to the determination of the dynamic resistance (r_d) for a forward-biased diode, (see Section 2-2). Also like the case of a diode, the *ac* resistance for the transistor *BE* junction can be calculated in terms of the current crossing the junction.

$$r'_e = \frac{26\ \text{mV}}{I_E} \qquad (6\text{-}2)$$

As in the case of r'_d for a diode, r'_e does not include the resistance of the device semiconductor material. Consequently, r'_e is slightly smaller than the actual measured value of r_e for a given transistor.

Equation 6-2 applies only to transistors at a temperature of 25°C. For determination of r'_e at higher or lower temperatures, the equation must be modified.

$$r'_e = \frac{26\ \text{mV}}{I_E}\left[\frac{T + 273°\text{C}}{298°\text{C}}\right] \qquad (6\text{-}3)$$

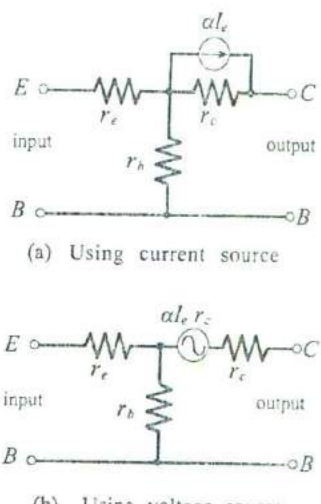


Figure 6-10
Transistor low-frequency r-parameter ac equivalent circuits.

h-Parameters

It has been shown that transistor circuits can be represented by an *r*-parameter or *T*-equivalent circuit. In circuits involving more than a single transistor, analysis by *r*-parameters can be virtually impossible. The *hybrid parameters*, or *h-parameters* are much more convenient for circuit analysis. These are used only for *ac* circuit analysis, although *dc* current gain factors are also expressed as *h*-parameters. Transistor *h*-parameter models simplify transistor circuit analysis by separating the input and output stages of a circuit to be analyzed.

In Fig. 6-12 a common-emitter *h-parameter equivalent circuit* is compared with a common-emitter *r*-parameter circuit. In each case an external collector resistor (R_C) is included, as well as a signal source voltage (v_s) and source resistance (r_s). Note that the output current generator in the *r*-parameter circuit has a value of αI_e, which equals βI_b.

The input to the *h*-parameter circuit is represented as an input resistance (h_{ie}) in series with a voltage source ($h_{re}v_{ce}$). Looking at the *r*-parameter circuit, it is seen that a change in output current I_c causes a voltage variation across r_e. This means that a voltage is *fed back* from the output to the input. In the *h*-parameter circuit this feedback voltage is represented as the portion h_{re} of the output voltage v_{ce}. The parameter h_{re} is appropriately termed the *reverse voltage transfer ratio*.

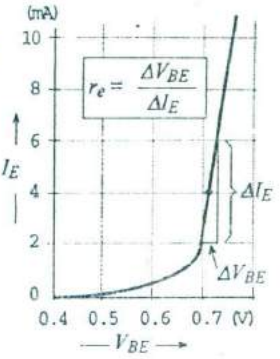
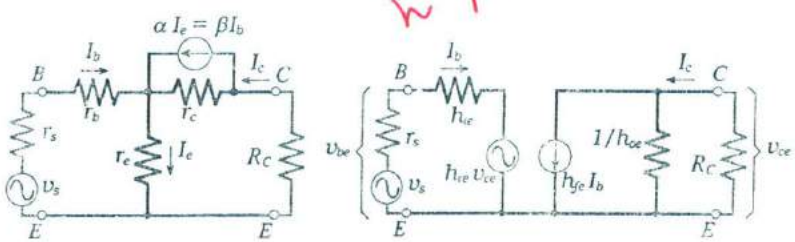


Figure 6-11
Determination of r_e from the transistor base-emitter junction forward characteristic.



(a) *CE r*-parameter equivalent circuit (b) *CE h*-parameter equivalent circuit

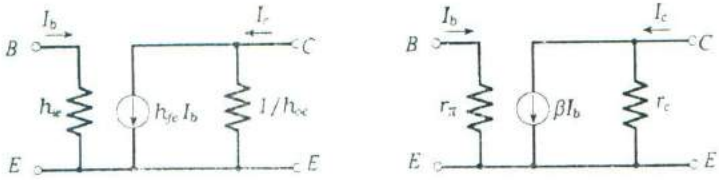
Figure 6-12
Comparison of common-emitter r-parameter and h-parameter equivalent circuits.

The output of the *h*-parameter circuit is represented as an output resistance ($1/h_{oe}$) in parallel with a current generator ($h_{fe}I_b$), where I_b is the (input) base current. So, $h_{fe}I_b$ is produced by the input current I_b, and it divides between the device output resistance $1/h_{oe}$ and the collector resistor R_C. I_c is the current passed to R_C. This compares with the *r*-parameter equivalent circuit, where some of the generator current (βI_b) flows through r_c. The current generator parameter (h_{fe}) is termed the *forward transfer current ratio*. The *output conductance* is h_{oe}, so that $1/h_{oe}$ is a resistance.

r_π Equivalent Circuit

An approximate *h*-parameter model for a transistor *CE* circuit is shown in Fig. 6-13(a). In this case, the feedback generator [$h_{re}v_{ce}$ in Fig. 6-12(b)] is omitted. The effect of $h_{re}v_{ce}$ is normally so small that it can be neglected for most practical purposes.

The approximate *h*-parameter circuit is reproduced in Fig. 6-13(b) with the components labelled as *r*-parameters; $r_\pi = h_{ie}$, $\beta I_b = h_{fe} I_b$, and $r_c = 1/h_{oe}$. This circuit, known as a *hybrid-π* model, is sometimes used instead of the *h*-parameter circuit.



(a) *CE h*-parameter transistor model (b) *CE* r_π transistor model

Figure 6-13
Transistor h-parameter and r_π *equivalent circuits.*

Definition of h-Parameters

The *e* in the subscript of h_{ie} identifies the parameter as a *common-emitter* quantity, and the *i* signifies that it is an *input* resistance. Common-base and common-collector input resistances are designated h_{ib} and h_{ic}, respectively.

As an *ac* input resistance, h_{ie} can be defined as the *ac* input voltage divided by the *ac* input current.

$$h_{ie} = \frac{V_{be}}{I_b}$$

This is usually stated as,

$$h_{ie} = \frac{V_{be}}{I_b}\bigg|_{V_{CE}} \qquad (6\text{-}4)$$

This means that the collector-emitter voltage (V_{CE}) must remain constant when h_{ie} is measured.

The input resistance can also be defined in terms of changes in *dc* levels;

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}\bigg|_{V_{CE}} \qquad (6\text{-}5)$$

Equation 6-5 can be used for determining h_{ie} from the transistor common-emitter input characteristics. As illustrated in Fig. 6-14, ΔV_{BE} and ΔI_B are measured at one point on the characteristics, and h_{ie} is calculated.

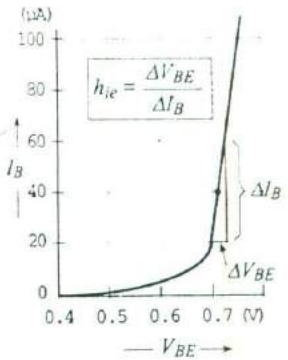


Figure 6-14
Derivation of h_{ie} *from the CE input characteristics.*

The reverse transfer ratio h_{re} can also be defined in terms of *ac* quantities, or as the ratio of *dc* current changes. In both cases, the input current (I_B) must be held constant.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\bigg|_{I_B} \qquad (6\text{-}6)$$

The forward current transfer ratio h_{fe} can similarly be defined in terms of *ac* quantities, or as the ratio of *dc* current changes. In both cases, the output voltage (V_{CE}) must be held constant.

$$h_{fe} = \frac{I_c}{I_b}\bigg|_{V_{CE}} \qquad (6\text{-}7)$$

or,
$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}} \qquad (6\text{-}8)$$

Equation 6-8 can be used to determine h_{fe} from the *CE* current gain characteristics. Figure 6-15 shows the measurement of ΔI_C and ΔI_B at one point on the characteristics for the h_{fe} calculation.

The output conductance, h_{fe}, is the ratio of *ac* collector current to *ac* collector-emitter voltage, and its value can be determined from the common emitter output characteristics, (see Fig. 6-16).

$$h_{oe} = \frac{I_c}{V_{ce}}\bigg|_{I_B} \qquad (6\text{-}9)$$

or,
$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}\bigg|_{I_B} \qquad (6\text{-}10)$$

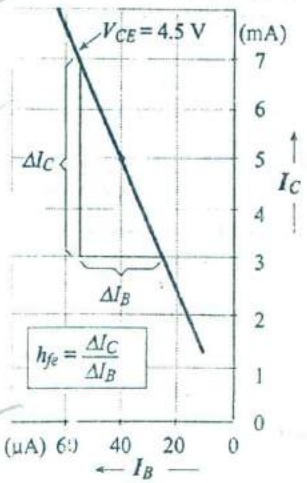


Figure 6-15
Derivation of h_{fe} from the *CE* current gain characteristics.

Example 6-3

Determine h_{fe} and h_{oe} for V_{CE} = 4.5 V and I_B = 40 μA from the transistor characteristics in Figs. 6-15 and 6-16.

Solution

From the current gain characteristics, at V_{CE} = 4.5 V and I_B = 40 μA,

$$\Delta I_C = 4 \text{ mA and } \Delta I_B \approx 30\,\mu\text{A}$$

Eq. 6-8,
$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} = \frac{4 \text{ mA}}{30\,\mu\text{A}}$$
$$= 133$$

From the output characteristics, at V_{CE} = 4.5 V and I_B = 40 μA,

$$\Delta I_C \approx 400\,\mu\text{A and } \Delta V_{CE} = 6 \text{ V}$$

Eq. 6-9,
$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{0.2 \text{ mA}}{6 \text{ V}}$$
$$= 33.3\,\mu\text{S (micro Siemens)}$$
$$1/h_{oe} = \frac{1}{33.3\,\mu\text{S}}$$
$$= 30\,\text{k}\Omega$$

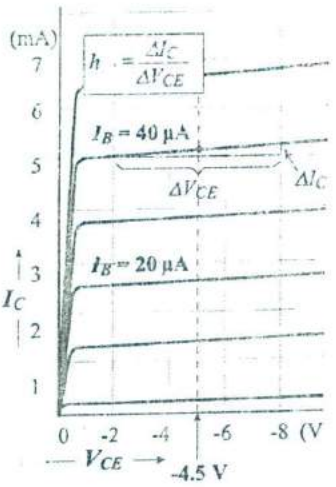


Figure 6-16
Derivation of h_{oe} from the *C* output characteristics.

Common-Base and Common-Collector h-Parameters

The common-base and common-collector *h*-parameters are defined similarly to common-emitter *h*-parameters. They may also be

derived from the *CB* and *CC* characteristics. Common-base parameters are identified as h_{ib}, h_{fb}, etc., and common-collector parameters are designated h_{ic}, h_{fc}, and so on. Common-emitter, common-base, and common-collector *h*-parameter equivalent circuits are further investigated in Sections 6-4 through 6-9.

Parameters Relationships

Device manufacturers do not list the values of all parameters on transistor data sheets. Usually, only the *CE* *h*-parameters are stated. However, *CB* and *CC* *h*-parameters can be determined from the *CE* *h*-parameters. *r*-parameters can also be calculated from the *CE* *h*-parameters. Table 6-1 shows the parameter relationships.

Table 6-1 Conversion from *CE* *h*-parameters to *CB* and *CC* *h*-parameters, and to *r*-parameters.

CE to *CB* *h*-parameters	*CE* to *CC* *h*-parameters	*CE* *h*-parameters to *r*-parameters
$h_{ib} \approx \dfrac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$	$\alpha \approx \dfrac{h_{fe}}{1 + h_{fe}}$
$h_{rb} \approx \dfrac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re}$	$r_e = \dfrac{1 + h_{fe}}{h_{oe}}$
$h_{fb} \approx -\dfrac{h_{fe}}{1 + h_{fe}}$	$h_{fc} = 1 + h_{fe}$	$r'_e = \dfrac{h_{re} 1}{1 + h_{fe}} \approx r'_e$
$h_{ob} \approx \dfrac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$	$r_b = h_{ie} - \dfrac{h_{re}(1 + h_{fe})}{h_{oe}}$
		$r_\pi = h_{ie}$
		$\beta = h_{fe}$

Example 6-4

Calculate h_{fc}, h_{ob}, and α from the parameters determined in Example 6-3.

Solution

from Table 6-1,

$$h_{fc} = 1 + h_{fe} = 1 + 133$$
$$= 134$$

$$h_{ob} \approx \frac{h_{oe}}{1 + h_{fe}} \approx \frac{33.3\ \mu S}{1 + 133}$$
$$= 249\ mS$$

$$\alpha \approx \frac{h_{fe}}{1 + h_{fe}} \approx \frac{133}{1 + 133}$$
$$= 0.993$$

Example 6-5

A transistor in a circuit has its current levels measured as; $I_B = 20\,\mu A$, and $I_C = 1$ mA. Estimate the *CE* input resistance. Also, determine r_π, and β.

Solution

Eq. 6-2, $$r'_e = \frac{26\text{ mV}}{I_E} \approx \frac{26\text{ mV}}{1\text{ mA}}$$
$$= 26\ \Omega$$

$$h_{fe} \approx \frac{I_C}{I_B} \approx \frac{1\text{ mA}}{20\,\mu A}$$
$$= 50$$

$$h_{ie} = (1 + h_{fe})\, r'_e = (1 + 50) \times 26\ \Omega$$
$$\approx 1.33\ k\Omega$$

$$r_\pi = h_{ie} = 1.33\ k\Omega$$

$$\beta = h_{fe} = 50$$

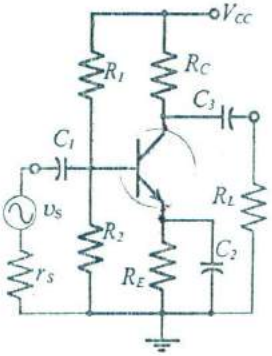


Figure 6-17
Transistor common-emitter amplifier with coupling and bypass capacitors.

Practise Problems

6-3.1 Determine h_{fe} and h_{oe} at $V_{CE} = 6$ V and $I_B = 20\,\mu A$ from the common-emitter output and current gain characteristics in Fig. 4-30.

6-3.2 Calculate α and r_c from the *h*-parameter values determined in Problem 6-3.1.

6-3.3 Calculate h_{ie} for a transistor at a temperature of 50°C when the emitter current is 1.3 mA and $h_{fe} = 80$.

6-4 *Common-Emitter Circuit Analysis*

Common-Emitter Circuit

Consider the transistor amplifier circuit shown in Fig. 6-17. When the capacitors are regarded as *ac* short-circuits, it is seen that the circuit input terminals are the transistor base and emitter, and the output terminals are the collector and the emitter. So, the emitter terminal is *common* to both input and output, and the circuit configuration is termed *common-emitter* (*CE*).

The current and voltage waveforms for the *CE* circuit in Fig. 6-17 are illustrated in Fig. 6-18. It is seen that there is a 180° *phase shift* between the input and output waveforms. This can be understood by considering the effect of a positive-going input signal. When v_s increases in a positive direction, it increases the transistor base-emitter voltage (V_{BE}). The increase in V_{BE} raises the level of I_C, thereby increasing the voltage drop across R_C, and thus reducing the level of the collector voltage (V_C). The changing level of V_C is capacitor-coupled to the circuit output to produce the *ac* output voltage (v_o). As v_s increases in a positive direction, v_o goes

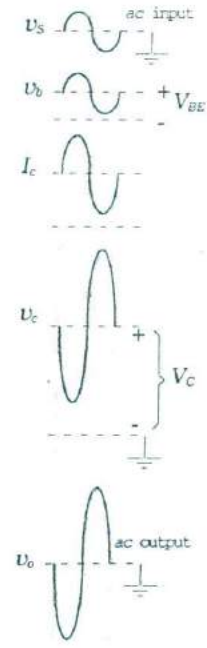
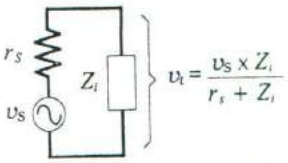


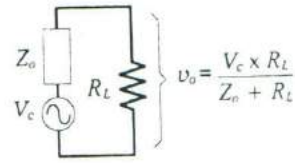
Figure 6-18
Voltage and current waveforms in a common-emitter amplifier.

in a negative direction, as illustrated. Similarly, when v_s changes in a negative direction, the resultant decrease in V_{BE} reduces the I_C level, thereby reducing V_{RC}, and producing a positive-going output.

The circuit in Fig. 6-17 has an *input impedance* (Z_i), and an *output impedance* (Z_o). These can cause voltage division of the circuit input and output voltages, as illustrated in Fig. 6-19. So, for most transistor circuits, Z_i and Z_o are important parameters. The circuit voltage amplification (A_v), or *voltage gain*, depends on the transistor parameters and on resistors R_C and R_L.



(a) Division of signal voltage

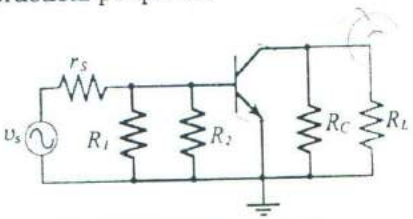


(b) Division of output voltage

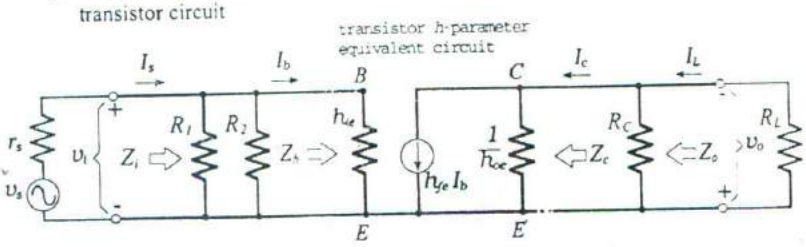
Figure 6-19
Circuit input and output voltages are divided by the effects of Z_i and Z_o.

h-Parameter Equivalent Circuit

The first step in *ac* analysis of a transistor circuit is to draw the *ac* equivalent circuit, by substituting short-circuits in place of the power supply and capacitors. When this is done for the circuit in Fig. 6-17, it gives the *ac* equivalent circuit shown in Fig. 6-20(a) [reproduced from Fig. 6-6(b)]. The *h*-parameter circuit is now drawn simply by replacing the transistor in the *ac* equivalent circuit with its *h*-parameter model, [from Fig. 6-12(b)]. This gives the *CE* *h*-parameter equivalent circuit in Fig. 6-20(b). Note that the feedback voltage generator ($h_{re}v_c$) in Fig. 6-12(b) is omitted in Fig. 6-20(b). As discussed, the effect of $h_{re}v_c$ in a *CE* circuit is unimportant for most practical purposes.



(a) *ac* equivalent circuit for *CE* transistor circuit



(b) *h*-parameter equivalent circuit for *CE* circuit

Figure 6-20
A common-emitter h-parameter circuit is drawn by first replacing the power supply and all capacitors with short-circuits, then the h-parameter model is substituted for the transistor.

The current directions and voltage polarities in Fig. 6-20(b) are those that occur when the instantaneous level of the input voltage is moving in a positive direction.

Input Impedance

The input section of the *h*-parameter circuit in Fig. 6-20(b) reproduced in Fig. 6-21 shows that the input impedance at the transistor terminals is,

$$Z_b \approx h_{ie} \qquad \textbf{(6-11)}$$

A typical value of h_{ie} for a low-current transistor is 1.5 kΩ. If h_{ie} is not known, it can be estimated by first calculating r'_e from Eq. 6-2 or Eq. 6-3, as appropriate. Then $r'_e = h_{ib}$, and $h_{ie} = (1 + h_{fe})h_{ib}$.

Z_b is the input impedance at the device base terminal. At the circuit input terminals, resistors R_1 and R_2 are seen to be in parallel with Z_b. So, the circuit input impedance is,

$$Z_i = R_1 \| R_2 \| Z_b \tag{6-12}$$

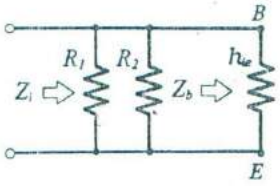


Figure 6-21
The transistor input impedance in a CE circuit is Z_b and the circuit input impedance is $Z_b \| R_1 \| R_2$.

Output Impedance

'Looking into' the output of the *CE* *h*-parameter circuit reproduced in Fig. 6-22, the output impedance at the transistor collector is,

$$Z_c \approx 1/h_{oe} \tag{6-13}$$

At the circuit output terminals, resistor R_C is in parallel with Z_c. So, the circuit output impedance is,

$$Z_o = R_C \| (1/h_{oe}) \tag{6-14}$$

Because $1/h_{oe}$ is typically 50 kΩ, and R_C is usually much less than 50 kΩ, the circuit output impedance is approximately equal to R_C. Using this information, it is possible to tell the output impedance of a *CE* circuit simply by reading the resistance of R_C.

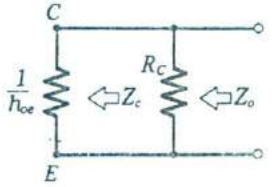


Figure 6-22
The output impedance for a CE circuit is $R_C \| (1/h_{oe})$.

Voltage Gain

The circuit voltage gain is given by the equation,

$$A_v = \frac{v_o}{v_i}$$

Figure 6-23(a) and (b) reproduced from Fig. 6-20 shows that,

$$v_i = I_b h_{ie}, \text{ and } v_o = -I_C (R_C \| R_L \| 1/h_{oe}),$$

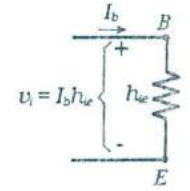
so,

$$A_v = \frac{-I_C (R_C \| R_L \| 1/h_{oe})}{I_b h_{ie}}$$

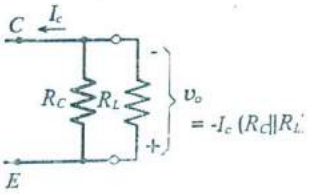
I_C/I_b can be replaced with h_{fe}. Also, because $1/h_{oe}$ can be omitted from the equation because it is usually much larger than $(R_C \| R_L)$. The normally used voltage gain equation now becomes,

$$A_v = \frac{-h_{fe} (R_C \| R_L)}{h_{ie}} \tag{6-15}$$

The minus sign in Eq. 6-15 indicates that v_o is 180° out of phase with v_i. (When v_i increases, v_o decreases, and vice versa.) Knowing the appropriate *h*-parameters as well as R_C and R_L, the voltage gain of a *CE* circuit can be quickly estimated. Using values of R_C = 4.7 kΩ, h_{fe} = 70, h_{ie} = 1.5 kΩ, and assuming that $R_L >> R_C$, a typical *CE* voltage gain is -220.



(a) Input voltage



(b) output voltage

Figure 6-23
Derivation of equations for v_i and v_o in a CE circuit.

Substituting from Table 6-1, the *CE* voltage gain equation can be rewritten as,

$$A_v \approx \frac{-(R_C \| R_L)}{h_{ib}} \qquad (6\text{-}16)$$

h_{ib} can be determined approximately as r'_e from the emitter current level. So, Eq. 6-16 can be useful in cases where the device parameters are not known.

Current Gain

The transistor current gain is,

$$h_{fe} = \frac{I_C}{I_b} \qquad (6\text{-}17)$$

This is the device current gain, *not* the circuit current gain. Examination of the circuit in Fig. 6-20 shows that the signal current (I_s) is divided between h_{ie} and the bias resistors [$R_B = (R_C \| R_L)$]. Also, that the output current from the transistor collector (I_c) is divided between R_C and R_L. The overall circuit current gain can be shown to be,

$$A_i = \frac{h_{fe} R_C R_B}{(R_C + R_L)(R_C + h_{ie})} \qquad (6\text{-}18)$$

In virtually all practical applications, the current gain of a transistor amplifier is normally **not** *an important quantity.*

Power Gain

The power gain of an amplifier can be shown to be,

$$A_p = A_v \times A_i \qquad (6\text{-}19)$$

Like current gain, the power gain of a transistor amplifier is largely unimportant for practical applications.

Summary of Typical CE Circuit Performance

Device input impedance	$Z_b \approx h_{ie}$
Circuit input impedance	$Z_i = R_1 \| R_2 \| Z_b$
Device output impedance	$Z_c \approx 1/h_{oe}$
Circuit output impedance	$Z_o \approx R_C \| (1/h_{oe}) \approx R_C$
Circuit voltage gain	$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie}} \approx \frac{-(R_C \| R_L)}{h_{ib}}$

The common-emitter circuit has good voltage gain, with 180° phase shift, medium input impedance, and relatively high output impedance. As a voltage amplifier, the *CE* circuit is by far the most often used of the three basic circuit configurations.

Example 6-6

The transistor parameters in the *CE* circuit in Fig. 6-24 are $h_{ie} = 2.1\ k\Omega$, $h_{fe} = 75$, and $h_{oe} = 1\ \mu S$. Calculate the circuit input impedance, output impedance, and voltage gain. This circuit is designed in Example 5-14.

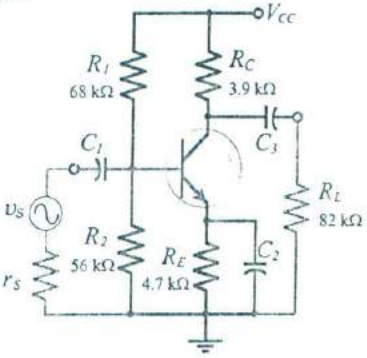


Figure 6-24
CE circuit for Example 6-6. Designed in Example 5-14.

Solution

From Eq. 6-11 and Eq. 6-12,

$$Z_i = R_1 \| R_2 \| h_{ie} = 68\ k\Omega \| 56\ k\Omega \| 2.1\ k\Omega$$
$$= 1.97\ k\Omega$$

Eq. 6-14, $$Z_o = R_C \| (1/h_{oe}) = 3.9\ k\Omega \| (1/1\ \mu S)$$
$$\approx 3.9\ k\Omega$$

Eq. 6-15, $$A_v = \frac{-h_{fe}\,(R_C \| R_L)}{h_{ie}} = \frac{-75 \times (3.9\ k\Omega \| 82\ k\Omega)}{2.1\ k\Omega}$$
$$= -133$$

Example 6-7

A *CE* circuit (as in Fig. 6-24) has $I_C = 1.5$ mA, $R_C = 4.7\ k\Omega$, and $R_L = 56\ k\Omega$. Estimate the value of r'_e, and calculate the circuit voltage gain.

Solution

Eq. 6-2, $$r'_e = \frac{26\ mV}{I_C} \approx \frac{26\ mV}{1.5\ mA}$$
$$= 17.3\ \Omega$$

Eq. 6-16, $$A_v \approx \frac{-(R_C \| R_L)}{h_{ib}} = \frac{-(4.7\ k\Omega \| 56\ k\Omega)}{17.3\ \Omega}$$
$$= -250$$

Practise Problems

6-4.1 Calculate Z_i, Z_o, and A_v for a *CE* circuit (as in Fig. 6-24) with the following quantities: $R_1 = 18\ k\Omega$, $R_2 = 8.2\ k\Omega$, $R_C = 5.6\ k\Omega$, $R_E = 2.7\ k\Omega$, $R_L = 68\ k\Omega$, $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$, $h_{oe} = 1.67\ \mu S$.

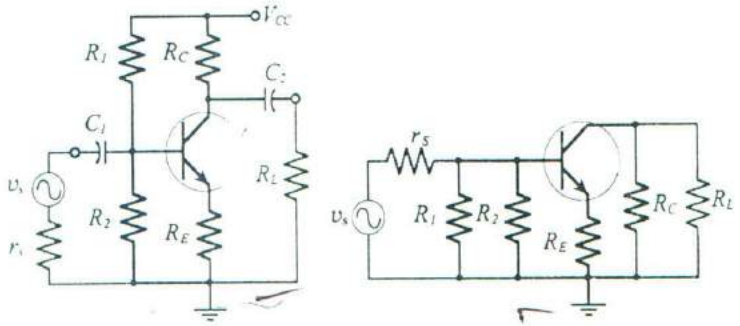
6-4.2 A *CE* circuit has a 0.8 mA emitter current, a 6.8 kΩ collector resistor, and a 68 kΩ capacitor-coupled load. Calculate the circuit voltage gain at 25°C and at 80°C.

6-5 *CE Circuit with Unbypassed Emitter Resistor*

h-parameter Equivalent Circuit

When an unbypassed emitter resistor (R_E) is present in a *CE* circuit, as in Fig. 6-25(a), it is also present in the *ac* equivalent circuit, [Fig. 6-25(b)]. R_E must also be shown in the *h*-parameter circuit between the transistor emitter terminal and the circuit

common input-output terminal, (Fig. 6-26). As with the previous *h*-parameter circuit, the current directions and voltage polarities shown are those that occur when the instantaneous input voltage is positive-going. The presence of R_E without a bypass capacitor significantly affects the circuit input impedance and voltage gain.



(a) Circuit with unbypassed R_E (b) *ac* equivalent circuit

Figure 6-25
CE circuit with unbypassed emitter resistor, and ac equivalent circuit.

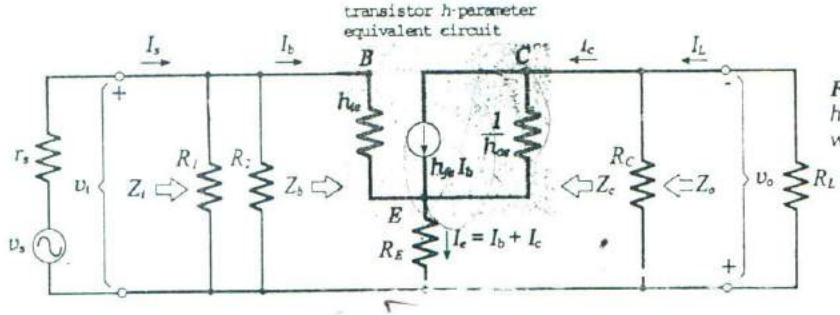


Figure 6-26
h-parameter circuit for CE circuit with unbypassed emitter resistor.

Input Impedance

An equation for the input impedance at the transistor base can be determined from v_i and I_b. From Fig. 6-26,

$$\begin{aligned} v_i &= I_b h_{ie} + I_e R_E \\ &= I_b h_{ie} + R_E(I_b + I_e) \\ &= I_b h_{ie} + R_E(I_b + h_{fe} I_b) \\ &= I_b [h_{ie} + R_E(1 + h_{fe})] \end{aligned}$$

so,
$$Z_b = \frac{v_i}{I_b} = \frac{I_b [h_{ie} + R_E(1 + h_{fe})]}{I_b}$$

or,
$$\boldsymbol{Z_b = h_{ie} + R_E(1 + h_{fe})} \qquad \textbf{(6-20)}$$

Equation 6-20 gives the input impedance at the transistor base terminal. The circuit input impedance is again given by Eq. 6-12,

$$\boldsymbol{Z_i = R_1 \| R_2 \| Z_b}$$

Examination of Eq. 6-20 shows that it is possible to very quickly estimate the input impedance at the transistor base in a *CE* circuit with an unbypassed emitter resistor. For example, a circuit with $R_E = 1\ k\Omega$ and $h_{fe} = 100$, has $Z_b \approx 100\ k\Omega$.

Output Impedance

The output impedance at the transistor collector can be shown to be substantially increased (above $1/h_{oe}$) by the presence of the unbypassed emitter resistor. Consequently, the circuit output impedance should be taken as,

$$Z_o \approx R_C$$

Voltage Gain

From the derivation of the input impedance equation,

$$v_i = I_b[h_{ie} + R_E(1 + h_{fe})]$$

and,

$$v_o = -I_c(R_C \| R_L)$$

so,

$$A_v = \frac{v_o}{v_i} = \frac{-I_c(R_C \| R_L)}{I_b[h_{ie} + R_E(1 + h_{fe})]}$$

giving,

$$\mathbf{A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + R_E(1 + h_{fe})}} \qquad \textbf{(6-21)}$$

Usually,

$$R_E(1 + h_{fe}) >> h_{ie}$$

so,

$$\mathbf{A_v \approx \frac{-(R_C \| R_L)}{R_E}} \qquad \textbf{(6-22)}$$

The voltage gain of a *CE* circuit with an unbypassed emitter resistor can be quickly estimated using Eq. 6-22. For the circuit in Fig. 6-25(a), with $R_C = 4.7\ k\Omega$, $R_E = 1\ k\Omega$, and $R_L >> R_C$, $A_v \approx -4.7$.

Performance Summary for CE Circuit with Unbypassed R_E

Device input impedance	$Z_b = h_{ie} + R_E(1 + h_{fe}) \approx h_{fe} R_E$
Circuit input impedance	$Z_i \approx R_B \| Z_b$ $= R_1 \| R_2 \| Z_b$
Circuit output impedance	$Z_o \approx R_C$
Circuit voltage gain	$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + R_E(1 + h_{fe})}$
Circuit voltage gain	$A_v \approx \frac{-(R_C \| R_L)}{R_E}$

The most significant feature of the performance of a *CE* circuit with an unbypassed emitter resistor is that its voltage gain is much lower than it would be normally. Its input impedance is also much higher than Z_i for a *CE* circuit that has R_E bypassed.

Example 6-8

The *CE* circuit in Fig. 6-27 is the same as in Fig. 6-24, but with bypass capacitor C_3 omitted. The transistor parameters are h_{ie} = 2.1 kΩ, h_{fe} = 75, and h_{oe} = 1 μS, (as in Example 6-6). Calculate the circuit input and output impedance and voltage gain.

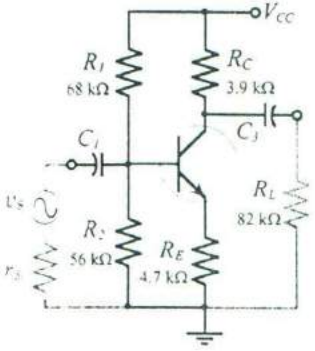


Figure 6-27
CE circuit for Example 6-8.

Solution

From Eq. 6-20, $Z_b = h_{ie} + R_E(1 + h_{fe}) = 2.1\ \text{k}\Omega + 4.7\ \text{k}\Omega(1 + 75)$
$= 359\ \text{k}\Omega$

From Eq. 6-12, $Z_i = R_1 \| R_2 \| Z_b = 68\ \text{k}\Omega \| 56\ \text{k}\Omega \| 359\ \text{k}\Omega$
$= 28.3\ \text{k}\Omega$

$Z_o \approx R_C = 3.9\ \text{k}\Omega$

Eq. 6-21, $$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + R_E(1 + h_{oe})} = \frac{-75 \times (3.9\ \text{k}\Omega \| 82\ \text{k}\Omega)}{2.1\ \text{k}\Omega + 4.7\ \text{k}\Omega(1 + 75)}$$
$= -0.78$

Practise Problems

6-5.1 Calculate Z_i, Z_o, and A_v for a *CE* circuit with an unbypassed emitter resistor (as in Fig. 6-27) with the following component values and parameters: R_1 = 18 kΩ, R_2 = 8.2 kΩ, R_C = 5.6 kΩ, R_E = 2.7 kΩ, R_L = 68 kΩ, h_{ie} = 1 kΩ, h_{fe} = 100, h_{oe} = 1.66 μS.

6-6 *Common-Collector Circuit Analysis*

Common-Collector Circuit

In the *common-collector* (*CC*) circuit shown in Fig. 6-28 the external load (R_L) is capacitor-coupled to the transistor emitter terminal. The circuit uses voltage divider bias to derive the transistor base voltage (V_B) from the supply. The transistor collector terminal is directly connected to V_{CC}; no collector resistor is used. The circuit output voltage is developed across the emitter resistor (R_E), and there is no bypass capacitor.

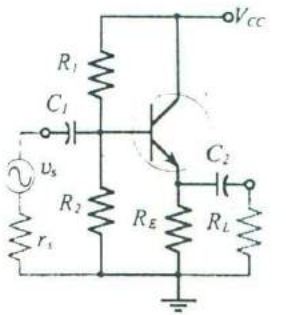


Figure 6-28
Transistor common-collector amplifier circuit, also called an emitter follower.

To understand the operation of a CC circuit, note that V_B is a constant quantity, and that $V_E = V_B - V_{BE}$. When a signal is applied via C_1 to the transistor base, V_B increases and decreases as the signal goes positive and negative. If the signal voltage (υ_s) increases to +0.5 V, V_B is increased by 0.5 V. Also, V_E increases by 0.5 V, because V_{BE} remains substantially constant, and $V_E = V_B - V_{BE}$. The change in V_E is coupled via C_2 to give an *ac* output voltage (υ_o = 0.5 V), (see the waveforms in Fig. 6-29). Similarly, when υ_s decreases to -0.5 V, both V_B and V_E decrease by 0.5 V, giving υ_o = -0.5 V.

It is seen that the *ac* output voltage from a *CC* circuit is essentially the same as the input voltage; there is no voltage gain or phase shift. Thus, the *CC* circuit can be said to have a voltage

gain of 1. (Actually, the output voltage can be shown to be slightly smaller than the input because of a very small change in V_{BE}.)

The fact that the *CC* output voltage follows the changes in signal voltage gives the circuit its other name: *emitter follower.*

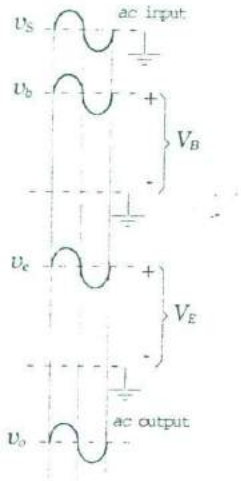
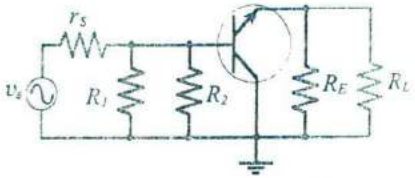


Figure 6-29
Voltage waveforms in a common-collector amplifier circuit.

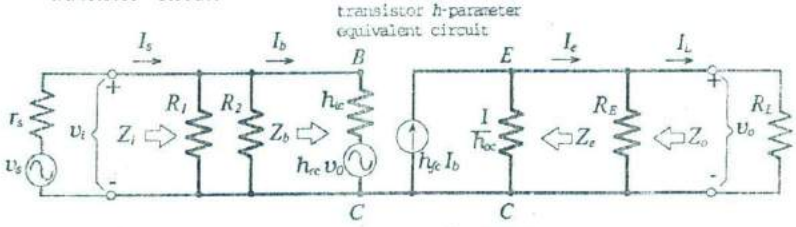
h-Parameter Equivalent Circuit

As for a *CE* circuit, the power supply and capacitors must be replaced with short-circuits to study the *CC ac* performance. This gives the *CC ac* equivalent circuit in Fig. 6-30(a). The input terminals of the *ac* equivalent circuit are seen to be the transistor base and collector, and the output terminals are the emitter and collector. Because the collector terminal is common to both input and output, the circuit configuration is named *common-collector.*

The *CC h*-parameter circuit is now drawn by substituting the transistor *h*-parameter model into the *ac* equivalent circuit, to give the circuit in Fig. 6-30(b). The current directions and voltage polarities indicated in Fig. 6-30(b) are, once again, those that are produced by a positive-going signal voltage. It should be noted that $h_{rc} = 1$ for a *CC* circuit; all of v_o is fed back to the input. So, unlike the case of a *CE* circuit, the feedback generator cannot be omitted in the equivalent circuit of a *CE* amplifier.



(a) *ac* equivalent circuit for *CC* transistor circuit



(b) *h*-parameter equivalent circuit for *CC* circuit

Figure 6-30
Common-collector amplifier ac equivalent circuit and h-parameter circuit.

Input Impedance

The input impedance for the *CC* circuit is determined by first writing an equation for the input voltage. Referring to Fig. 6-30 and Fig. 6-31,

$$\begin{aligned} v_i &= I_b h_{ic} + h_{rc} v_o \\ &= I_b h_{ic} + I_e (R_E \| R_L) \\ &= I_b h_{ic} + h_{fc} I_b (R_E \| R_L) \\ &= I_b [h_{ic} + h_{fc} (R_E \| R_L)] \end{aligned}$$

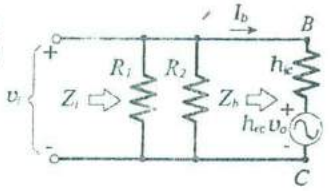


Figure 6-31
Input impedance determination for a CC circuit.

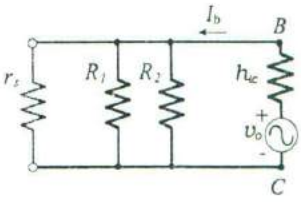
and, $$Z_b = \frac{v_i}{I_b} = \frac{I_b[h_{ic} + h_{fc}(R_E \| R_L)]}{I_b}$$

or, $$\boldsymbol{Z_b = h_{ic} + h_{fc}(R_E \| R_L)} \qquad \textbf{(6-23)}$$

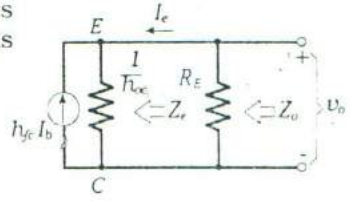
Equation 6-23 is similar to the equation for the transistor input impedance in a *CE* circuit with an unbypassed emitter resistor (Eq. 6-20), except that R_L is now in parallel with R_E. The circuit input impedance is again given by Eq. 6-12.

$$Z_i = R_1 \| R_2 \| Z_b$$

Using Eq. 6-23, the input impedance at the transistor base in a *CC* circuit can be quickly estimated. A circuit with $R_E = 1\ \text{k}\Omega$ and $h_{fe} = 100$, has $Z_b \approx 100\ \text{k}\Omega$ if $R_L >> R_E$.



(a) I_b determination with $v_s = 0$



(b) Z_e and Z_o determination

Figure 6-32
Determination of output impedance for a CC circuit.

Output Impedance

As already discussed, the *ac* voltage at the output of a *CC* circuit is all fed back to the input. This fact is used in determining the output impedance (Z_e) at the emitter terminal. The signal voltage is assumed to be zero, and v_o is used to calculate I_e. With $v_s = 0$, I_b is produced by the fed back voltage ($h_{rc} v_o = v_r$), [see Fig. 6-32(a)].

$$I_b = \frac{v_o}{h_{ic} + (R_1 \| R_2 \| r_s)}$$

and, $$I_e = h_{fc} I_b = \frac{h_{fc}\, v_o}{h_{ic} + (R_1 \| R_2 \| r_s)}$$

$$Z_e = \frac{v_o}{I_e} = \frac{v_o[h_{ic} + (R_1 \| R_2 \| r_s)]}{h_{fc}\, v_o} \qquad \text{[see Fig. 6-32(b)]}$$

so, $$\boldsymbol{Z_e = \frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}} \qquad \textbf{(6-24)}$$

Note that the output impedance at the emitter terminal is

$$\frac{h_{ic} + (Z \text{ in series with the base terminal})}{h_{fc}}$$

It is interesting to compare this to the base input impedance (Eq. 6-23), which is,

$$h_{ic} + h_{fc}\,(Z \text{ in series with the emitter terminal})$$

Equation 6-24 gives the device output impedance. (Actually, $1/h_{oc}$ should be included, but it has a negligible effect on Z_e.) The circuit output impedance also involves R_E, [see Fig. 6-32(b)].

$$\boldsymbol{Z_o = Z_e \| R_E} \qquad \textbf{(6-25)}$$

R_E is usually much larger than Z_e, so that $Z_o \approx Z_e$.

Voltage Gain

As already explained, the *ac* output voltage from a *CC* circuit is

almost exactly equal to the input voltage. However, the precise equation for A_v is easily derived by considering the *ac* output and input voltages as derived from Fig. 6-30(b).

$$v_i = I_b[h_{ic} + h_{fc}(R_E \| R_L)]$$

and,

$$v_o = I_e(R_E \| R_L)$$

so,

$$A_v = \frac{v_o}{v_i} = \frac{I_e(R_E \| R_L)}{I_b[h_{ic} + h_{fc}(R_E \| R_L)]}$$

this reduces to,

$$A_v = \frac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} \qquad \textbf{(6-26)}$$

Because $r'_e \approx h_{ib}$, Eq. 6-26 can be used in situations where the device parameters are unknown. Usually, $R_E \| R_L$ is so much larger than h_{ib} that the *CC* circuit voltage gain is simply taken as,

$$A_v \approx 1 \qquad \textbf{(6-27)}$$

Summary of CC Circuit Performance

Device input impedance	$Z_b = h_{ic} + h_{fc}(R_E \| R_L)$
Circuit input impedance	$Z_i = R_B \| Z_b = R_1 \| R_2 \| Z_b$
Device output impedance	$Z_e = \dfrac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}$
Circuit output impedance	$Z_o = Z_e \| R_E$
Circuit voltage gain	$A_v = \dfrac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} \approx 1$

A *CC* circuit has a voltage gain of 1, no phase shift between input and output, high input impedance, and low output impedance. Because of its high Z_i, low Z_o, and unity gain, the *CC* circuit is normally used as a *buffer amplifier*, placed between a high impedance signal source and a low impedance load.

Example 6-9

The transistor parameters for the CC circuit in Fig. 6-33 are $h_{ie} = 2.1\ k\Omega$ and $h_{fe} = 75$. (a) Calculate the circuit input and output impedance with R_L not connected. (b) Calculate Z_i and A_v with R_L connected.

Solution

(a) *R_L not connected*

From Table 6-1, $h_{ic} = h_{ie} = 2.1\ k\Omega$

and, $h_{fc} = 1 + h_{fe} = 76$

Eq. 6-23, $Z_b = h_{ic} + h_{fc}(R_E \| R_L) = 2.1\ k\Omega + 76(4.7\ k\Omega)$

$= 359.3\ k\Omega$

Eq. 6-12, $Z_i = R_1 \| R_2 \| Z_b = 10\ \text{k}\Omega \| 10\ \text{k}\Omega \| 359.3\ \text{k}\Omega$
$= 4.93\ \text{k}\Omega$

Eq. 6-24, $Z_e = \dfrac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}} = \dfrac{2.1\ \text{k}\Omega + (10\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1\ \text{k}\Omega)}{76}$
$= 38.6\ \Omega$

Eq. 6-25, $Z_o = Z_e \| R_E = 38.6\ \Omega \| 4.7\ \text{k}\Omega$
$= 38.3\ \Omega$

(b) R_L connected

Eq. 6-23, $Z_b = h_{ic} + h_{fc}(R_E \| R_L) = 2.1\ \text{k}\Omega + 76(4.7\ \text{k}\Omega \| 12\ \text{k}\Omega)$
$= 258.8\ \text{k}\Omega$

Eq. 6-12, $Z_i = R_1 \| R_2 \| Z_b = 10\ \text{k}\Omega \| 10\ \text{k}\Omega \| 258.8\ \text{k}\Omega$
$= 4.91\ \text{k}\Omega$

From Table 6-1, $h_{ib} = \dfrac{h_{ie}}{1 + h_{fc}} = \dfrac{2.1\ \text{k}\Omega}{1 + 75}$
$= 27.6\ \Omega$

Eq. 6-26, $A_i = \dfrac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} = \dfrac{(4.7\ \text{k}\Omega \| 12\ \text{k}\Omega)}{27.6\ \Omega + (4.7\ \text{k}\Omega \| 12\ \text{k}\Omega)}$
$= 0.99$

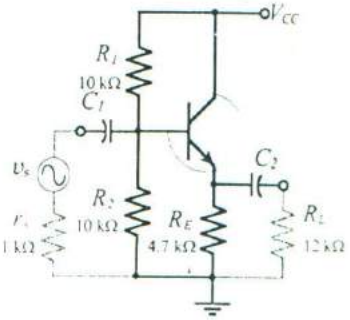


Figure 6-33
CC circuit for Example 6-9.

Practise Problems

6-6.1 Calculate Z_i and Z_o, for a CC circuit (as in Fig. 6-33) with the following component values and parameters: $R_1 = 56\ \text{k}\Omega$, $R_2 = 39\ \text{k}\Omega$, $R_E = 5.6\ \text{k}\Omega$, $R_L = 22\ \text{k}\Omega$, $r_s = 400\ \Omega$, $h_{ie} = 1\ \text{k}\Omega$, $h_{fc} = 100$.

6-7 Common-Base Circuit Analysis

Common-Base Circuit

The common-base (*CB*) circuit in Fig. 6-34 is very similar to a *CE* circuit, except that the input signal is applied to the transistor emitter terminal (via C_2), instead of the base. Also, there is no bypass capacitor across the R_E, but the base terminal is *ac* grounded via capacitor C_1. Because the base is *ac* grounded, all of the signal voltage is developed across the transistor base-emitter junction. As for a *CE* circuit, the output voltage is developed across the collector resistor (R_C).

A positive-going signal voltage at the input of a *CB* circuit pushes the transistor emitter in a positive direction while the base voltage remains fixed. Thus, a positive-going signal reduced the base-emitter voltage, (see the waveforms in Fig. 6-35). The reduction in V_{BE} reduces the transistor collector current, and the I_C reduction reduces V_{RC}, and consequently, causes the transistor collector voltage to increase. The rise in V_C is effectively a rise in the circuit

output voltage (v_o). It is seen that a positive-going input voltage produced a positive-going output. It can also be demonstrated that a negative-going input produces a negative-going output. There is no phase shift from input to output in a *CB* circuit.

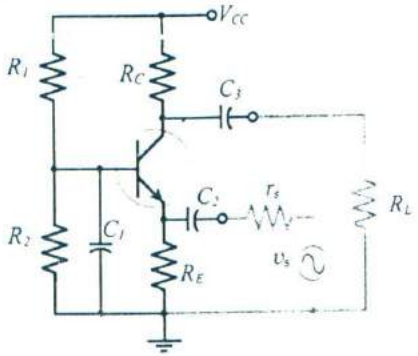


Figure 6-34
In a common-base circuit, the signal is capacitor-coupled to the transistor emitter terminal, and the output is taken from the collector.

h-parameter Equivalent Circuit

The *CB ac* equivalent circuit is drawn, as always, by replacing the supply voltage and capacitors with short circuits. This gives the circuit in Fig. 6-36(a), which shows that the transistor base terminal (grounded via capacitor C_1) is common to both input and output. Hence the name *common base*.

The *CB h*-parameter circuit is now drawn by substituting the transistor *h*-parameter model into the *ac* equivalent circuit, giving the circuit in Fig. 6-36(b). Once again, the current directions and voltage polarities indicated in the *h*-parameter circuit are those produced by a positive-going signal voltage. Note that the feedback voltage generator ($h_{rb}\,v_o$) is not included in the *CB h*-parameter circuit. This is because the feedback voltage effect is so small that it can be neglected when deriving practical approximate equations for the circuit performance. This corresponds with the *CE h*-parameter circuit, but not with the *CC h*-parameter circuit, where the feedback voltage is very important.

Input Impedance

Referring to Fig. 6-36(b), the input impedance to the transistor emitter is simply h_{ib}.

$$Z_e = h_{ib} \qquad \textbf{(6-28)}$$

Typically h_{ib} is around 21 Ω for a low-current transistor. (Also, $h_{ib} \approx r'_e$, see Section 6-3.) Resistor R_E is in parallel with Z_e, so the circuit input impedance is,

$$Z_i = Z_e \| R_E \qquad \textbf{(6-29)}$$

R_E is usually much larger than Z_e, so $Z_i \approx Z_e$.

Output Impedance

'Looking into' the collector terminals of the *CB h*-parameter circuit in Fig. 6-36(b), a very large resistance ($1/h_{ob}$) is seen.

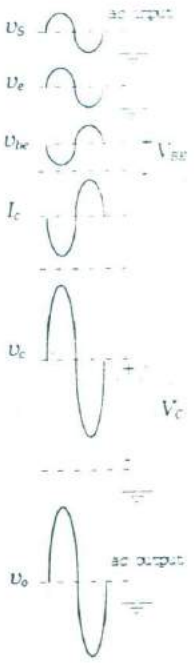


Figure 6-35
Voltage and current waveforms for a common-base amplifier circuit.

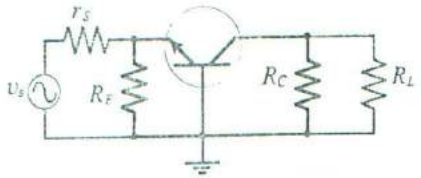
$$Z_c = 1/h_{ob} \tag{6-30}$$

Once again, Z_c is the device output impedance, and the circuit output impedance is R_C in parallel with Z_c.

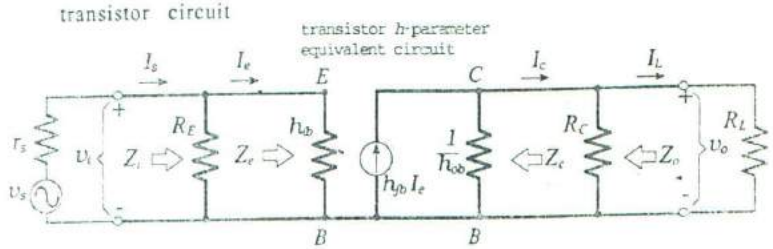
$$Z_o = Z_c \| R_c \tag{6-31}$$

Because Z_c is normally much larger than R_C, $Z_o \approx R_C$.

As in the case of a *CE* circuit, the output impedance of a *CB* circuit can be determined by just reading the resistance of R_C.



(a) *ac* equivalent circuit for *CB* transistor circuit



(b) *h*-parameter equivalent circuit for *CB* circuit

Figure 6-36
Common-base amplifier, ac equivalent circuit, and h-parameter circuit.

Voltage Gain

The input voltage equation for the circuit in Fig. 6-36(b) is,

$$v_i = I_e h_{ib}$$

and the output voltage is,

$$v_o = I_c(R_C \| R_L)$$
$$= h_{fb} I_e (R_C \| R_L)$$

so,
$$A_v = \frac{v_o}{v_i} = \frac{h_{fb} I_e (R_C \| R_L)}{I_e h_{ib}}$$

and,
$$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib}} \tag{6-32}$$

Effect of Unbypassed Base Resistors

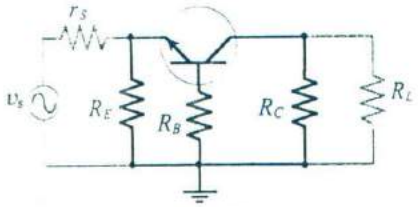
If capacitor C_1 is not present in the *CB* circuit in Fig. 6-34, the transistor base is *not ac* short-circuited to ground. So, a resistance ($R_B = R_1 \| R_2$) must be shown in the *ac* equivalent circuit [Fig. 6-37(a)], and in the *h*-parameter circuit [Fig. 6-37(b)]. The presence of the unbypassed base resistors can substantially affect the transistor input impedance and the circuit voltage gain. Analysis of the *h*-parameter circuit shows that,

$$Z_e = h_{ib} + R_B(1 - h_{fb}) \quad \textbf{(6-33)}$$

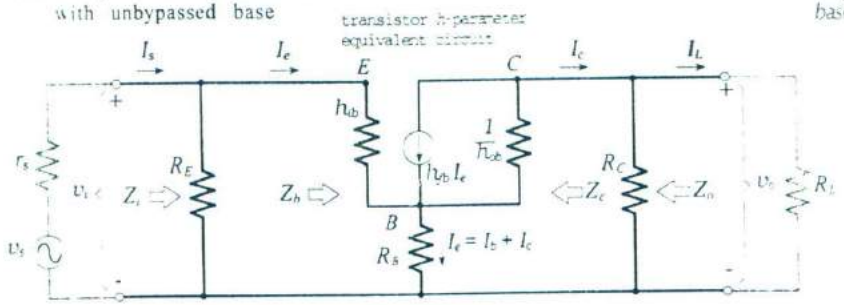
and,

$$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib} + R_B(1 - h_{fb})} \quad \textbf{(6-34)}$$

Comparing Eq. 6-33 to Eq. 6-28 (Z_e with C_1 present), it is seen that $R_B(1 - h_{fb})$ is added to h_{ib} to give Z_e without C_1 present, (Eq. 6-33). Eq. 6-34 is similar to Eq. 6-32 (A_v with C_1 present), except that $R_B(1 - h_{fb})$ is again added to h_{ib} to give the *CB* circuit voltage gain without C_1, (Eq. 6-34). Typically $h_{fb} = 0.99$ and $(1 - h_{fb}) = 0.01$.



(a) *ac* equivalent for *CB* circuit with unbypassed base



(b) *h*-parameter equivalent circuit for *CB* circuit with unbypassed base

Figure 6-37
AC equivalent circuit and h-parameter circuit for a CB amplifier with an unbypassed base resistor.

Summary of CB Circuit Performance

With the base bypassed to ground:

Device input impedance	$Z_e = h_{ib}$
Circuit input impedance	$Z_i = Z_e \| R_E$
Device output impedance	$Z_c = \frac{1}{h_{ob}}$
Circuit output impedance	$Z_o \approx R_c$
Circuit voltage gain	$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib}}$

With the base unbypassed:

Device input impedance	$Z_e = h_{ib} + R_B(1 - h_{fb})$
Circuit voltage gain	$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib} + R_B(1 - h_{fb})}$

A *CB* circuit has good voltage gain and relatively high output impedance, like a *CE* circuit. Unlike a *CE* circuit, a *CB* circuit has a very low input impedance, and this makes it unsuitable for most voltage amplifier applications. It is normally employed only as a high-frequency amplifier. The transistor base terminal in a *CB* circuit should always be bypassed to ground. When this is not done, the input impedance is increased and the voltage amplification is substantially reduced.

Example 6-10

The transistor parameters in the *CB* circuit in Fig. 6-38 are $h_{ie} = 2.1\ \text{k}\Omega$ and $h_{fe} = 75$. Calculate the circuit input and output impedances and voltage gain.

Solution

From Table 6-1, $$h_{ib} = \frac{h_{ie}}{1 + h_{fe}} = \frac{2.1\ \text{k}\Omega}{1 + 75}$$
$$= 27.6\ \Omega$$

and, $$h_{ib} = \frac{h_{fe}}{1 + h_{fe}} = \frac{75}{1 + 75}$$
$$= 0.987$$

Eq. 6-29, $$Z_i = h_{ib} \| R_E = 27.6\ \Omega \| 4.7\ \text{k}\Omega$$
$$= 27.4\ \Omega$$

Eq. 6-31, $$Z_o = (1/h_{ob}) \| R_C \approx R_C$$
$$= 3.9\ \text{k}\Omega$$

Eq. 6-32, $$A_v = \frac{h_{ib}(R_C \| R_L)}{h_{ib}} = \frac{0.987\ (3.9\ \text{k}\Omega \| 82\ \text{k}\Omega)}{27.6\ \Omega}$$
$$= 133$$

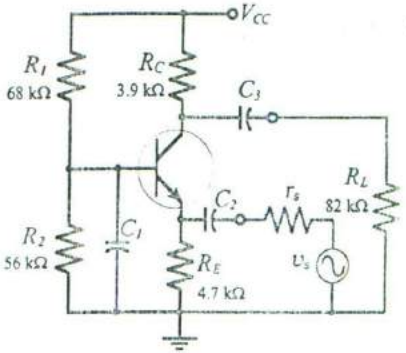


Figure 6-38
CB circuit for Example 6-10.

Example 6-11

Calculate the input impedance and voltage gain for the *CB* circuit in Ex. 6-10 when capacitor C_1 is disconnected.

Solution

Eq. 6-33, $$Z_e = h_{ib} + R_B(1 - h_{fb}) = 27.6\ \Omega + (68\ \text{k}\Omega \| 56\ \text{k}\Omega)(1 - 0.987)$$
$$= 426.8\ \Omega$$

Eq. 6-29, $$Z_i = Z_e \| R_E = 426.8\ \Omega \| 4.7\ \text{k}\Omega$$
$$= 391\ \Omega$$

Eq. 6-34, $$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib} + R_B(1 - h_{fb})} = \frac{0.987\ (3.9\ \text{k}\Omega \| 82\ \text{k}\Omega)}{27.6\ \Omega + (68\ \text{k}\Omega \| 56\ \text{k}\Omega)(1 - 0.987)}$$
$$= 8.6$$

Practise Problems

6-7.1 Calculate Z_i, Z_o, and A_v for a *CB* circuit (as in Fig. 6-38) with the following component values and parameters: $R_1 = 56\ k\Omega$, $R_2 = 39\ k\Omega$, $R_C = 5.6\ k\Omega$, $R_E = 3.3\ k\Omega$, $R_L = 47\ k\Omega$, $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$.

6-7.2 Determine Z_i and A_v for the circuit in Problem 6-7.1 when capacitor C_1 is disconnected.

6-8 Comparison of CE, CC, and CB Circuits

Table 6-2 compares Z_i, Z_o, and A_v for *CE*, *CC*, and *CB* circuits. As already discussed, the *CE* circuit has high voltage gain, medium input impedance, high output impedance, and a 180° phase shift from input to output. The *CC* circuit has high input impedance, low output impedance, a voltage gain of 1, and no phase shift. The *CB* circuit offers low input impedance, high output impedance, high voltage gain, and no phase shift.

Table 6-2 Comparison of common-emitter, common-collector, and common-base circuits.

Circuit configuration	Z_i	Z_o	A_v	Phase shift
CE	*medium*	$\approx R_C$	*high*	*180°*
CC	*high*	*low*	≈ 1	*0*
CB	*low*	$\approx R_C$	*high*	*0*

Device manufacturers normally only list the *CE* *h*-parameters on a transistor data sheet. Although these can be converted to *CC* and *CB* parameters, it is convenient to use *CE* parameters for all three types of circuits. Table 6-3 gives the circuit impedance equations in terms of *CE* *h*-parameters. In the case of input and output impedances, it is helpful to think in terms of the terminal being *looked into*.

Impedance at the Transistor Base

Consideration of each type of circuit shows that the input impedance (Z_i) depends upon which transistor terminal is involved. In both the *CE* and *CC* circuits, the input signal is applied to the transistor base terminal. So, Z_i is the impedance 'looking into' the base. Figure 6-39 shows that, for a *CE* circuit with an unbypassed emitter resistor,

$$Z_b = h_{ie} + R_E(1 + h_{fe})$$

When R_E is bypassed, the $R_E(1 + h_{fe})$ portion can be treated as zero, so that,

$$Z_b = h_{ie}$$

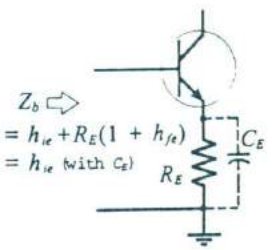


Figure 6-39
Impedance at the transistor base terminal.

The *CC* equations for Z_b are almost identical to the *CE* equations, except that they use h_{ic} and h_{fc}, which are essentially equal to h_{ie} and h_{fe}. (see Table 6-3). A rough approximation for the base input impedance of any transistor circuit with an unbypassed emitter resistor is,

$$Z_b \approx h_{fe}(\textit{impedance in series with the emitter})$$

The circuit input impedance for both *CE* and *CC* configurations is Z_b in parallel with the bias resistors,

$$Z_i = Z_b \| R_1 \| R_2$$

Table 6-3 Common-emitter, common-collector, and common-base circuit equations using *CE h*-parameters.

Circuit configuration	Z_b	Z_e	Z_c
CE	h_{ie}	—	$1/h_{oe}$
CE with unbypassed R_E	$h_{ie} + R_E(1 + h_{fe})$	—	$1/h_{oe}$
CC	$h_{ie} + (R_E \| R_L)(1 + h_{fe})$	$\dfrac{h_{ie} + R_B}{1 + h_{fe}}$	—
CB	–	$\dfrac{h_{ie}}{1 + h_{fe}}$	$\dfrac{1 + h_{fe}}{h_{oe}}$
CB with unbypassed R_B	–	$\dfrac{h_{ie} + R_B}{1 + h_{fe}}$	$\dfrac{1 + h_{fe}}{h_{oe}}$

Impedance at the Transistor Emitter

The transistor emitter is the output terminal for a *CC* circuit and the input terminal for a *CB* circuit. So, the device impedance in each case is the impedance 'looking into' the transistor emitter terminal (Z_e). Although the Z_e equations for the two circuits look different, they can be shown to give exactly the same result in similar situations. For a *CC* circuit or a *CB* circuit with an unbypassed base (using *CE* parameters),

$$Z_e = \frac{h_{ie} + R_B}{1 + h_{fe}}$$

where R_B is the impedance 'looking back' from the transistor base.

As shown in Fig. 6-40, R_B includes the signal source resistance (r_s) for a *CC* circuit. A *CB* circuit normally has its base bypassed as shown, so that the impedance at the emitter is,

$$Z_e = \frac{h_{ie}}{1 + h_{fe}}$$

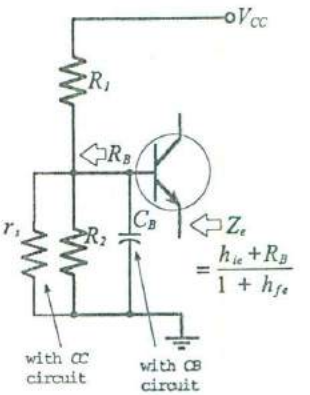


Figure 6-40 Impedance at the transistor emitter terminal.

For all circuit arrangements, the impedance at the transistor emitter terminal is,

$$Z_e = \frac{\text{Impedance in series with the base}}{1 + h_{fe}}$$

Impedance at the Transistor Collector

The output for *CE* and *CB* circuits is produced at the transistor collector terminal. So, the impedance 'looking into' the collector is the device output impedance. This is normally a very large quantity at low and medium signal frequencies. As illustrated in Fig. 6-41, the circuit output impedance at the collector is essentially,

$$Z_o \approx R_C$$

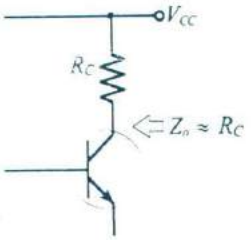


Figure 6-41
Impedance at the transistor collector terminal.

Voltage gain

In the case of a circuit with an unbypassed emitter resistor, the *ac* voltage at the emitter follows the *ac* input at the transistor base. So, a *CC* circuit (an emitter follower) has a voltage gain of 1.

With both *CE* and *CB* circuits, the *ac* input (v_i) is developed across the base-emitter junction, and the *ac* output (v_o) is produced at the transistor collector terminal, (see Fig 6-42). Thus, the magnitude of the voltage gain is the same for *CB* and *CE* circuits with similar component values and transistor parameters. The *CE* voltage gain equation can be used for the *CB* circuit, with the omission of the minus sign that indicates *CE* phase inversion.

Although the voltages gains are equal for similar *CB* and *CE* circuits, the low input impedance of the *CB* circuit can substantially attenuate the signal voltage, and result in a low amplitude output. This is demonstrated in Example 6-12.

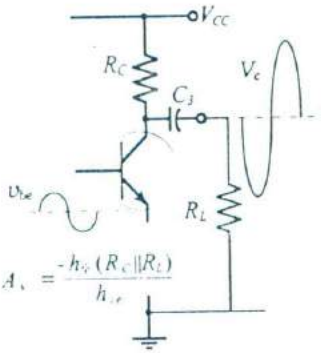


Figure 6-42
CE and CB voltage gain.

Example 6-12

A 50 mV signal with a 600 Ω source resistance is applied to the circuit in Fig. 6-43. Calculate v_o for: (a) *CE* circuit operation with v_s at the transistor base, and R_E bypassed. (b) *CB* circuit operation with v_s at the emitter, and the base resistors bypassed. The transistor parameters are h_{ie} = 1.5 kΩ and h_{fe} = 100.

Solution

(a) *CE circuit*

$$A_v = \frac{h_{fe}(R_C \| R_L)}{h_{ie}} = \frac{100\ (5.6\ \text{k}\Omega \| 33\ \text{k}\Omega)}{1.5\ \text{k}\Omega}$$

$$= 319$$

$$Z_b = h_{ie} = 1\ \text{k}\Omega$$

$$Z_i = Z_b \| R_1 \| R_2 = 1\ \text{k}\Omega \| 100\ \text{k}\Omega \| 47\ \text{k}\Omega$$

$$= 970\ \Omega$$

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} = \frac{50\ \text{mV} \times 970\ \Omega}{600\ \Omega + 970\ \Omega}$$

$$= 30.9\ \text{mV}$$

$$v_o = A_v \times v_i = 319 \times 30.9 \text{ mV}$$
$$= 9.9 \text{ V}$$

(b) *CB circuit*

$$A_v = \frac{h_{fe}(R_C \| R_L)}{h_{ie}} = 319$$

from Table 6-3, $$Z_e = \frac{h_{ie}}{1 + h_{fe}} = \frac{1.5 \text{ k}\Omega}{1 + 100}$$
$$= 14.85 \ \Omega$$

$$Z_i = Z_e \| R_E = 14.85 \ \Omega \| 5.6 \text{ k}\Omega$$
$$= 14.81 \ \Omega$$

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} = \frac{50 \text{ mV} \times 14.81 \ \Omega}{600 \ \Omega + 14.81 \ \Omega}$$
$$= 1.2 \text{ mV}$$

$$v_o = A_v \times v_i = 319 \times 1.2 \text{ mV}$$
$$= 383 \text{ mV}$$

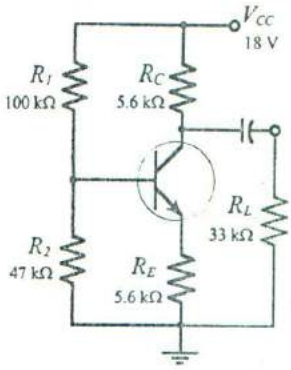


Figure 6-43
Circuit for Example 6-12.

Practise Problems

6-8.1 Using the appropriate *CE* equations from Table 6-3, calculate Z_i, Z_o, and A_v for a *CB* circuit (as in Fig. 6-38) with the following component values and parameters: $R_1 = 56 \text{ k}\Omega$, $R_2 = 39 \text{ k}\Omega$, $R_C = 5.6 \text{ k}\Omega$, $R_E = 3.3 \text{ k}\Omega$, $R_L = 47 \text{ k}\Omega$, $h_{ie} = 1 \text{ k}\Omega$, $h_{fe} = 100$.

6-8.2 Determine v_o for the circuit in Problem 6-8.1 when a 30 mV *ac* signal with $r_s = 400 \ \Omega$ is capacitor-coupled to the transistor emitter.

Chapter-6 Review Questions

Section 6-1

6-1 Sketch the circuit of a *CE* amplifier with a capacitor-coupled signal source and capacitor-coupled load. Explain the need for coupling capacitors, and discuss the correct polarity for connecting the capacitors.

6-2 Explain what is meant by *ac* degeneration in a transistor circuit. Show how *ac* degeneration is eliminated in voltage divider bias and collector-to-base bias circuits.

Section 6-2

6-3 Sketch the *ac* equivalent circuit for a *CE* circuit with voltage divider bias, a bypassed emitter resistor, a capacitor-coupled signal source, and a capacitor-coupled load. Briefly explain.

6-4 Sketch the *ac* equivalent circuit for a *CE* circuit with collector-to-base bias [as in Fig. 6-3(a)], a capacitor-coupled signal source, and a capacitor-coupled load. Briefly explain.

6-5 Discuss the purpose of an *ac* load line for a transistor circuit. State how *ac* load lines differ from *dc* load lines for circuits with bypassed emitter resistors, and for circuits with capacitor-coupled loads.

Section 6-3

6-6 Sketch the *T*-equivalent (*r*-parameter) circuit for a transistor connected in *CB* configuration. Identify each component of the circuit and discuss its origin. Also, sketch a simplified form of the transistor low-frequency equivalent circuit.

6-7 Sketch the *h*-parameter equivalent circuit for a transistor connected in *CE* configuration. Identify each component of the circuit and discuss its origin.

6-8 Define h_{ie}, h_{fe}, h_{oe}, and h_{FE}, and show how each parameter may be derived from the transistor characteristics. Also, state typical *h*-parameter values for a low-current transistor.

6-9 Sketch an approximate *h*-parameter *CE* transistor model that may be used for most purposes. Briefly explain.

6-10 Draw a *CE* transistor hybrid-π model. Briefly explain.

6-11 Define r'_e, and write equations for calculating r'_e at 25°C, and at other temperatures.

Section 6-4

6-12 Briefly explain the operation of the *CE* circuit described in Question 6-3.

6-13 Draw an *h*-parameter equivalent circuit for the *CE* circuit described in Question 6-3. Identify all components.

6-14 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-13.

6-15 Draw an *h*-parameter equivalent circuit for the *CE* circuit described in Question 6-4. Identify all components.

6-16 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-15.

6-17 Sketch a base-biased *pnp* transistor *CE* circuit. Include a capacitor-coupled signal source and load resistor. Draw the *h*-parameter equivalent circuit identifying all components.

6-18 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-17.

Section 6-5

6-19 Referring to the *CE* circuit described in Question 6-3, explain the effect of removing the bypass capacitor from R_E.

6-20 Draw an *h*-parameter equivalent circuit for the *CE* circuit in Question 6-19.

6-21 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-20.

6-22 Sketch a collector-to-base biased *pnp* transistor *CE* circuit with two center-bypassed base resistors and an unbypassed emitter resistor. Include a capacitor-coupled signal source and load resistor. Draw the *h*-parameter equivalent circuit identifying all components.

6-23 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-22.

Section 6-6

6-24 Sketch a practical *npn* transistor *CC* circuit that uses base bias. Include a capacitor-coupled signal source and load resistor. Explain the circuit operation.

6-25 Draw the *h*-parameter equivalent circuit for the circuit in Question 6-24. Identify all components.

6-26 Write equations for Z_i, Z_o, and A_v for the *h*-parameter circuit in Question 6-25.

6-27 Sketch the *h*-parameter equivalent for a *CC* circuit with voltage divider bias, a capacitor-coupled signal source, and a capacitor-coupled load.

6-28 Write the Z_i and Z_o equations for the *h*-parameter circuit in Question 6-27.

6-29 Sketch a base-biased *pnp* transistor *CC* circuit. Include a capacitor-coupled signal source and load resistor.

6-30 Draw the *h*-parameter equivalent circuit for the circuit in Question 6-29.

Section 6-7

6-31 Sketch a practical *npn* transistor *CB* circuit that uses collector-to-base bias. Include a capacitor-coupled signal source and load resistor. Explain the circuit operation.

6-32 Draw the *h*-parameter equivalent circuit for the circuit in Question 6-31. Identify all components.

6-33 Write equations for Z_i, Z_o, and A_v for the *CB* *h*-parameter circuit in Question 6-32.

6-34 Sketch a practical *pnp* transistor *CB* circuit that uses voltage divider bias. Include a capacitor-coupled signal source and load resistor.

6-35 Sketch the *h*-parameter equivalent for a *CB* circuit with voltage divider bias, a capacitor-coupled signal source, and a capacitor-coupled load.

6-36 Write the Z_i, Z_o, and A_v equations for the *CB* *h*-parameter circuit in Question 6-35.

Section 6-8

6-37 Compare the performance of *CE*, *CC*, and *CB* circuits, and discuss typical applications of each type of circuit.

6-38 Write equations for the impedances 'seen looking into' the base, emitter, and collector terminals of a transistor in a circuit. Briefly explain each equation.

Chapter-6 Problems

Section 6-1

6-1 Calculate V_{CE} for the circuit in Fig. 6-43 when the load is capacitor-coupled, as shown, and when the load is directly connected to the collector terminal.

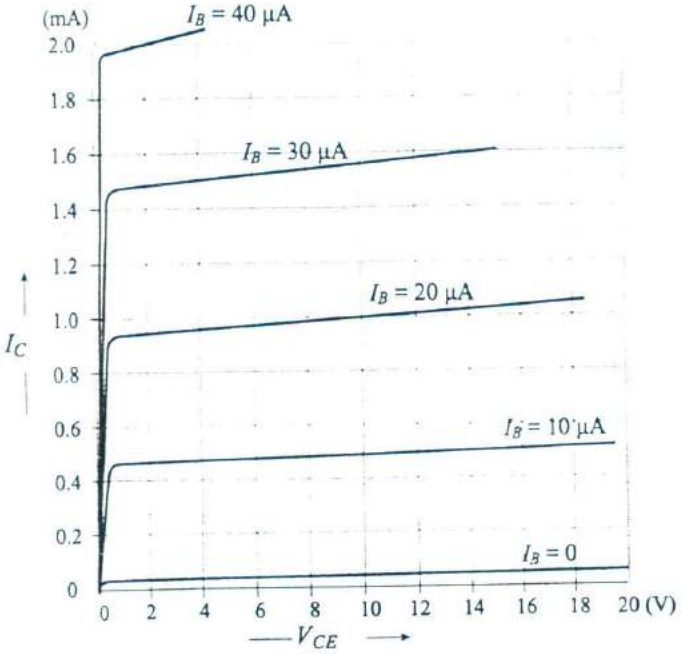


Figure 6-44

6-2 Determine V_B for the circuit in Fig. 6-43 when a 600 Ω signal source is capacitor-coupled to the input, and when the signal source is directly connected.

Section 6-2

6-3 The transistor characteristics for the circuit in Fig. 6-43 are shown in Fig. 6-44. Draw the *dc* and *ac* load lines for the circuit when it is operated in *CE* configuration with R_E bypassed. Also, determine the maximum possible symmetrical output voltage swing.

6-4 Draw the new *ac* load line for the circuit in Problem 6-3 when R_L is changed to 12 kΩ.

6-5 Using the device characteristics in Fig. 6-44, draw the *dc* and *ac* load lines for the *CE* circuit shown in Fig. 6-45.

6-6 The *CE* circuit in Fig. 6-46 uses collector-to-base bias with a bypass capacitor. Draw the *dc* and *ac* load lines for the circuit using the device characteristics in Fig. 6-44. The transistor has $h_{FE} = 100$.

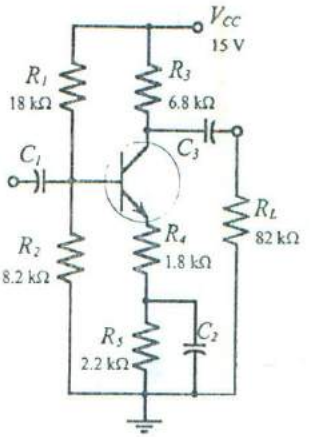


Figure 6-45

Section 6-3

6-7 Referring to the *CE* input and output characteristics in Figs. 4-27 and 4-28, determine h_{ie}, h_{oe}, and h_{fe} for $V_{CE} = 6$ V, and $I_B = 40$ μA.

6-8 A transistor in a *CE* circuit has a constant I_B level of 40 μA. When $V_{CE} = 5$ V, I_C is measured as 4.9 mA, and when V_{CE} is adjusted to 10 V, I_C becomes 5 mA. Calculate h_{oe} and h_{FE}.

6-9 A transistor has V_{CE} maintained constant at 7.5 V, and I_C measured at several levels of I_B as follows:

I_B	25	50	75	100	(μA)
I_C	3.06	6.12	9.2	12.3	(mA)

Determine the h_{fe} value for the transistor.

6-10 The transistor in Problem 6-9 has V_{CE} maintained constant at 7.5 V, and I_B measured at several levels of V_{BE} as follows:

V_{BE}	0.68	0.72	0.76	0.8	(V)
I_B	20	40	60	80	(μA)

Determine the h_{ie} value for the transistor.

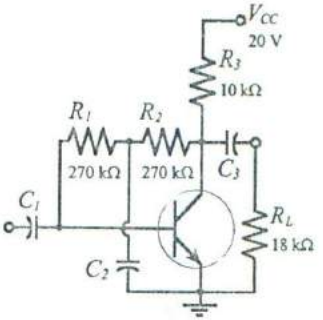


Figure 6-46

6-11 The transistor in Problems 6-9 and 6-10 has I_B maintained constant at 40 μA, and corresponding levels of I_C and V_{CE} measured as follows:

V_{CE}	2	4	6	8	(V)
I_C	4.7	4.8	4.9	5	(mA)

Determine the h_{oe} value for the transistor.

6-12 Calculate α and r_c for the transistor referred to in Problems 6-9 through 6-11.

6-13 Determine the value of r'_e for a transistor with a 2 mA emitter current if its junction temperature is 80°C.

6-14 The collector and base currents of a transistor are measured as 1.28 mA and 20 μA, respectively. Calculate r'_e, h_{ie}, and r_π for the transistor.

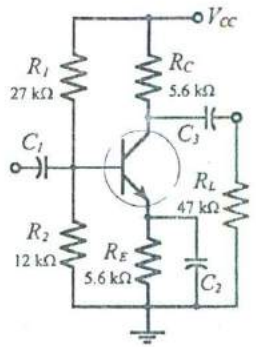


Figure 6-47

Section 6-4

6-15 The *CE* circuit in Fig. 6-47 has the following transistor parameters: $h_{ie} = 1$ kΩ, $h_{fe} = 85$, $h_{oe} = 2$ μS. Calculate Z_i, Z_o, and A_v.

6-16 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 6-15 when the transistor is replaced with one having $h_{ie} = 1.4\ k\Omega$ and $h_{fe} = 55$.

6-17 The base biased *CE* circuit in Fig. 6-48 has the following transistor parameters: $h_{ie} = 1.3\ k\Omega$, $h_{fe} = 40$, $h_{oe} = 1.5\ \mu S$. Calculate Z_i, Z_o, and A_v.

6-18 The collector-to-base biased *CE* circuit in Fig. 6.49 has the following transistor parameters: $h_{ie} = 1.3\ k\Omega$, $h_{fe} = 40$, $h_{oe} = 1.5\ \mu S$. Calculate Z_i, Z_o, and A_v.

6-19 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 6-17 when the transistor is replaced with one having $h_{ie} = 1.5\ k\Omega$, $h_{oe} = 1\ \mu S$, and $h_{fe} = 100$.

6-20 The transistor in the circuit in Problem 6-18 is replaced with one having $h_{ie} = 1.5\ k\Omega$, $h_{oe} = 1\ \mu S$, and $h_{fe} = 100$. Recalculate Z_i, Z_o, and A_v.

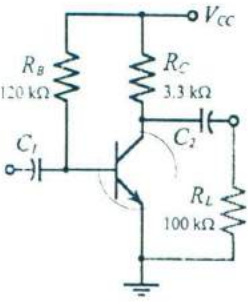


Figure 6-48

Section 6-5

6-21 For the circuit in Problem 6-15, recalculate Z_i and A_v when the bypass capacitor is removed from R_E.

6-22 The circuit in Problem 6-15 has R_E replaced with two series-connected resistors, $R_{E1} = 1.5\ k\Omega$, and $R_{E2} = 3.9\ k\Omega$. Calculate Z_i, and A_v when only R_{E1} is capacitor-bypassed, and when only R_{E2} is capacitor-bypassed.

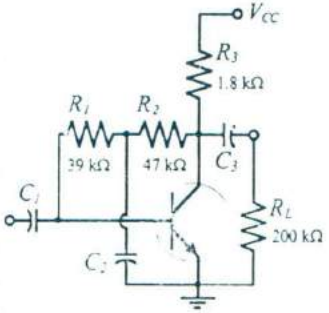


Figure 6-49

Section 6-6

6-23 The transistor parameters for the *CC* circuit in Fig. 6-50 are: $h_{ie} = 1\ k\Omega$, $h_{fe} = 85$, $h_{oe} = 2\ \mu S$. Calculate Z_i and Z_o.

6-24 Recalculate Z_i and Z_o for Problem 6-23 when the transistor is replaced with one having $h_{ie} = 1.4\ k\Omega$ and $h_{fe} = 55$.

6-25 The *CC* circuit in Fig. 6-51 has the following transistor parameters: $h_{ie} = 1.3\ k\Omega$ and $h_{fe} = 40$. Calculate Z_i and Z_o.

6-26 A *CC* circuit using voltage divider bias (as in Fig. 6-50) has the following component values: $R_1 = 33\ k\Omega$, $R_2 = 47\ k\Omega$, $R_E = 15\ k\Omega$, $R_L = 47\ k\Omega$. The transistor parameters are: $h_{ie} = 1.2\ k\Omega$ and $h_{fe} = 120$. Calculate Z_i and Z_o.

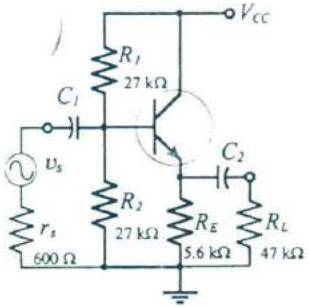


Figure 6-50

Section 6-7

6-27 The *CB* circuit in Fig. 6-52 has a transistor with the following parameters: $h_{ie} = 1\ k\Omega$, $h_{fe} = 85$, $h_{oe} = 2\ \mu S$. Calculate Z_i, Z_o, and A_v.

6-28 Recalculate Z_i and A_v for the *CB* circuit in Problem 6-27 when the transistor is replaced with one having $h_{ie} = 1.4\ k\Omega$ and $h_{fe} = 55$.

6-29 Calculate Z_i, Z_o, and A_v for the *CB* circuit in Fig. 6-53. The transistor parameters are: $h_{ie} = 1.3\ k\Omega$, $h_{fe} = 40$, $h_{oe} = 1.5\ \mu S$.

6-30 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 6-29 when the transistor is replaced with one having $h_{ie} = 1.5$ kΩ, $h_{oe} = 1$ μS, and $h_{fe} = 100$.

6-31 A *CB* circuit (as in Fig. 6-52) has the following component values and transistor parameters: $R_1 = 33$ kΩ, $R_2 = 22$ kΩ, $R_C = 3.3$ kΩ, $R_E = 3.9$ kΩ, $R_L = 39$ kΩ, $h_{ie} = 1.6$ kΩ, $h_{fe} = 200$, $h_{oe} = 1.5$ μS. Calculate Z_i, Z_o, and A_v.

Section 6-8

6-32 The transistor in the *CE* circuit in Problem 6-15 is replaced with a *2N3904* transistor (see Appendix 1-5). Calculate the maximum and minimum values of Z_i, Z_o, and A_v.

6-33 The *CC* circuit in Problem 6-23 is reconstructed to use a *2N3903* transistor. Calculate the maximum and minimum values of Z_i and Z_o.

6-34 The transistor in the *CB* circuit in Problem 6-31 is replaced with a *2N3903* transistor. Calculate the maximum and minimum values of Z_i and Z_o.

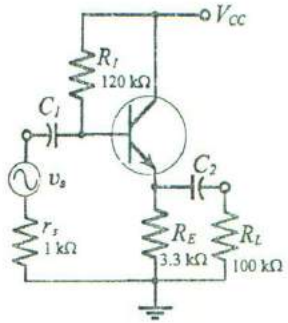


Figure 6-51

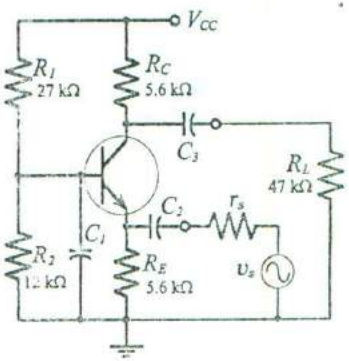


Figure 6-52

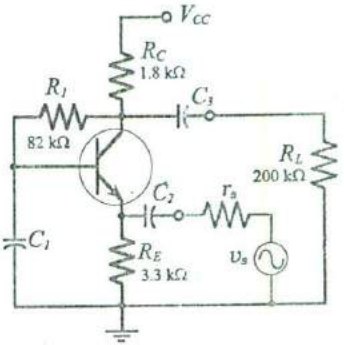


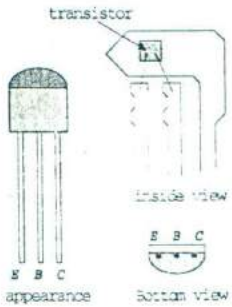
Figure 6-53

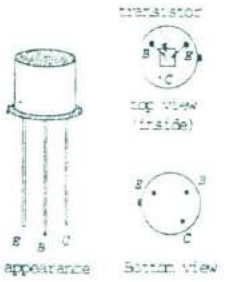
Practise Problem Answers

6-1.1 9.5 V, 8.9 V
6-2.1 point C at 2.07 mA and 3.3 V from Q
6-3.1 133, 20 μS
6-3.2 0.993, 6.7 MΩ
6-3.3 1.76 kΩ
6-4.1 849 Ω, 5.6 kΩ, -517
6-4.2 190, 161
6-5.1 5.52 kΩ, 5.6 kΩ, -1.87
6-6.1 21.9 kΩ, 14 Ω
6-7.1 9.87 Ω, 5.6 kΩ, 500
6-7.2 224 Ω, 20.6
6-8.1 9.87 Ω, 5.6 kΩ, 500
6-8.2 361 mV

Chapter 7

Semiconductor Device and IC Fabrication





Chapter Contents

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7-2 *Diode Fabrication and Packaging* 213
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Review Questions 223

Objectives

You will be able to:

1. *Describe the process of preparing semiconductor material for device manufacture, and explain diffusion and epitaxial growth.*
2. *Draw sketches to show the fabrication of alloy and diffused diodes.*
3. *Explain the manufacturing requirements for transistors to produce satisfactory current gain, frequency response, power dissipation, etc.*
4. *Describe the various transistor fabrication methods and their performance characteristics.*
5. *Discuss manufacturing methods for the production of integrated circuits.*
6. *Draw sketches to show the construction of monolithic IC components, and discuss problems that occur with the use of IC components.*
7. *Sketch various diode, transistor, and IC packages, and show the terminal identification systems.*

Introduction

The method employed to manufacture a semiconductor device determines its electrical characteristics and, thus, dictates its applications. For example, low-current fast-switching diodes and transistors must be fabricated differently from high-power devices. The process that produces a transistor with high current gain may result in undesirable large junction capacitances. Also, a technique that gives a small junction capacitance might produce devices with low breakdown voltages. An *integrated circuit (IC)* consists of many transistors, diodes, and other components in one package. Usually, all of the components are fabricated on one small silicon chip.

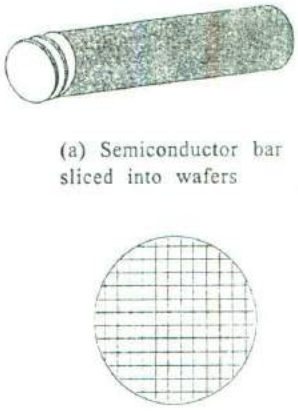
7-1 Processing of Semiconductor Materials

Preparation of Silicon and Germanium

Silicon is one of the commonest elements on earth. It occurs as silicon dioxide (SiO_2) and as silicates; mixtures of silicon and other materials. Germanium is derived from zinc or copper ores. When converted to bulk metal, silicon and germanium contain large quantities of impurities. Both metals must be carefully refined before they can be used for semiconductor device manufacture.

Semiconductor material is normally *polycrystalline* after it is refined. This means that it is made up of many individual formations of atoms with no overall fixed pattern. For use in semiconductors, the metal must be converted into *single-crystal* material; that is, all of its atoms must be arranged into a single pattern.

In its final condition for device manufacture, silicon and germanium are in the form of single-crystal bars about 2.5 cm in diameter and perhaps 30 cm long. The bars are sliced into disc-shaped wafers about 0.4 cm thick, and the wafers are polished to a mirror surface. Several thousand devices are usually fabricated on the surface of each wafer, then the wafers are scribed and cut like glass, (see Fig. 7-1).



(a) Semiconductor bar sliced into wafers

(b) Scribed wafer

Figure 7-1
Bars of single-crystal semiconductor material are sliced into wafers for device manufacture.

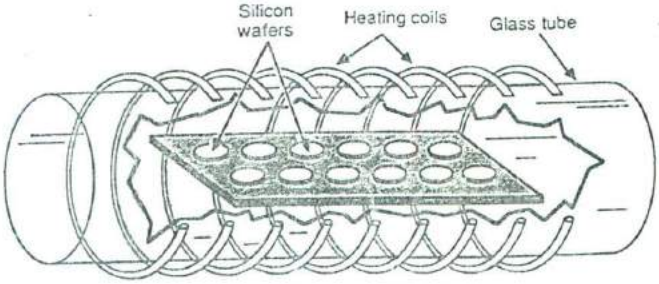


Figure 7-2
Semiconductor wafers are heated in an atmosphere containing n-type or p-type impurities which diffuse into the surface of the wafers.

Diffusion

For processing, semiconductor wafers contained in an enclosure are heated by means of *radio frequency* (*RF*) heating coils. This is illustrated in Fig. 7-2. When wafers of *n*-type material are raised to a high temperature in an atmosphere containing *p*-type impurity atoms some of the impurities *diffuse* into each wafer. This converts the outer layer of the *n*-type material into *p*-type. (Fig 7-3). The diffusion process can be continued by further heating the wafers in an atmosphere containing *n*-type impurity atoms, so that *npn* layers are produced, as illustrated. Because the diffusion process is very slow (about 2.5 μm per hour), very narrow diffused regions can be created by careful timing.

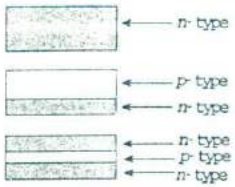


Figure 7-3
The diffusion process converts n-type semiconductor into p-type, and vice versa.

Epitaxial Growth

The *epitaxial* process is very similar to the diffusion process, except that silicon or germanium atoms are contained in the gas surrounding the semiconductor wafers. The semiconductor atoms in the gas *grow* (accumulate) on the wafer in the form of a thin layer, (Fig. 7-4). This layer is single-crystal material and it may be *p*-type or *n*-type, according to the impurity content of the gas. The epitaxial layer may be doped by the diffusion process.

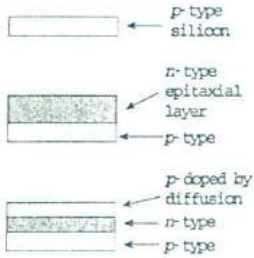


Figure 7-4
Epitaxial growth adds layers of n-type or p-type material on the surface of a wafer.

Section 7-1 Review

7-1.1 Briefly explain polycrystalline material, single-crystal material, diffusion, and epitaxial growth.

7-2 Diode Fabrication and Packaging

Alloy and Diffused Diodes

Two commonly used techniques for diode manufacture are the *alloy* method and the *diffusion* method. To construct an alloy diode, a *pn*-junction is formed by melting a tiny pellet of aluminum (or some other *p*-type impurity) on the surface of an *n*-type crystal. Alternatively, an *n*-type impurity may be melted on the surface of a *p*-type crystal. The process is illustrated in Fig. 7-5(a).

Figure 7-5(b) shows the diffusion technique for diode construction. When an *n*-type semiconductor is heated in a chamber containing an acceptor impurity in vapour form, some of the acceptor atoms are diffused (or absorbed) into the *n*-type crystal. This produces a *p*-region in the *n*-type material and thus creates a *pn*-junction. The size of the *p*-region can be precisely defined by uncovering only part of the *n*-type material during the diffusion process, (the rest of the surface has a thin coating of silicon dioxide). Metal contacts are electroplated on to each region for connecting leads.

The diffusion technique lends itself to the simultaneous fabrication of many hundreds of diodes on one small disc of semiconductor material. This process is also used in the production of transistors and integrated circuits.

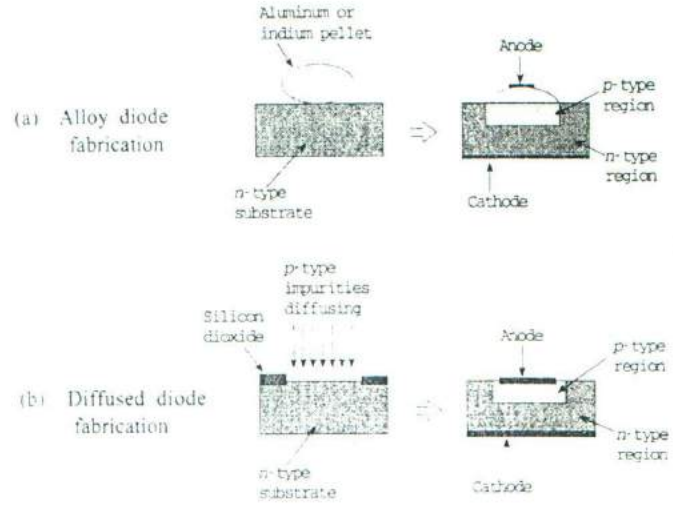


Figure 7-5
Diode fabrication methods. For the alloy diode, a pellet containing p-type impurities is melted into n-type material. A diffused diode is created by heating a wafer of n-type material in an atmosphere containing p-type impurities.

Diode Packaging

As discussed in Section 2-1, semiconductor diodes vary widely in size, depending on their application. Figure 7-6 shows typical single diode packages for low, medium, and high current devices. In Fig. 7-7 multiple diode packages are illustrated. Two diodes in a surface mount package (see Section 7-7) are shown in Fig. 7-7(a), and two in a power-transistor-type package are illustrated in Fig. 7-7(b). Note from the circuits that the cathode terminals are internally commoned in each case.

A rectifier assembly is shown in Fig. 7-7(c). This is four diodes connected to function as a bridge rectifier and contained in one package. One side of the package has a metal plate for mounting on a heat sink (see Section 8-8). The two output terminals are identified as + and -, and the other two terminals are for the *ac* input.

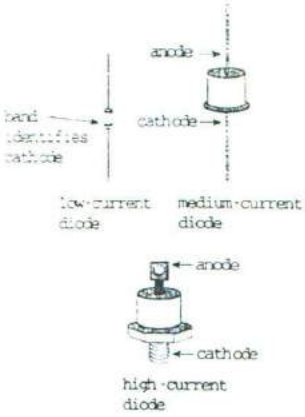


Figure 7-6
Individual diodes vary in size according to the current they are required to pass.

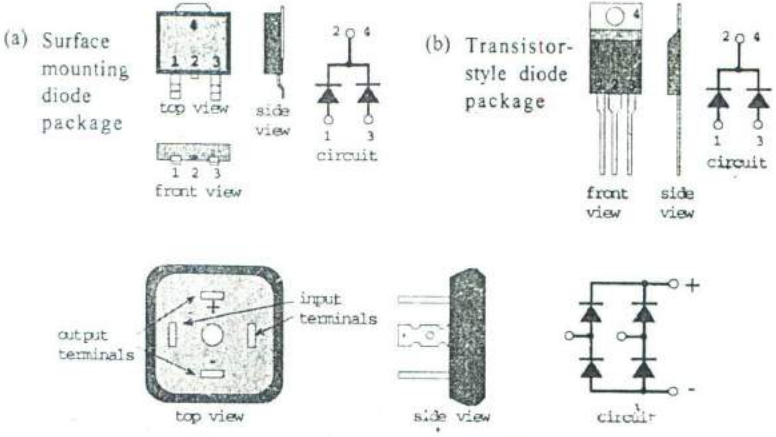


Figure 7-7
Some multiple diode packages

Section 7-2 Review

7-2.1 Briefly describe the construction of alloy diodes and diffused diodes.

7-3 Transistor Construction and Performance

Current Gain

Good current gain requires that most charge carriers from the emitter pass rapidly to the collector. So, there should be little outflow of charge carriers via the base terminal, and there should be few carrier recombinations within the base. These conditions dictate a very narrow, lightly doped, base, (see Fig. 7-8).

High Power

High-power transistors must have large emitter-base surfaces to provide the required quantity of charge carriers. Large collector-base surfaces are also required to dissipate power without overheating the collector-base junction, (Fig. 7-8).

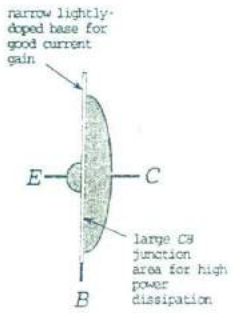


Figure 7-8
High current gain requires a narrow lightly-doped transistor base, and high power dissipation demands a large CB junction area.

Frequency Response

For the highest possible frequency response, the transistor base region must be very narrow to ensure a short transit time of charge carriers from emitter to collector, (see Fig. 7-9). Input capacitance must also be kept to a minimum, and this requires a small area emitter-base junction as well as a highly-resistive (lightly doped) base region.

Because power transistors require large junction surfaces, and high-frequency performance demands small junction areas, there is a conflict in high-frequency power transistors. To keep the junction area to a minimum and still provide adequate charge-carrier emission, the emitter-base junction is usually in the form of a long thin zig-zag strip.

Switching Transistors

Fast switching demands the same low junction capacitance required for good high-frequency performance. A switching transistor should have a low *saturation voltage* and a short *storage time*, (see Section 8-5). For low saturation voltages, the collector region must have low resistivity, (Fig. 7-9). Short storage time requires fast recombination of charge carriers left in the depletion region at the collector-base junction. Fast recombination is assisted by additional doping of the collector with gold atoms.

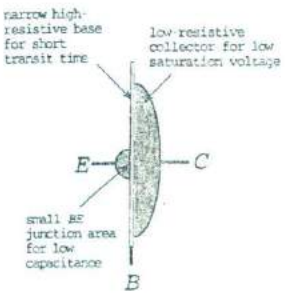


Figure 7-9
A small BE junction area and narrow base are required for high frequency performance and fast switching. Low saturation voltage is promoted by a low-resistive collector region.

Breakdown and Punch-Through

The transistor collector-base junction is normally reverse biased, so the maximum collector voltage is limited by the junction reverse breakdown voltage. To achieve high breakdown voltages, either the collector or the base must be very lightly doped. If the base is more lightly doped than the collector, the collector-base depletion region penetrates deeply into the base. This will cause transistor breakdown by *punch-through* when it links with the emitter-base

depletion region. To avoid punch through, the collector region close to the base is usually more lightly doped than the base. The collector-base depletion region then spreads into the collector, rather than into the base.

Section 7-3 Review

7-3.1 Briefly discuss the requirements for constructing transistors with (a) good current gain, (b) high frequency response.

7-3.2 Explain the design requirements for transistors with (a) high power dissipation, (b) high breakdown voltage.

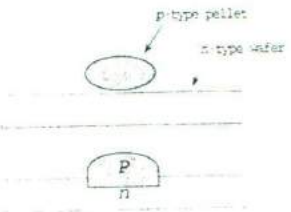
7-3.3 List the requirements for switching transistor construction.

7-4 Transistor Fabrication

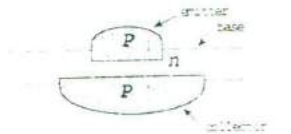
Alloy Transistors

For manufacture of *alloy transistors*, single-crystal *n*-type wafers are scribed into many small sections, or *dice*, each of which forms the substrate for one transistor. A small pellet of *p*-type material is melted on one surface of each section until it partially penetrates and forms an alloy with the substrate, [Fig. 7-10(a)], thus creating a *pn*-junction. The process is repeated on the other side of the wafer to constitute a *pnp* transistor.

One of the junctions has a large area and one has a small area, as illustrated in Fig. 7-10(b). The small-area junction becomes the emitter-base junction, and the larger one becomes the collector-base junction. One reason for this is that the large area junction most easily collects all of the charge carriers emitted from the small-area junction. Another more important reason is that most of the power is dissipated at the transistor collector-base junction.



(a) *p*-type pellet melted on an *n*-type wafer



(b) Alloy transistor

Figure 7-10
A pnp alloy transistor is constructed by melting p-type pellets on the surface of an n-type wafer.

Suppose a silicon transistor has I_C = 10 mA and V_{CE} = 10 V, (see Fig. 7-11). The total power dissipate in the transistor is,

$$P = V_{CE} \times I_C = 10\text{ V} \times 10\text{ mA}$$
$$= 100\text{ mW}$$

The base-emitter voltage is V_{BE} = 0.7 V, and the collector-base voltage is,

$$V_{CB} = V_{CE} - V_{BE} = 10\text{ V} - 0.7\text{ V}$$
$$= 9.3\text{ V}$$

The power dissipated at the base-emitter junction is,

$$V_{BE} \times I_C = 0.7\text{ V} \times 10\text{ mA}$$
$$= 7\text{ mW}$$

and, the power dissipated at the collector-base junction is,

$$V_{CB} \times I_C = 9.3\text{ V} \times 10\text{ mA}$$
$$= 93\text{ mW}$$

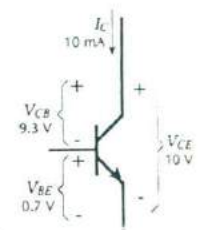


Figure 7-11
Most of the power dissipation in a transistor occurs at the collector-base junction.

Microalloy Transistors

Because very narrow base widths are difficult to obtain with alloy transistors, they are not suitable for high frequency applications. To improve the high-frequency performance, holes are first etched into the wafer from each side, leaving a very thin layer, (Fig 7-12). By a plating process, surfaces of impurity material are formed on each side of the thin *n*-type portion. Heat is then applied to alloy the impurities into the base region. This process produces very thin base regions and good high-frequency performance. The device is termed a *microalloy* transistor.

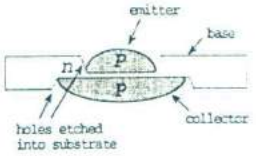


Figure 7-12
A very narrow base region gives microalloy transistors good high-frequency performance.

Microalloy-Diffused Transistors

In microalloy transistors, the collector-base depletion region penetrates deeply into the very thin base. Thus, a major disadvantage is that punch-through can occur at very low collector voltages. *Microalloy-diffused* transistors use a substrate that is initially undoped. After the holes are etched into each side of the wafer to produce the thin base region, the base is doped by diffusion from the collector side. The diffusion can be carefully controlled so that the base region is heavily doped at the collector side, with the doping becoming progressively less until the material is almost intrinsic (undoped) at the emitter. With this kind of doping, the collector-base depletion region penetrates only a short distance into the base, so that high punch-through voltages are achieved.

Diffused Mesa

In the production of *mesa transistors*, several thousand transistors are simultaneously formed on the wafer, by the diffusion process. As shown in Fig. 7-13, the main body of the wafer becomes the *n*-type collectors, the diffused *p*-regions become the bases, and the final *n*-regions are the emitters. Metal films are deposited on the base and emitter surfaces for contacts.

The transistors could be separated by the usual process of scribing lines on the surface of the wafer and breaking it into individual units. However, this produces very rough edges that result in relatively high leakage currents between collector and base. So, before cutting the wafer, the transistors are isolated by etching away the unwanted portions of the diffused area to form troughs between devices. As illustrated, the base and emitter regions now project above the main wafer which forms the collector region. This is the *mesa* structure. The narrow base widths that can be achieved by the diffusion process make the mesa transistor useful at very high frequencies.

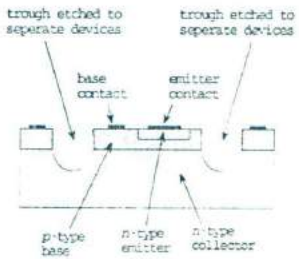


Figure 7-13
Mesa transistors are created by etching troughs between individual devices to give low collector-base leakage currents.

Epitaxial Mesa

One of the disadvantages of the process just described is that, because the collector region is highly resistive, diffused mesa transistors have a high saturation voltage, (see Section 5-10). Such devices are unsuitable for saturated switching applications. This same characteristic (high collector resistance) is desirable for

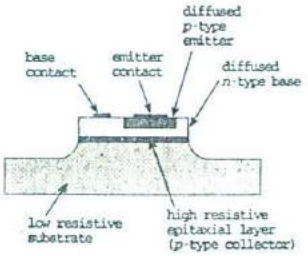


Figure 7-14
Epitaxial mesa transistor. The epitaxial process combined with the mesa structure gives high breakdown voltages and low saturation levels.

high punch-through voltage. One method of achieving both high punch-through voltage and low saturation level uses the epitaxial process, to produce an *epitaxial mesa* transistor.

Starting with a low-resistive (highly doped) wafer, a thin, highly resistive epitaxial layer is grown. This layer becomes the collector, and the base and emitter are diffused as already discussed. The arrangement is illustrated in Fig. 7-14. The punch-through voltage is high because the collector-base depletion region spreads deepest into the lightly doped collector. Saturation voltage is low, because the collector region is very narrow and the main body of the wafer through which collector current must flow has a very low resistance.

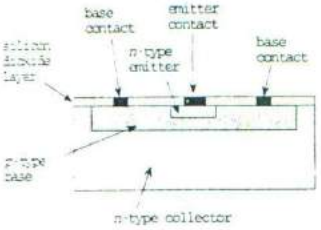


Figure 7-15
A diffused planar transistor has the collector-base junction covered, so that I_{CBO} is reduced to very low levels.

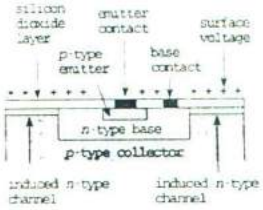
Diffused Planar Transistor

In all the previously described transistors the collector-base junction is exposed (within the transistor package), and substantial charge carrier leakage can occur at the junction surface. In the *diffused planar* transistor illustrated in Fig. 7-15, the collector-base junction is covered with a layer of silicon dioxide. This construction gives a very low collector-base leakage current (I_{CBO}); typically 0.1 nA.

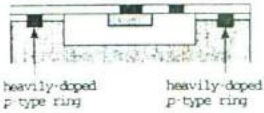
Annular Transistor

A problem which occurs particularly with *pnp* planar transistors is the *induced channel*. This results when a relatively high voltage is applied to the silicon dioxide surface, (at one of the terminals). Consider the *pnp* structure shown in Fig. 7-16(a). If the surface of the silicon dioxide has a positive voltage, minority charge carriers within the lightly doped *p*-type substrate are attracted by the positive potential. The minority charge carriers concentrate at the upper edge of the substrate and form an *n*-type channel from the base to the edge of the device. This becomes an extension of the *n*-type base region and results in charge carrier leakage at the exposed edge of the collector-base junction.

The problem arises because the *p*-type substrate is highly resistive. If it were heavily doped with *p*-type charge carriers, the concentration of *n*-type carriers would be absorbed (the electrons would be swallowed by holes). The introduction of a heavily doped *p*-type ring around the base, as in Fig. 7-16(b), interrupts the induced channel and isolates the collector-base junction from the device surface. The *annular transistor*, therefore, is a high-voltage device with the low collector-base leakage of the planar transistor.



(a) *n*-type channel induced by terminal voltage



(b) Heavily doped *p*-type ring interrupts the induced channel

Figure 7-16
Annular transistors have a heavily-doped p-type ring included to interrupt unwanted n-type channels that are induced by high voltages.

Section 7-4 Review

7-4.1 Briefly explain the construction of alloy, microalloy, and microalloy-diffused transistors.

7-4.2 Describe diffused mesa and epitaxial mesa transistor construction.

7-4.3 Discuss the construction of diffused planar and annular transistors.

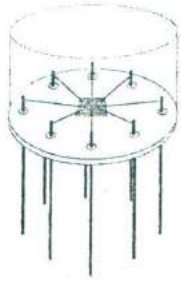
7-5 Integrated Circuits

IC Types

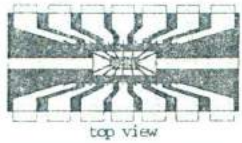
An *integrated circuit* (*IC*) consists of several interconnected transistors, resistors, etc., all contained in one small package with external connecting terminals. The circuit may be entirely self-contained, requiring only input and output connections and a supply voltage. Alternatively, a few external components may have to be connected to make the circuit operate.

Integrated circuits may be classified in terms of their function as *analog* or *digital*. Analog *ICs* (also termed *linear ICs*) may be amplifiers, voltage regulators, etc. Digital *ICs* (logic gates and counting circuits) contain transistors which are normally either in a switched-*off* or switched-*on* state.

The techniques used in manufacturing integrated circuits provide another method of classification. The major *IC* manufacturing technique is termed *monolithic*. Other fabrication techniques are *thin-film*, *thick-film*, and *hybrid*.



(a) Can-type *IC* enclosure



(b) Plastic *IC* enclosure

Figure 7-17
Monolithic integrated circuits consist of a single-chip circuit contained in a metal or plastic enclosure with connecting pins.

Monolithic Integrated Circuits

In a *monolithic* integrated circuit all components are fabricated by the diffusion process on a single chip of silicon. Interconnections between components are provided on the surface of the structure, and external connecting wires are taken out to terminals, as illustrated in Fig. 7-17. The vast majority of integrated circuits are monolithic because it is the most economical process for mass production.

Thin Film

Thin-film integrated circuits are constructed by depositing films of conducting material on the surface of a glass or ceramic base. By controlling the width and thickness of the films, and by using different materials selected for their resistivity, resistors and conductors are fabricated. Capacitors are produced by sandwiching a film of insulating oxide between two conducting films. Inductors are made by depositing metal film in a spiral formation. Transistors and diodes are usually tiny discrete components connected into the circuit.

Thick Film

Thick-film integrated circuits are sometimes referred to as *printed thin-film* circuits. In this process, silk-screen printing techniques are employed to create the desired circuit pattern on a ceramic substrate. The inks used are pastes which have conductive, resistive, or dielectric properties. After printing, the circuits are high-temperature-fired in a furnace to fuse the films to the substrate. Thick-film passive components are fabricated in the same way as those in thin-film circuits. As with thin-film circuits, active components are added as separate devices. A portion of a thick-film circuit is shown in Fig. 7-18.

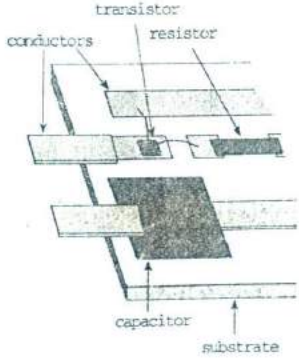


Figure 7-18
Enlarged portion of a thick film integrated circuit.

Integrated circuits produced by thin- or thick-film techniques usually have better component tolerances and give better high-frequency performance than monolithic integrated circuits.

Hybrid

Figure 7-19 illustrates the structure of a *hybrid* or *multichip* integrated circuit. As the name implies, the circuit is constructed by interconnecting a number of individual chips. The active components are diffused transistors or diodes. The passive components may be groups of diffused resistors or capacitors on a single chip, or they may be thin-film components. Connections between chips are provided by fine wire or metal film.

Like thin-film and thick-film *IC*s, multichip circuits usually have better performance than monolithic circuits. Although the process is too expensive for mass production, multichip techniques are quite economical for small quantities and are frequently used as prototypes for monolithic integrated circuits.

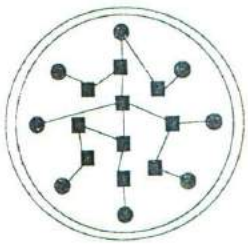


Figure 7-19
Uncovered top view of hybrid integrated circuit. Individual components are interconnected to form a single circuit.

Section 7-5 Review

7-5.1 Briefly define monolithic, thin-film, thick-film, and hybrid integrated circuits.

7-6 Integrated Circuit Components

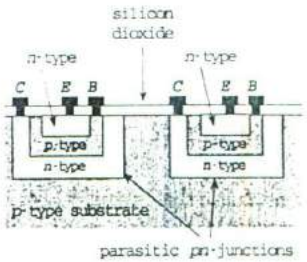
Transistors and Diodes

The epitaxial planar diffusion process described in Section 7-4 is normally employed for the manufacture of *IC* transistors and diodes. Collector, base, and emitter regions are diffused into a silicon substrate and surface terminals are provided for connection, as illustrated in Fig. 7-20(a).

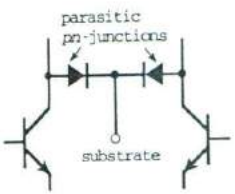
In discrete transistors the substrate is normally used as a collector. If this were done with transistors in a monolithic integrated circuit, all transistors fabricated on one substrate would have their collectors connected together. For this reason, separate collector regions must be diffused into the substrate.

Even though separate collector regions are formed, they are not completely isolated from the substrate. Figure 7-20(a) shows that an unwanted (*parasitic*) *pn*-junction is formed by the substrate and the transistor collector region. If the circuit is to function correctly, these junctions must never become forward biased. Thus, in the case of a *p*-type substrate, the substrate must always be kept negative with respect to the transistor collectors, [Fig. 7-20(b)]. This requires that the substrate be connected to the most negative terminal of the circuit supply.

The parasitic junctions can affect the circuit performance even when they are reverse biased. The junction reverse leakage current can be a serious problem in circuits that operate at very low current levels. The capacitance of the reverse-biased junction can affect the circuit high-frequency performance, and the junction



(a) Cross-section of two adjacent *IC* transistors



(b) Circuit diagram showing parasitic junctions

Figure 7-20
Integrated circuit components have unwanted (parasitic) interconnecting pn-junctions that must be kept reverse biased.

breakdown voltage imposes limits on the usable level of supply voltage. All these factors can be minimized by using highly resistive (lightly doped) material for the substrate.

Integrated circuit diodes are fabricated by diffusion exactly like transistors. Two of the regions are used to form one *pn*-junction. Alternatively, the collector region of a transistor may be connected directly to the base base (Fig. 7-21), so that the device behaves as a diode while operating similarly to a saturated transistor.

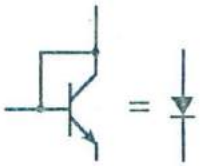


Figure 7-21
A transistor can be made to behave as a diode by connecting the collector and base.

Resistors

The resistivity of semiconductor material is a function of doping density, so resistors can be produced by doping strips of material and providing terminals, (Fig. 7-22). The range of resistor values that may be produced by the diffusion process varies from ohms to hundreds of kilohms. The typical tolerance, however, may be no better than ±5%, and may even be as high as ±20%. However, if all resistors are diffused at the same time, then the *tolerance ratio* can be good. For example, several resistors with the same nominal value may all have a ±20% tolerance, but have actual resistance values within a few percent of each other.

Another method of producing resistors for integrated circuits uses the thin-film technique. In this process a metal film is deposited on a glass or silicon dioxide surface. The thickness, width, and length of the film are regulated to give a desired resistance value. Since diffused resistors can be processed while diffusing transistors, the diffusion technique is the least expensive and the most frequently used.

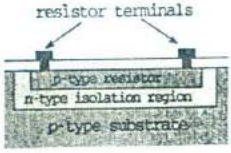


Figure 7-22
A monolithic IC resistor is created by doping a strip of semiconductor material to give the desired resistance.

Capacitors

Because all *pn*-junctions have capacitance, capacitors may be produced by fabricating suitable junctions. As in the case of other diffused components, parasitic junctions are unavoidable. Both the parasitic and the main junction must be kept reverse biased to avoid direct current flow. The depletion region width and junction capacitance vary with changes in reverse bias, so for capacitance value stability, a *dc* reverse bias greater than maximum signal voltage levels must be maintained across the junction.

Integrated circuit capacitors may also be fabricated by utilizing the silicon dioxide surface layer as a dielectric. A heavily-doped *n*-region is diffused to form one plate of the capacitor. The other plate is created by depositing a film of aluminum on the silicon dioxide, (see Fig. 7-23). Voltages of any polarity may be employed with this type of capacitor, and the breakdown voltage is very much larger than that for diffused capacitors. The junction areas available for creation of *IC* capacitors are very small indeed, so that normally only picofarad capacitance values are possible.

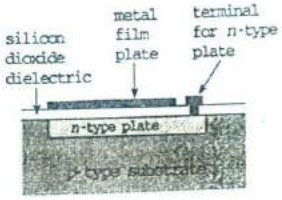


Figure 7-23
IC capacitor using silicon dioxide as the dielectric. The lower plate is heavily-doped n-type semiconductor, and the upper plate is a metal film.

Section 7-6 Review

7-6.1 Discuss the fabrication of integrated circuit transistors and diodes.

7-6.2 Explain how *IC* resistors and capacitors are constructed.

7-7 Transistor and IC Packaging

Discrete Transistor Packaging

Many low-power transistors are encapsuled in resin with protruding metal connecting leads, as illustrated in Fig. 7-24. This is known as a *TO-92* package. Note the emitter, base, and collector terminal connections. These are in the sequence *E,B,C*, left to right, looking at the bottom of the transistor with the flat side uppermost. This kind of package is economical, but it has a limited operating temperature range.

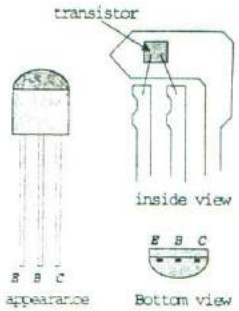


Figure 7-24
Low-power resin-encapsuled transistor; TO-92 package.

Figure 7-25 shows another method of low-power transistor packaging where the device is hermetically scaled in a metal can. Depending on the size of the can, this is identified as a *TO-5* to *TO-18* package. The transistor is first mounted with its collector in (mechanically and electrically) contact with a heat-conducting metal plate. Wires (insulated from the plate) pass through for the emitter and base connections, and the covering metal can is welded to the plate. Looking at the bottom of the transistor, and moving clockwise from the tab, the terminals are identified as *E.B.C.* The metal can enclosure gives a greater temperature range and greater power dissipation than resin encapsulation.

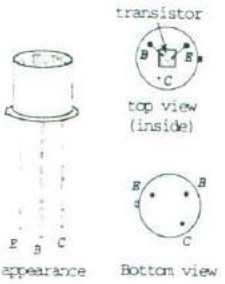
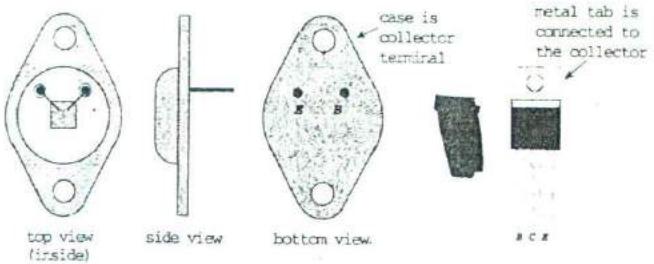


Figure 7-25
Low-power metal can-enclosed transistor; TO-18 package.

For high-power transistor packaging, a sealed can (*TO-3*) is often used, [Fig. 7-26(a)]. In this case the heat-conducting plate is much larger than in the *TO-5* package, and it is designed for mounting directly on a heat sink. Connecting pins are provided for the base and the emitter, and the collector connection is made by means of the metal plate. Note the terminal identifications, again looking at the bottom of the device.

Figure 7-26(b) shows a plastic-encapsuled power transistor with a metal tab for fastening to a heat sink. Once again, note the transistor terminal identifications, and note that the the metal tab is connected to the collector. Several other package types are available for low-power and high-power devices.



(a) *TO-3* metal can enclosure (b) *TO-220* plastic enclosure

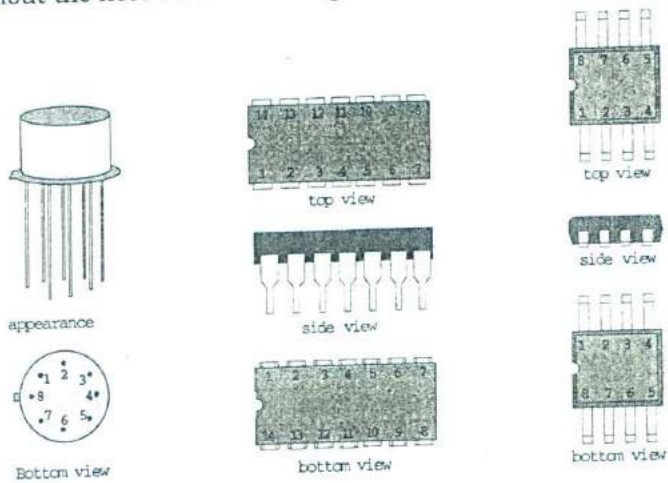
Figure 7-26
Metal can-type and plastic-encapsuled high power transistors.

IC Packages

Like semiconductor devices, integrated circuits must be packaged to provide mechanical protection and terminals for electrical connection. Several standard packages in general use are illustrated in Fig. 7-27.

The metal-can-type of container affords electromagnetic shielding for the *IC* chip which cannot be obtained with the plastic packages, [Fig. 7-27(a)]. Note that the terminals are numbered clockwise from the tab, looking at the bottom of the can.

Plastic *dual-in-line (DIL)* packages [Fig. 7-27(b)] are more economical than metal cans, and are widely used for industrial and consumer applications. The terminal numbering system again follows the bottom-view clockwise rule, starting from a notch in the plastic. A dimple, or other marker, is sometimes used instead of a notch. This is located on top of the package close to pin 1. *DIL*-type packages are much more convenient for circuit board use than cans, because the lead arrangement and flat package allows greater circuit densities. The surface mounting package shown in Fig. 7-27(c) is most economical for printed circuit board use, because the terminals are soldered directly on to the board without the need for hole drilling.



(a) Metal can-enclosed *IC*

(b) Plastic *DIL IC* package

(c) Surface mount *IC* package

Figure 7-27
Integrated circuits are typically packaged in metal cans, dual-in-line, or surface-mount plastic enclosures.

Section 7-7 Review

7-7.1 Sketch the terminal arrangements for *TO-92*, *TO-5*, and *TO-3* transistor packages, and identify the emitter, base, and collector terminals on each package.

7-7.2 Sketch metal can and *DIL* integrated circuit packages, and show the terminal numbering systems.

Chapter-7 Review Questions

Section 7-1

7-1 Describe the process of preparing semiconductor material for device manufacture.

7-2 Explain diffusion and epitaxial growth, and discuss the application of each process to transistor manufacture.

Section 7-2

7-3 Draw sketches to show the construction of alloy diodes and diffused diodes. Briefly explain in each case.

Section 7-3

7-4 Explain the various transistor manufacturing requirements for maximum performance with respect to (a) current gain, (b) power dissipation, (c) frequency response, (d) switching response, (e) breakdown voltage.

Section 7-4

7-5 Describe the microalloy and microalloy diffusion techniques for transistor manufacture. Explain the advantages and disadvantages of transistors made by these techniques.

7-6 Using sketches, explain the diffused mesa and epitaxial mesa transistors. Discuss the advantages and disadvantages of mesa transistors.

7-7 Explain the manufacturing process for diffused-planar and annular transistors, and discuss the advantages and disadvantages of each.

7-8 Show that most of the power dissipation in a transistor occurs at the collector-base junction.

Section 7-5

7-9 Briefly explain the thin-film and thick-film methods of integrated circuit manufacture, and discuss their advantages and disadvantages.

7-10 Using illustrations, explain the fabrication process for monolithic integrated circuits. Discuss the advantages and disadvantages of monolithic *ICs*.

7-11 Describe hybrid integrated circuits.

Section 7-6

7-12 Sketch the construction and circuit diagram for two monolithic integrated circuit transistors showing the parasitic components. State any precautions necessary in the use of the circuit.

7-13 Briefly explain how diodes, resistors, and capacitors are fabricated in monolithic integrated circuits.

Section 7-7

7-14 Sketch *TO-92*, *TO-18*, and *TO-3* transistor packages, and identify the emitter, base, and collector terminals.

7-15 Sketch metal can and *DIL* integrated circuit packages, and show the terminal numbering system.