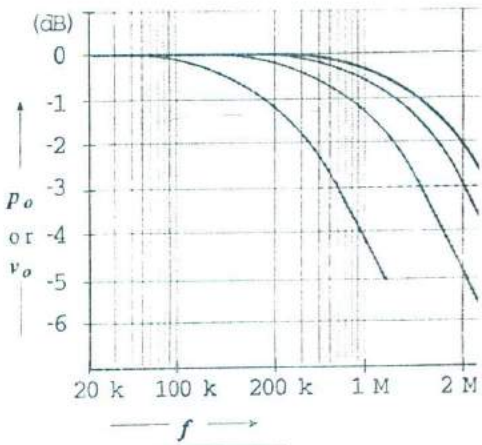
Chapter 8

BJT Specifications and Performance

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Objectives

You will be able to:

1. Identify important parameters on transistor data sheets for small-signal, high-power, high-frequency, and switching transistors, and determine the parameter values.
2. Calculate circuit power gains and power output changes in decibels.
3. Define Miller effect, and determine the input capacitance for transistor circuits using the data sheet specifications.
4. Explain the effects of input and stray capacitances on BJT circuit frequency response, and calculate cutoff frequencies for CE, CB, and CC circuits.
5. Determine transistor switching times from the data sheet, and calculate device turn-on and turn-off times.
6. Define noise figure and noise factor, and estimate circuit output noise levels originating from resistors and transistors.
7. Determine transistor maximum power dissipations at any temperature using power derating factors and derating graphs.
8. Sketch a thermal resistance circuit for a transistor with a heat sink. Determine the required thermal resistance for transistor heat sinks, and select suitable heat sinks for given circuit conditions.

Introduction

The performance characteristics and parameters for each type of transistor are specified on a data sheet published by the device manufacturer. The specifications must be correctly interpreted to achieve optimum transistor performance, and to avoid breakdown. Transistors must be selected to have a specified maximum collector-emitter voltage greater than the voltage applied to the *CE* terminals. The specified maximum collector current must be greater than the highest I_C level that may flow in the circuit. The maximum power that may be dissipated in a device is normally listed for a case temperature of 25°C. This value must be derated for operation at higher temperatures, and heat sinks must be employed where appropriate. Transistor cutoff frequency, switching times, noise figure, and input capacitance are all items that can be very important in various applications.

8-1 Transistor Data Sheets

To select a transistor for a particular application, the data sheets provided by device manufacturers must be consulted. Typical transistor data sheets are shown in Appendix 1-5 through 1-9, and portions are reproduced in this chapter.

Most data sheets start off with the device type number at the top of the page, a descriptive title, and a list of major applications for the device. This information is usually followed by mechanical data in the form of an illustration showing the package shape and dimensions, as well as indicating which leads are collector, base, and emitter, (see Fig. 8-1).

2N3903, 2N3904 (Silicon) NPN Transistors



NPN silicon annular transistors, designed for general purpose switching and amplifier applications.

Maximum ratings at T_A =25°C unless otherwise noted.

Characteristic	Symbol	Rating	Unit
Collector-emitter voltage	V_{CEO}	40	V_{dc}
Emitter-base voltage	V_{EB}	6	V_{dc}
Collector Current	I_C	200	mA

Figure 8-1
Portion of 2N3903-2N3904 transistor data sheet listing maximum terminal voltages and collector current.

The absolute maximum ratings of the transistor at a temperature of 25°C are listed next. These are the maximum voltages, currents, and power dissipation that the device can survive without breaking down. It is very important that these ratings never be

exceeded; otherwise, failure of the device is quite possible. *For reliability, the maximum ratings should not even be approached.* The maximum transistor ratings must also be adjusted downward for operation at temperatures greater than 25 °C.

Following the absolute maximum ratings, the data sheet normally shows a complete list of electrical characteristics for the device. Again, these are specified at 25°C, and allowances are necessary for temperature variations.

A complete understanding of all the quantities specified on a data sheet will not be achieved until circuit analysis and design is studied. Some of the most important quantities are considered below. It is important to note that the ratings for a given transistor are stated for specified circuit conditions. The ratings are no longer valid if these conditions change.

V_{CBO} *Collector-base voltage* — maximum *dc* voltage for reverse-biased collector-base junction.

V_{CEO} *Collector-emitter voltage* — maximum collector-emitter *dc* voltage with base open-circuited.

V_{EBO} *Emitter-base voltage* — maximum emitter-base reverse-bias *dc* voltage.

I_C *Collector current* — maximum *dc* collector current.

I_{CBO} or **I_{CO}** *Collector cutoff current* — *dc* collector current with the collector-base junction reverse biased and the emitter open-circuited.

$V_{CE(sat)}$ *Collector-emitter saturation voltage* — collector-emitter voltage with the device in saturation.

h_{FE} *Static forward current transfer ratio* — common emitter ratio of *dc* collector current and base current.

NF *Noise figure* — ratio of total noise output to total noise input expressed as a decibel (*dB*) ratio (see Sections 8-2). Defines the amount of noise added by the device, (see Sections 8-5).

f_{hfe} or **$f_{\alpha e}$** *Common emitter cutoff frequency* — common emitter operating frequency at which the device current gain falls to 0.707 of its normal (mid-frequency) value.

f_{hfb} or **$f_{\alpha b}$** *Common base cutoff frequency* — as above, for common base.

From the section of the *2N3903-2N3904* data sheet reproduced in Fig. 8-1, the maximum collector-emitter voltage is specified as V_{CEO} = 40 V. Obviously, this device should not be used in any circuit with a supply exceeding 40 V; otherwise the transistor might break down. Preferably, the circuit supply voltage should always be less than the specified maximum V_{CEO}.

The maximum V_{EB} is listed as 6 V. This is the highest voltage that may be applied *in reverse* across the base-emitter junction of

the transistor. If a greater voltage is used, the base-emitter junction of the transistor is likely to break down. The maximum (reverse) V_{EB} for most transistors is 5 V. In circumstances where the applied voltage might exceed this level, a clipping circuit may be used, (see Sections 3-7 and 3-8). Alternatively, a diode can be connected in series with the transistor emitter to increase the breakdown voltage, as shown in Fig. 8-2. The normal forward-biased base-emitter voltage for a transistor is, of course, approximately 0.7 V for a silicon transistor and approximately 0.3 V for a germanium transistor.

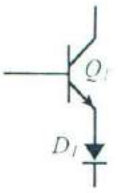


Figure 8-2
A diode connected in series with a transistor emitter protects the BE junction against excessive reverse voltage.

Figure 8-3 shows sections of a transistor data sheet which specify the *dc current gain* h_{FE}, and the *small signal* (or *ac*) *current gain* h_{fe}. For a *2N3904* device with I_C = 10 mA, h_{FE} is listed as 100 minimum and 300 maximum, (see the solid underlined quantities). If the transistor collector current is to be around 1 mA, then the minimum h_{FE} is 70, (dashed underlined). The maximum h_{FE} for I_C = 1 mA is not specified. It is unlikely that $h_{FE(max)}$ would exceed 300 for this condition. However, because the manufacturer does not list a maximum value, it remains uncertain. This situation illustrates the importance of reliable bias circuits that make I_C and V_{CE} largely independent of h_{FE}. (See Ch. 5).

2N3903, 2N3904

Characteristic		Symbol	Min	Max	Unit
DC current gain		h_{FE}			—
(I_C = 0.1 mA dc, V_{CE} = 1 V dc)	2N3903		20	—	
	2N3904		40	—	
(I_C = 1.0 mA dc, V_{CE} = 1 V dc)	2N3903		35	—	
	2N3904		70	—	
(I_C = 10 mA dc, V_{CE} = 1 V dc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mA dc, V_{CE} = 1 V dc)	2N3903		30	—	
	2N3904		60	—	
(I_C = 100 mA dc, V_{CE} = 1 V dc)	2N3903		15	—	
	2N3904		30	—	

Small Signal Current Gain		h_{fe}			—
(I_C = 1 mA dc, V_{CE} = 10 V, f = 1 kHz)					
	2N3903		50	200	
	2N3904		100	400	

Figure 8-3
Portion of 2N3903-2N3904 transistor data sheet listing dc current gain and small-signal ac current gain.

The *small-signal current gain* (h_{fe}) for a *2N3904* is listed in Fig. 8-3 as 100 minimum and 400 maximum. Once again, this parameter is specified for a particular set of bias conditions. The signal

frequency at which h_{fe} was measured is specified as 1 kHz. Section 8-2 discusses the fact that h_{fe} decreases at high frequencies.

Example 8-1

Referring to the 2N3905 specification in Appendix 1-6, determine the h_{ff} range for I_c = 10 mA, and the h_{fe} range for f = 1 kHz. Also determine the emitter-base breakdown voltage.

Solution

at I_c = 10 mA, h_{ff} = 50 to 150

at f = 1 kHz, h_{fe} = 50 to 200

$V_{(BR)EBO}$ = 5 V

Practise Problems

8-1.1 From the data sheet in Appendix 1-7, determine the following quantities for a 2N3251 transistor: $h_{FE(min)}$ at I_C = 1 mA, $h_{fe(min)}$ at f = 1 kHz, $V_{CE(max)}$, $V_{EB(max)}$, noise figure.

8-2 Decibels and Half-Power Points

Power Measurement in Decibels

The *power gain* (A_p) of an amplifier may be expressed in terms of the log of the ration of output power (p_o) to input power (p_i). This is illustrated in Fig. 8-4.

$$A_p = \log_{10}\left[\frac{p_o}{p_i}\right] \text{ bels}$$

or,

$$\mathbf{A_p = 10 \log_{10}\left[\frac{p_o}{p_i}\right] \text{ decibels (dB)}} \qquad \textbf{(8-1)}$$

Thus, the *decibel* is the unit of *power gain*, or *power level change*.

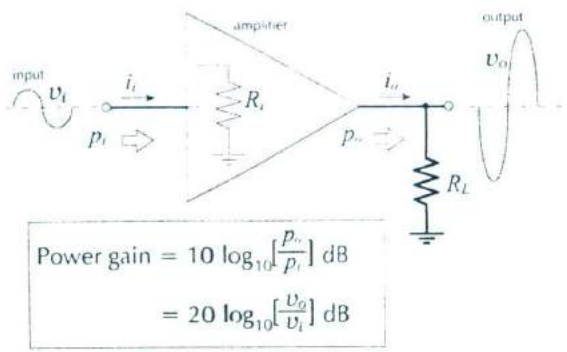


Figure 8-4
Amplifier power gain is measured in decibels (dB). Output power level changes are also measured in decibels.

The power dissipated in a resistance is (v^2/R).

So,
$$A_p = 10 \log_{10} \left[\frac{(v_o)^2/R_L}{(v_i)^2/R_i}\right] dB$$

$$= 10 \log_{10} \left[\frac{v_o}{v_i}\right]^2 dB \quad (\text{when } R_i = R_L)$$

or,
$$\mathbf{A_p = 20 \log_{10} \left[\frac{v_o}{v_i}\right] dB} \qquad \textbf{(8-2)}$$

Also, $P_o = i_o^2 R_L$ and $P_i = i_i^2 R_i$

So,
$$\mathbf{A_p = 20 \log_{10} \left[\frac{i_o}{i_i}\right] dB} \qquad \textbf{(8-3)}$$

It is important to note that *the above equations are correct only when the load resistance connected to the circuit output is equal to the circuit input resistance.* However, it is common practice in the electronics industry to apply these equations regardless of the relationship between input and load resistances!

Amplifier *output power level changes* (ΔP_o) are also measured in decibels, and in this case the equations become,

$$\mathbf{\Delta P_o = 10 \log_{10} \left[\frac{p_2}{p_1}\right] dB} \qquad \textbf{(8-4)}$$

where p_1 is the initial output power level, and p_2 is the new level.

Also,
$$\mathbf{\Delta P_o = 20 \log_{10} \left[\frac{v_2}{v_1}\right] dB} \qquad \textbf{(8-5)}$$

and,
$$\mathbf{\Delta P_o = 20 \log_{10} \left[\frac{i_2}{i_1}\right] dB} \qquad \textbf{(8-6)}$$

where v_1 and i_1 are the initial output voltage and current levels, and v_2 and i_2 are the new levels. Equations 8-4 through 8-6 are correct so long as the amplifier load resistance remains constant. Examples 8-2 and 8-3 demonstrate that the output power of an amplifier is reduced by 3 dB when the measured power falls to half its normal level, or when the measured voltage falls to 0.707 of its normal level.

Example 8-2

The output power from an amplifier is 50 mW when the signal frequency is 5 kHz. The power output falls to 25 mW when the frequency is increased to 20 kHz. Calculate the output power change in decibels.

Solution

Eq. 8-4,
$$\Delta P_o = 10 \log_{10} \left[\frac{p_2}{p_1}\right] = 10 \log_{10} \left[\frac{25 \text{ mW}}{50 \text{ mW}}\right]$$

$$= -3 \text{ dB}$$

Half-Power Points

Figure 8-5 shows a typical graph of amplifier output voltage or power plotted versus frequency. Note that the frequency scale is logarithmic. The output normally remains constant over a middle range of frequencies and falls off at low and high frequencies, due to effects explained in Sections 8-3 and 8-4. The gain over this middle range is termed the *mid-frequency gain*. The low frequency and high frequency at which the gain falls by 3 dB are designated f_1 and f_2, respectively. This range is normally considered the useful range of operating frequency for the amplifier, and the frequency difference ($f_2 - f_1$) is termed the *amplifier bandwidth* (*BW*).

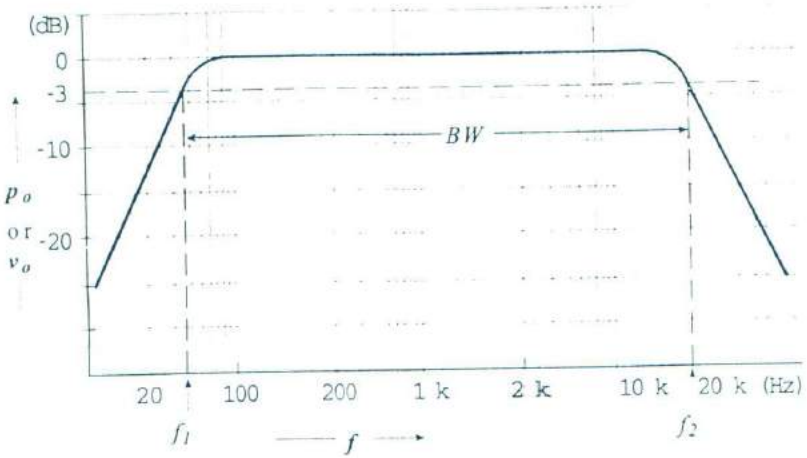


Figure 8-5
The output voltage and output power of an amplifier normally remains constant over a middle band of signal frequencies, and falls-off at high and low frequencies.

Frequencies f_1 and f_2 are termed the *half-power points*, or the 3 *dB points*. This is because, as shown in Example 8-2, the power output is -3 *dB* from its normal level when p_2 is half p_1. When the amplifier output is expressed as a voltage on the graph of frequency response, the 3 *dB* points (f_1 and f_2) occur when v_2 is 0.707 v_1. This relationship is demonstrated in Example 8-3.

Example 8-3

The output voltage of an amplifier is measured as 1 V at 5 kHz, and as 0.707 V at 20 kHz. Calculate the output power change.

Solution

Eq. 8-5,

$$\Delta P_o = 20 \log_{10} \left[\frac{V_2}{V_1}\right] = 20 \log_{10} \left[\frac{0.707\ \text{V}}{1\ \text{V}}\right]$$

$$= -3\ dB$$

Practise Problems

8-2.1 The output voltage of an amplifier is 2 V when the signal frequency is 3 kHz, and 0.5 V when the signal frequency is increased to 50 kHz. Calculate the decibel change in output power.

8-3 BJT Cutoff Frequency and Capacitances

Device Cutoff Frequency

All transistors have junction capacitances, (see Sections 2-6 and 6-3). The junction capacitances and the transit time of charge carriers through the semiconductor material limit the high frequency performance of the device. This limitation is expressed as a *cutoff frequency* (f_α), which is the frequency at which the transistor current gain falls to 0.707 of its gain at low and medium frequencies. The cutoff frequency can be expressed in two ways, the *common emitter cutoff frequency* $f_{\alpha e}$, and the *common base cutoff frequency* ($f_{\alpha b}$). $f_{\alpha e}$ is the frequency at which the common emitter current gain (h_{fe}), falls to 0.707 x (mid-frequency h_{fe}). $f_{\alpha b}$ is the frequency at which the common base current gain (h_{fb}) falls to 0.707 x (mid-frequency h_{fb}). It can be shown that,

$$f_{\alpha b} = h_{fe} f_{\alpha e} \qquad (8\text{-}7)$$

Equation 8-7 shows that $f_{\alpha b}$ can be identified as the *current-gain-bandwidth product*, or *total bandwidth* (f_T). This is the designation used on many transistor data sheets. The data sheet portion in Fig. 8-6 shows that f_T is 250 MHz for a *2N3903* and 300 MHz for a *2N3904*.

Characteristic	Symbol	Min	Max	Unit
Small-Signal Characteristics				
Current-gain—Bandwidth Product (I_C = 10 mA dc, V_{CE} = 20 V, f = 100 MHz)	f_T			MHz
2N3903		250	—	
2N3904		300	—	

Figure 8-6
Specification of transistor cutoff frequency on the 2N3903, 2N3904 data sheet.

Junction Capacitances

As already discussed, all *BJTs* have junction capacitances. These are identified as the base-collector capacitance (C_{bc}) and the base-emitter capacitance (C_{be}), (see Fig. 8-7). The device data sheet portion in Fig. 8-8 shows that the capacitances are usually listed as an *output capacitance* (C_{obo}), which is the same as C_{bc}, and an *input capacitance* (C_{ibo}) which corresponds to C_{be}. It should be noted that in both cases, the capacitance values are specified for reverse-biased junctions with zero current levels. C_{obo} varies when V_{CB} is altered, however, the changes are usually a maximum of approximately ±3 pF. C_{ibo} changes substantially from the specified capacitance when the base-emitter junction is forward biased, (as it always is for linear *BJT* operation).

When an emitter current flows across the *BE* junction, there is a diffusion capacitance (see Section 2-6) at the junction. This is directly proportional to the current level. It can be shown that,

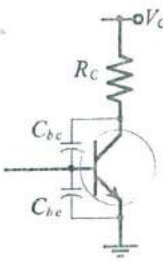


Figure 8-7
All transistors have junction capacitances.

$$C_{be} \approx \frac{6.1\, I_E}{f_T} \qquad (8\text{-}8)$$

Characteristic	Symbol	Min	Max	Unit
Output Capacitance (V_{CB} = 5 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	4.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	—	8.0	pF

Figure 8-8 Junction capacitance specifications for 2N3903 and 2N3904 transistors.

Miller Effect

Figure 8-9 shows an input signal ($+\Delta V_i$) applied to the base of a transistor connected in *CE* configuration. If the circuit voltage amplification is $-A_v$, then the collector voltage change is,

$$\Delta V_o = -A_v \times \Delta V_i$$

Note that, because of the phase reversal between input and output, the collector voltage is *reduced* by ($A_v \Delta V_i$) when the base voltage is *increased* by ΔV_i. The increase in V_B and decrease in V_C results in a total collector-base voltage reduction of,

$$\begin{aligned} \Delta V_{CB} &= \Delta V_i + A_v \Delta V_i \\ &= \Delta V_i (1 + A_v) \end{aligned}$$

This voltage change appears across the collector-base capacitance.

Using the equation $Q = C \times \Delta V$, it is found that the charge supplied to the input of the circuit is,

$$Q = C_{bc} \times \Delta V_i (1 + A_v)$$

or,

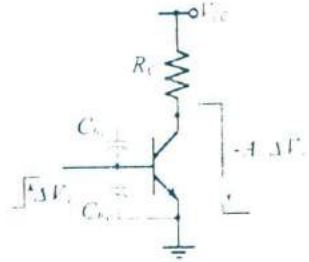
$$Q = (1 + A_v) C_{bc} \times \Delta V_i$$

Therefore, "*looking into*" the base, the collector-base capacitance appears to be $(1 + A_v)C_{bc}$. So, the capacitance is *amplified* by a factor of $(1 + A_v)$. This is known as the *Miller effect*.

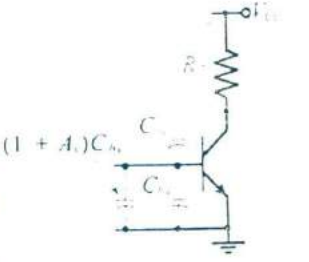
The total input capacitance (C_{in}) to the transistor is $(1 + A_v)C_{bc}$ in parallel with the base-emitter capacitance (C_{be}):

$$C_{in} = C_{be} + (1 + A_v)C_{bc} \qquad (8\text{-}9)$$

It should be noted that the Miller effect occurs only with amplifiers that have a 180° phase shift between input and output, (an inverting amplifier). Consequently, it occurs with *CE* circuits, but not with *CB* and emitter follower and circuits.



(a) ΔV_i and $-A_v \Delta V_i$ change V_{CB}



(b) $C_{in} = C_{be} + (1 + A_v)C_{bc}$

Figure 8-9 Because of the Miller effect, the input capacitance for a common-emitter amplifier is $C_{in} = C_{be} + (1 + A_v)C_{bc}$.

Example 8-4

The transistor in the circuit in Fig. 8-10 has I_C = 1 mA, h_{fe} = 50, h_{ie} = 1.3 kΩ, f_T = 250 MHz, and C_{bc} = 5 pF. Calculate the input capacitance when the circuit is operated as a *CE* amplifier with R_E bypassed.

Solution

From Eq. 6-12,
$$|A_v| = \frac{h_{fe}(R_C \| R_L)}{h_{ie}} = \frac{50 \times (8.2\ \text{k}\Omega \| 100\ \text{k}\Omega)}{1.3\ \text{k}\Omega}$$
$$= 291$$

Eq. 8-8,
$$C_{be} \approx \frac{6.1\, I_E}{f_T} \approx \frac{6.1 \times 1\ \text{mA}}{250\ \text{MHz}}$$
$$= 24.4\ \text{pF}$$

Eq. 8-9,
$$C_{in} = C_{be} + (1 + A_v)C_{bc} = 24.4\ \text{pF} + [(1 + 291) \times 5\ \text{pF}]$$
$$= 1.48\ \text{nF}$$

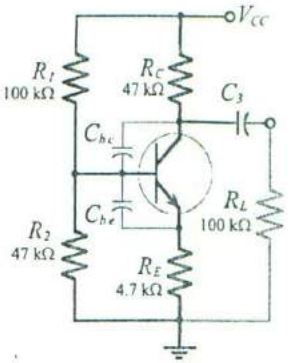


Figure 8-10
The upper cutoff frequency for a transistor circuit can be limited by the input capacitance.

Practise Problems

8-3.1 A CE circuit with a voltage gain of 100 has $I_C = 0.75$ mA, $C_{bc} = 3$ pF, and $f_T = 300$ MHz. Calculate C_{in} when a 45 pF capacitor is connected across the collector-base terminals.

8-4 BJT Circuit Frequency Response

Coupling and Bypass Capacitor Effects

Consider the typical transistor amplifier frequency response illustrated in Fig. 8-5. As discussed, the amplifier voltage gain is constant over a middle range of signal frequencies, and it falls at the low and high ends of the frequency range.

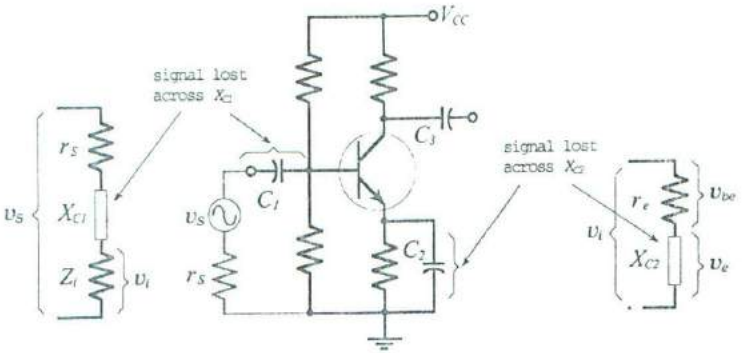


Figure 8-11
The low-frequency fall off in voltage gain in a transistor amplifier is due to signal loss across coupling and bypass capacitors.

The gain fall-off at low signal frequencies is due to the effect of coupling and bypass capacitors. Recall that the reactance of a capacitor is $X_C = 1/(2\pi fC)$. At medium and high frequencies, the factor f makes X_C very small, so that all coupling and bypass capacitors behave as ac short circuits. At low frequencies, X_C is large enough to divide the voltages across the capacitors and series resistances, (see Fig. 8-11). As the signal frequency gets lower, the capacitive reactance increases, more of the signal is lost across the capacitors, and the circuit gain continues to fall. Coupling and bypass capacitors are further investigated in Section 12-1.

Input Capacitance Effect on CE and CB Circuits

The input capacitance of an amplifier (discussed in Section 8-3) reduces the circuit gain by 3 dB when the capacitive impedance equals the resistance in parallel with the input, (see Fig. 8-12). That is when,

$$\mathbf{X_{Ci} = Z_i || r_s} \qquad \textbf{(8-10)}$$

So, all circuits have an *input capacitance limited upper cutoff frequency* ($f_{2(i)}$). As already explained, the input capacitance of a *CE* circuit is amplified by the Miller effect, but Miller effect does not occur in a *CB* circuit. Consequently, a *CB* circuit operates to a much higher signal frequency than a similar *CE* circuit.

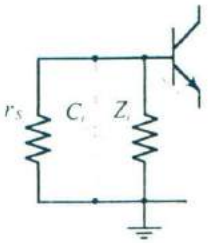


Figure 8-12
The input resistance (Z_i) and the signal source resistance (r_s) are in parallel with the circuit input capacitance (C_{in}).

Example 8-5

Calculate the input capacitance limited upper cutoff frequency for the circuit in Fig. 8-13 (reproduced from Fig. 8-10); (a) when the circuit is used in *CE* configuration with R_E bypassed, (b) when operating as a *CB* circuit with the base bypassed to ground. As in Ex. 8-4, C_{bc} = 5 pF and C_{be} = 24.4 pF. Also, h_{fe} = 50, h_{ie} = 1.3 kΩ, h_{ib} = 24.5 Ω, and r_s = 600 Ω.

Solution

(a) Common emitter circuit,

$$Z_i = R_1||R_2||h_{ie} = 100\ \text{k}\Omega||47\ \text{k}\Omega||1.3\ \text{k}\Omega$$
$$= 1.25\ \text{k}\Omega$$

$$r_s||Z_i = 600\ \Omega||1.25\ \text{k}\Omega$$
$$= 405\ \Omega$$

From Ex. 8-4, $C_{in} = 1.48$ nF

From Eq. 8-10, $$f_{2(i)} = \frac{1}{2\pi C_{in}(r_s||Z_i)} = \frac{1}{2\pi \times 1.48\ \text{nF} \times 405\ \Omega}$$
$$= 266\ \text{kHz}$$

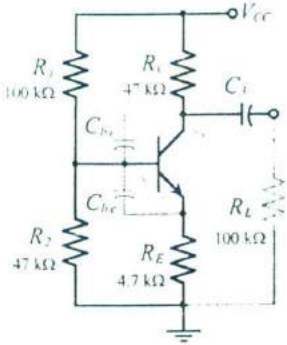


Figure 8-13
Circuit that may be connected to function in either CE or CB configuration.

(b) Common base circuit,

$$Z_i = R_E||h_{ib} = 4.7\ \text{k}\Omega||24.5\ \Omega$$
$$= 24.4\ \Omega$$

$$r_s||Z_i = 600\ \Omega||24.4\ \Omega$$
$$= 23.4\ \Omega$$

$$C_{in} = C_{be} + C_{bc} = 24.4\ \text{pF} + 5\ \text{pF}$$
$$= 29.4\ \text{pF}$$

from Eq. 8-10, $$f_{2(i)} = \frac{1}{2\pi C_{in}(r_s||Z_i)} = \frac{1}{2\pi \times 29.4\ \text{pF} \times 23.4\ \Omega}$$
$$= 231\ \text{MHz}$$

Input Capacitance Effects on Emitter Follower

When a transistor is used as an emitter follower its *BE* junction voltage is not significantly altered by the *ac* input signal, because virtually all of v_i appears at the emitter as v_o, (see Fig. 8-14). Also, there is no Miller effect to amplify C_{bc}, so the input capacitance is $C_{ibo} \| C_{obo}$. The input capacitance limited cutoff frequency for an emitter follower is very much higher than that for a *CE* circuit.

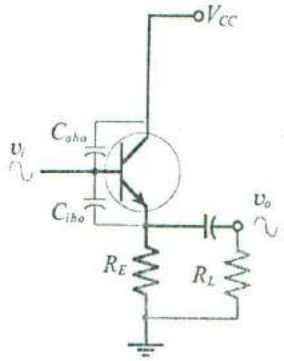


Figure 8-14
There is no Miller effect input capacitance amplification with an emitter follower circuit.

Stray Capacitance

Figure 8-15 illustrates the fact that *stray capacitances* (C_{si} and C_{so}) exists in all transistor circuits. This is capacitance between connecting wires and ground, and normally it is extremely small. The stray capacitance at the device base is usually much smaller than the input capacitance at the base, so that it can normally be neglected. When this is not the case, the stray capacitance must be included with the input capacitance for *CE* circuit cutoff frequency calculations.

At the circuit output, the impedance of the stray capacitance (C_{so}) is very high at low and medium signal frequencies, so that it has no effect on the gain. At high frequencies, the stray capacitive impedance becomes small enough to shunt away some of the input and output currents, and thus it reduces the circuit gain. Referring to Fig. 8-15, it is seen that circuit *ac* load consists of the output stray capacitance (C_{so}) in parallel with R_C and R_L. Rewriting the voltage gain equation for *CE* and *CB* circuits,

$$|A_v| = \frac{h_{fe}(R_C \| R_L \| X_{cso})}{h_{ie}}$$

If the transistor cutoff frequency has not caused the gain to fall off at a lower frequency, then the gain falls by 3 dB when $X_{cso} = R_C \| R_L$. This is an *output capacitance limited cutoff frequency* ($f_{2(o)}$).

If the voltage gain falls by 3 dB at $f_{\alpha e}$ due to the transistor, and by 3 dB at the same frequency due to the stray capacitance, then the gain is down by 6 dB. Consequently, the amplifier upper cutoff frequency is lower than $f_{\alpha e}$. This is illustrated in Fig. 8-16.

As discussed, there is an additional 3 dB attenuation when $X_{cso} = R_C \| R_L$. If $X_{cso} = 2(R_C \| R_L)$ at $f_{\alpha e}$, the additional attenuation can be shown to be 1 dB, (see Fig. 8-16). With $X_{cso} = 5(R_C \| R_L)$ at $f_{\alpha e}$, there is only 0.2 dB additional attenuation, as illustrated.

In some circumstances it is desirable to set the upper cutoff frequency of a circuit at a frequency well below the transistor cutoff frequency, (see Fig. 8-16). This is done simply by connecting a capacitor from the collector terminal to ground exactly as C_{so} is shown in Fig. 8-15. The capacitance value is calculated at the desired cutoff frequency to give,

$$X_c = R_C \| R_L \qquad (8\text{-}11)$$

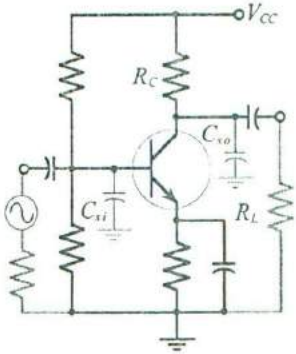


Figure 8-15
Stray capacitance can cause transistor amplifier gain reduction at high frequency.

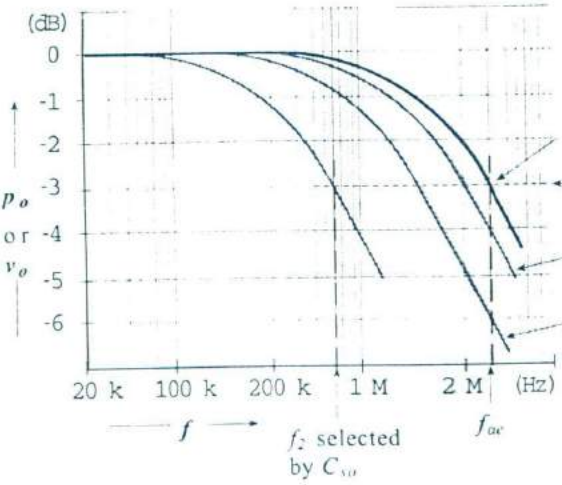


Figure 8-16
The BJT cutoff frequency (f_{ae}) determines the upper cutoff frequency of a circuit, so long as the impedance of the output stray capacitance (C_{so}) is much larger than $R_C \| R_L$. When X_{CSO} is much smaller than $R_C \| R_L$, the circuit upper cutoff frequency is determined by C_{so}.

Example 8-6

A transistor with $f_T = 50$ MHz and $h_{fe} = 50$ is employed in the *CE* amplifier in Fig. 8-17. Determine the upper 3 *dB* frequency for the device. Also, calculate the required capacitance for C_4 to give a 60 kHz upper cutoff frequency. Assume that $R_L >> R_C$.

Solution

From Eq. 8-7,
$$f_{ae} = \frac{f_T}{h_{fe}} = \frac{50 \text{ MHz}}{50}$$
$$= 1 \text{ MHz}$$

From Eq. 8-11,
$$C_4 = \frac{1}{2\pi f_{2(o)} R_C} = \frac{1}{2 \times \pi \times 60 \text{ kHz} \times 10 \text{ k}\Omega}$$
$$= 265 \text{ pF}$$

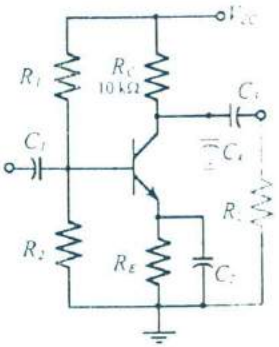


Figure 8-17
Circuit for Ex. 8-7.

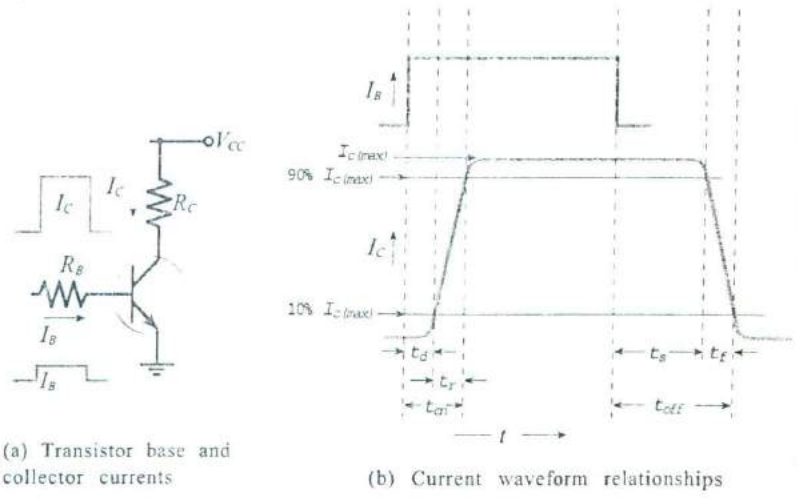
Practise Problems

8-4.1 A *CE* amplifier circuit has $R_C = 5.6$ kΩ, and $R_L = 56$ kΩ. The transistor used has $h_{fe} = 60$, $h_{ie} = 1.5$ kΩ, $C_{be} = 192$ pF and $C_{bc} = 6$ pF. The signal source resistance is 1 kΩ, and the voltage divider bias resistors are $R_1 = 82$ kΩ and $R_2 = 39$ kΩ. Determine the input capacitance limited upper cutoff frequency.

8-4.2 A transistor in a single-stage *CE* amplifier has $h_{fe} = 75$ and $f_T = 12$ MHz. The load resistance is $R_C \| R_L = 20$ kΩ. Determine the upper 3 *dB* frequency (f_2) for the circuit. Also, calculate the output stray capacitance that will produce an additional 3 dB attenuation at f_2.

8-5 *Transistor Switching Times*

For transistor switching circuits (see Section 5-10), the switching speed of the device can be an important quantity. Consider the circuit in Fig. 8-18(a). When the base input current is applied, the transistor does not switch *on* immediately. Like frequency response, the switching time is affected by junction capacitance and the transit time of electrons across the junctions. The time between the application of the input pulse and commencement of collector current flow is termed the *delay time* (t_d), [see Fig. 8-18(b). Even when the transistor begins to switch *on*, a finite time elapses before I_C reaches its maximum level. This is known as the *rise time* (t_r). The rise time is specified as the time required for I_C to go from 10% to 90% of its maximum level. As illustrated, the *turn-on time* (t_{on}), is the sum of t_d and t_r.



(a) Transistor base and collector currents

(b) Current waveform relationships

Figure 8-18
The turn-on time for a switching transistor is the sum of the delay time (t_d) and the rise time (t_r). The transistor turn-off time is the sum of the storage time (t_s) and the fall time (t_f).

When the input current is switched *off*, I_C does not go to zero until after a *turn-off time* t_{off}, made up of a *storage time* (t_s), and a *fall time* (t_f), as illustrated. The fall time is specified as the time required for I_C to go from 90% to 10% of its maximum level. The storage time is the result of charge carriers being trapped in the depletion region when a junction polarity is reversed. When a transistor is in a saturated *on* condition (see Section 5-10), both the collector-base and emitter-base junctions are forward biased. At switch-*off*, both junctions are reverse biased, and before I_C begins to fall, the stored charge carriers must be withdrawn or made to recombine with opposite-type charge carriers.

For a fast-switching transistor, t_{on} and t_{off} must be of the order of nanoseconds. The *2N3904* transistor data sheet portion in Fig. 8-19 specifies the following switching times: $t_d = 35$ ns, $t_r = 35$ ns, $t_s = 200$ ns, and $t_f = 50$ ns.

Characteristic		Symbol	Min	Max	Unit
Switching Characteristics (2N3904)					
Delay time	V_{CC} = 3 V, V_{BE} = 0.5 V,	t_d	—	35	ns
Rise time	I_C = 10 mA, I_{B1} = 1 mA	t_r	—	35	ns
Storage time	V_{CC} = 3 V, I_C = 10 mA,	t_s	—	200	ns
Fall time	$I_{B1} = I_{B2}$ = 1 mA	t_f	—	50	ns

Figure 8-19
Transistor switching times, as specified on a data sheet.

Example 8-7

The circuit shown in Fig. 8-18(a) uses a 2N3904 transistor and has an input pulse with a 5 μs pulse width (PW). Determine the time from commencement of I_t until it turns off.

Solution

I_t commences at t_d (at 10% of $I_{C(max)}$) after the start of the input pulse, and ceases at ($t_s + t_f$) (at 10% of $I_{C(max)}$) after the end of the input pulse.

$$t = PW - t_d + t_s + t_f = 5\ \mu s - 35\ ns + 200\ ns + 50\ ns$$
$$= 5.215\ \mu s$$

Practise Problems

8-5.1 Calculate the turn-*on* time and the turn-*off* time for a transistor with: t_d = 10 ns, t_r = 12 ns, t_s = 15 ns, t_f = 12 ns. Also, determine the time from commencement of a 100 ns input pulse to the end of the transistor *on* time.

8-6 *Transistor Circuit Noise*

Unwanted signals at the output of an electronics system are termed *noise*. The noise amplitude may be large enough to severely distort, or completely swamp, the wanted signals. Consequently, the noise level dictates the minimum signal amplitude that can be handled. Noise originates as atmospheric noise from outside the system and as circuit noise generated within resistors and devices.

Consider a conductive material at room temperature, (Fig. 8-20). The motion of free electrons drifting around within the material constitutes a flow of many tiny random electric currents. These currents cause minute voltage drops, which appear across the ends (or terminals) of the material. Because the number of free electrons available and the random motion of the electrons are both increased as temperature rises, the generated voltage amplitude is proportional to temperature. This unwanted, randomly varying voltage is termed *thermal noise*.

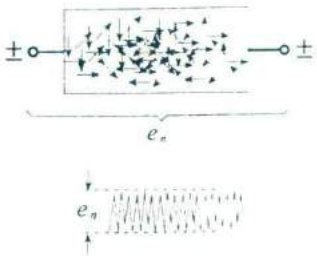


Figure 8-20
Noise voltages are generated within a resistor by random movements of electrons.

Thermal noise is generated within resistors, and when the resistors are at the input stage of an amplifier, the noise is amplified and produced as an output. Noise from other resistors is not amplified as much as that from the resistors right at the input; consequently, only the input stage resistors need be considered in noise calculations. Noise is also generated within a transistor, and like resistors, the input stage transistor is the most important because its noise is amplified more than that from any other stage.

Because thermal noise is an alternating quantity, its rms output level from any amplifier is dependent upon the bandwidth of the amplifier. It can be shown that the rms noise voltage generated in a resistance is,

$$e_n = \sqrt{4\,kTBR} \qquad \textbf{(8-12)}$$

where, k = *Boltzmann's constant* = 1.374×10^{-23} J/K
(i.e., joules per degree Kelvin)
T = absolute temperature (Kelvin)
R = resistance in ohms
B = circuit bandwidth

In the circuit shown in Fig. 8-21(a) R_1 and R_2 are bias resistors; e_s is a signal voltage with source resistance r_s. The total noise-generating resistance (R_G) in parallel with the amplifier input terminal is,

$$R_G = r_s \| R_2 \| R_2 \qquad \textbf{(8-13)}$$

In the noise equivalent circuit [Fig. 8-21(b)], e_n is the noise voltage generated by R_G. If the device input resistance is R_i, then the noise voltage is divided,

$$e_{ni} = e_n \times \frac{R_i}{R_i + R_G} \qquad \textbf{(8-14)}$$

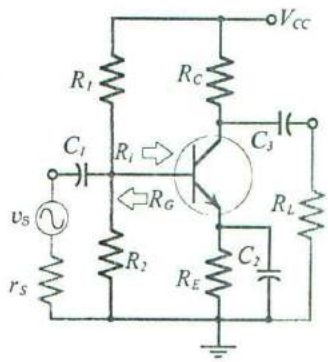
If the amplifier voltage gain is A_v, the output noise due to R_G is,

$$e_{no} = A_v\, e_{ni} \qquad \textbf{(8-15)}$$

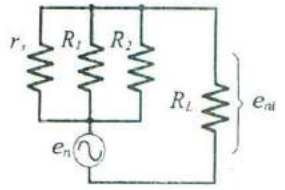
With a circuit collector resistance R_C and load resistance R_L, the noise output power produced by R_G is,

$$P_{nG} = \frac{e_{no}^2}{R_C \| R_L} \qquad \textbf{(8-16)}$$

To specify the amount of noise generated by a transistor, manufacturers usually quote a *noise figure* (*NF*). To arrive at this figure, the transistor noise output is measured under specified bias conditions and with a specified source resistance, temperature, and noise bandwidth. The noise figure defines the amount of noise added by the transistor to the noise generated by the specified resistance (R_G) at the input. Recall that R_G is the combined bias and signal source resistances, as seen from the amplifier input.



(a) *CE* amplifier circuit



(b) Equivalent noise input circuit

Figure 8-21
Thermal noise at the input of an amplifier depends upon the equivalent resistance of the bias and signal source resistances.

The data sheet portion in Fig. 8-22 specifies *spot noise figures* for a *2N4104* transistor. This means that the noise has been measured for a bandwidth of 1 Hz. The bias conditions are listed because the transistor noise can be affected by V_{CE} and I_C. Note that the specified I_C levels are very low (5 μA to 30 μA), because transistor noise increases with increasing current levels.

Noise Characteristics (2N4104)

Parameter	Test Conditions	Min	Max
NF spot noise figure	V_{CE} = 5 V, I_C = 30 μA, R_G = 10 kΩ, f = 10 Hz		15 dB
	V_{CE} = 5 V, I_C = 30 μA, R_G = 10 kΩ, f = 100 Hz		4 dB
	V_{CE} = 5 V, I_C = 5 μA, R_G = 50 kΩ, f = 1 kHz		1 dB
	V_{CE} = 5 V, I_C = 5 μA, R_G = 50 kΩ, f = 10 kHz		1 dB

Figure 8-22
Data sheet specification of noise characteristics for a 2N4104 transistor.

The *noise factor* (F) is the total circuit noise power output divided by noise output power from the source resistor.

$$F = \frac{P_{no}}{P_{nG}} \qquad \textbf{(8-17)}$$

The *noise figure* (NF) is the decibel value of F.

$$NF = 10 \log_{10} F \qquad \textbf{(8-18)}$$

Ideally, a transistor would add no noise to the circuit, and its noise figure would be zero. Obviously, the smallest possible transistor noise figure is the most desirable.

If the circuit in which the transistor is employed does not have the value of source resistance and the bias conditions specified, then the specified noise figure does not apply. In this case the noise figures can still be used to compare transistors, but for accurate estimations of noise, a new measurement of the noise figure must be made. From Eq. 8-17, the total noise output power due to R_G and the input transistor is,

$$P_{no} = F \times P_{nG} \qquad \textbf{(8-19)}$$

Example 8-8

Calculate the noise output voltage for the amplifier in Fig. 8-23 if the transistor is completely noiseless. The circuit voltage gain is 600, the base input resistance is 3 kΩ, and the cutoff frequencies are f_1 = 100 Hz and f_2 = 40 kHz. The circuit temperature is 25°C.

Solution

Eq. 8-13, $R_G = r_s \| R_1 \| R_2 = 30\ \text{k}\Omega \| 30\ \text{k}\Omega \| 30\ \text{k}\Omega$

$= 10\ \text{k}\Omega$

$T = 25°\text{C} = (273 + 25)\ \text{K}$

$= 298\ \text{K}$ (degrees Kelvin)

$B = f_2 - f_1 = 40\ \text{kHz} - 100\ \text{Hz}$

$= 39.9\ \text{kHz}$

Eq. 8-12, $e_n = \sqrt{4\,k\,T\,B\,R}$

$= \sqrt{4 \times 1.37 \times 10^{-23} \times 298 \times 39.9\ \text{kHz} \times 10\ \text{k}\Omega}$

$= 2.6\ \mu\text{V}$

Eq. 8-14, $e_{ni} = e_n \times \dfrac{R_i}{R_i + R_G} = 2.6\ \mu\text{V} \times \dfrac{3\ \text{k}\Omega}{3\ \text{k}\Omega + 10\ \text{k}\Omega}$

$= 0.59\ \mu\text{V}$

Eq. 8-15, $e_{no} = A_v\, e_{ni} = 600 \times 0.59\ \mu\text{V}$

$= 354\ \mu\text{V}$

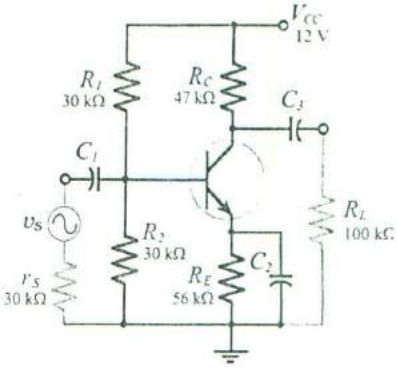


Figure 8-23
Circuit for Examples 8-8 and 8-9.

Example 8-9

The circuit in Ex. 8-8 uses a *2N4104* transistor with bias conditions of $I_C = 30\ \mu\text{A}$ and $V_{CE} = 5$ V. Calculate the total noise output voltage for the amplifier.

Solution

From Fig. 8-22, $NF = 4$ dB

From Eq. 8-18, $F = \text{antilog}\left[\dfrac{NF}{10}\right] = \text{antilog}\left[\dfrac{4\ \text{dB}}{10}\right]$

$= 2.51$

Eq. 8-19, $P_{no} = F \times P_{nG}$

so, $\dfrac{v_n^2}{R_C \| R_L} = F \times \dfrac{e_{no}^2}{R_C \| R_L}$

giving, $v_n = \sqrt{F} \times e_{no} = \sqrt{2.51} \times 354\ \mu\text{V}$

$= 560\ \mu\text{V}$

Practise Problems

8-6.1 A transistor circuit has $A_v = 800$, $B = 20$ kHz, $T = 40°\text{C}$, and $R_i = 2\ \text{k}\Omega$. Determine the noise output voltage produced by bias resistors with an equivalent resistance of 15 kΩ.

8-6.2 Calculate the total noise output voltage for the circuit in Problem 8-6.1 if the transistor has a noise figure of 6 dB.

8-7 Transistor Power Dissipation

Maximum Power Dissipation

Consider the portion of the data sheet for the *2N3903* and *2N3904* transistor reproduced in Fig. 8-24. The *total device dissipation* (P_D) is specified as 625 mW at a maximum ambient temperature (T_A) of 25°C. This means that ($V_{CE} \times I_C$) must not exceed 625 mW when the surrounding air temperature is 25°C. Figure 8-1 lists the maximum I_C and V_{CE} for the *2N3903* and *2N3904* as 40 V and 200 mA, respectively. If these two quantities exist simultaneously at the transistor, the power dissipation is,

$$P_D = V_{CE} \times I_C = 40 \text{ V} \times 200 \text{ mA}$$
$$= 8 \text{ W}$$

which is much greater than the 625 mW specified maximum.

If the maximum V_{CE} is used with a *2N3904* transistor, then the maximum collector current must not exceed,

$$I_C = \frac{P_{Dmax}}{V_{CE}} = \frac{625 \text{ mW}}{40 \text{ V}}$$
$$= 15.6 \text{ mA}$$

When the transistor has to pass the maximum I_C, the V_{CE} should be limited to,

$$V_{CE} = \frac{P_{Dmax}}{I_C} = \frac{625 \text{ mW}}{200 \text{ mA}}$$
$$= 3.1 \text{ V}$$

If the air temperature is greater than 25°C, the transistor maximum power dissipation must be derated. From Fig. 8-24, the *power derating factor* for *2N3903-2N3904* transistors is 5 mW/°C. This may be used to calculate the device maximum power dissipation at any air temperature.

$$P_{D(T2)} = P_{D(25°C)} - D(T_2 - 25°C) \qquad \textbf{(8-20)}$$

where D is the power dissipation derating factor.

2N3903, 2N3904

Total Device Dissipation @ T_A = 25°C	P_D	625	mW
Derate above 25°C		5	mW/°C

Figure 8-24
Power dissipation specification for low-power transistors.

Example 8-10

Calculate the maximum I_C level that may be used with a *2N3904* transistor at 55°C when V_{CE} is 10 V.

Solution

Eq. 8-20, $P_{D(T2)} = P_{D(25°C)} - D(T_2 - 25°C)$

$= 625 \text{ mW} - (5 \text{ mW/°C})(55°C - 25°C)$

$= 475 \text{ mW}$

$$I_C = \frac{P_D}{V_{CE}} = \frac{475 \text{ mW}}{10 \text{ V}}$$

$= 47.5 \text{ mA}$

The data sheet portion in Fig. 8-25 shows the voltage, current and power ratings for a *2N3055* high-power transistor. The maximum dissipation is specified as 115 W at a *case temperature* (T_C) of 25°C. Note that for a power transistor the *case* temperature is specified, instead of the air temperature. The derating factor is 0.667 W/°C.

2N3055 Silicon NPN transistor

Characteristic	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter - Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	115	Watts
Derate above 25°C		0.667	W/°C

Figure 8-25
Data sheet portion for 2N3055 power transistor.

The maximum power dissipation at any temperature may be calculated for the *2N3055* by use of Eq. 8-20. Alternatively, a *power derating graph* can be constructed for reading the device maximum power dissipation at any temperature. This is demonstrated in Ex. 8-11.

Example 8-11

Draw a power derating graph for a *2N3055* transistor, and determine the device maximum power dissipation at 100°C.

Solution

Prepare a horizontal temperature scale to 200°C, and a vertical power dissipation scale to 115 W, as in Fig. 8-26.

Plot point A at P_D = 115 W and T = 25 °C.

When $P_D = 0$, $T = 25°C + \frac{P_D}{D} = 25°C + \frac{15\ W}{0.667\ W/°C}$

$= 197°C$

Plot point B at $P_D = 0$ and $T = 197°C$.
Draw the power derating graph through points A and B.

From the graph, at $T = 100°C$,

$P_D = 65\ W$

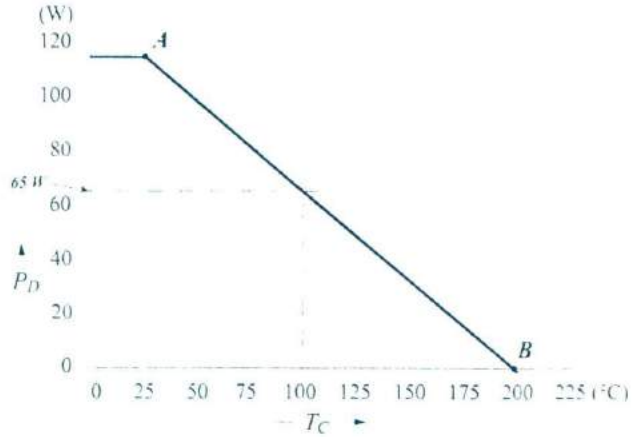


Figure 8-26
Power derating graph for 2N3055 transistor.

Maximum Power Dissipation Curve

When the maximum power that may be dissipated in a transistor is determined, the maximum I_C level may be calculated for any given V_{CE}, or vice versa. The corresponding voltage and current levels may be more easily determined by drawing a *maximum power dissipation curve* on the transistor output characteristics. To draw this curve, the greatest power that may be dissipated at the operating temperature is first calculated. Then, using convenient collector-emitter voltage levels, the corresponding collector current levels are calculated for the maximum power dissipation. Using these current and voltage levels the curve is plotted on the device characteristics. Example 8-12 demonstrates the process.

The transistor voltage and current conditions must at all times be maintained in the portion of the characteristics below the maximum power-dissipation curve. This means, for example, that all point on load lines must be below the curve.

Example 8-12

Draw a maximum power dissipation curve for $P_D = 80$ W on the I_C/V_{CE} characteristics in Fig. 8-27.

Solution

when $V_{CE} = 60$ V, $$I_C = \frac{P_D}{V_{CE}} = \frac{80\text{ W}}{60\text{ V}}$$
$$= 1.3\text{ A}$$

Plot point 1 on the characteristics at:

$$V_{CE} = 60\text{ V and } I_C = 1.3\text{ A}$$

when $V_{CE} = 40$ V, $$I_C = \frac{80\text{ W}}{40\text{ V}} = 2\text{ A} \quad \textit{(point 2)}$$

when $V_{CE} = 20$ V, $$I_C = \frac{80\text{ W}}{20\text{ V}} = 4\text{ A} \quad \textit{(point 3)}$$

when $V_{CE} = 10$ V, $$I_C = \frac{80\text{ W)}}{10\text{ V}} = 8\text{ A} \quad \textit{(point 4}$$

Draw the maximum power dissipation curve through the points on the graph.

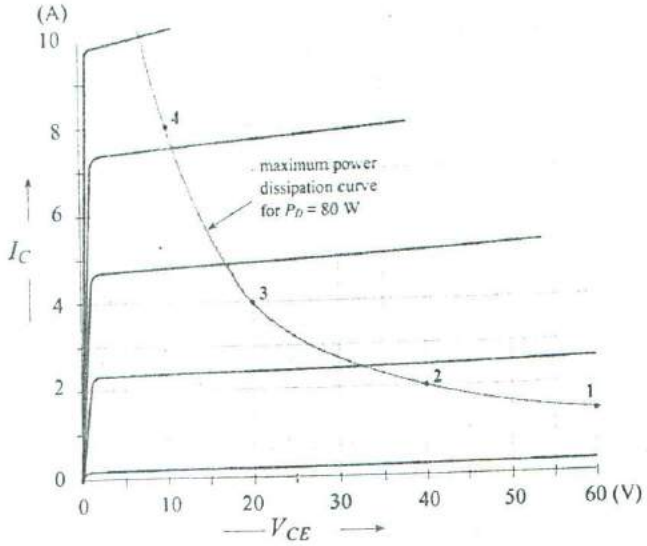


Figure 8-27 *Transistor maximum power dissipation curve drawn on the I_C/V_{CE} characteristics.*

Practise Problems

8-7.1 Draw a power derating graph for a transistor with $P_{D(25°C)} = 310$ mW and $D = 2.81$ mW/°C. Read the device maximum power dissipation at 80°C from the graph.

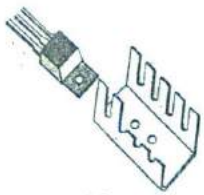
8-7.2 Using $V_{CE(max)} = 40$ V, determine four suitable points for drawing the maximum power dissipation curve for the transistor in Practise Problem 8-7.1 when $T_C = 75°C$.

8-8 Heat Sinking

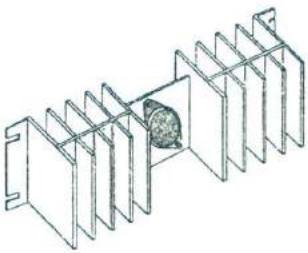
When power is dissipated in a transistor, the heat generated must flow from the collector-base junction to the case, and then to the surrounding atmosphere. When only a very small amount of power is involved, as in a small-signal transistor, the surface area of the transistor case is normally large enough to allow all of the heat to escape. For the large power dissipations that can occur in high-power transistors, the transistor surface area is not large enough. *Heat sinks* must be used to increase the area in contact with the atmosphere. For small transistors, the clip-on *star-type* heat sinks illustrated in Fig. 8-28(a) may be used. For higher-power transistors, sheet-metal and aluminum-extrusion heat sinks are available, as illustrated in Fig. 8-28(b) and (c).



(a) Clip-on type heat sink with *TO-18* transistor enclosure



(b) Sheet-metal heat sink with *TO-220* transistor



(c) Aluminum extrusion heat sink with *TO-3* transistor

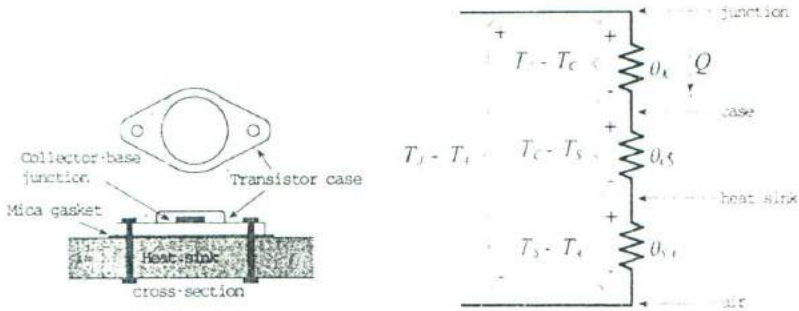
Figure 8-28
Heat sinks are used to conduct heat from a transistor case, to keep the device from overheating when power is dissipated.

Figure 8-29(a) shows the cross section of a transistor fastened to a heat sink. The heat generated at the collector-base junction must flow from the junction to the transistor case, then from the case to the heat sink, and finally from the heat sink to the surrounding air. In many cases, a mica gasket is inserted between the transistor case and the heat sink for electrical insulation, [see Fig. 8-29(a)]. Each portion of the path that the heat must pass through has a *thermal resistance*. These are:

θ_{JC} — *junction-to-case* thermal resistance
θ_{CS} — *case-to-sink* thermal resistance
θ_{SA} — *sink-to-air* thermal resistance

Figure 8-29(b) shows the *thermal equivalent circuit* for the transistor and heat sink. This consists of the three thermal resistances connected in series. The size of heat sink required for a transistor with a given power dissipation may be determined from the thermal equivalent circuit.

The temperature difference between the transistor collector-base junction and the air surrounding the heat sink ($T_J - T_A$) causes the dissipated power (Q) to flow through each of the thermal resistances in turn. The thermal resistance series circuit is analogous to an electrical series resistive circuit. The power flow in the thermal circuit is similar to the current flow in the electrical circuit. Also, the temperature drop across each thermal resistance is analogous to the voltage drop across each electrical resistance, [see Fig. 8-29(b)]. Ohm's Law may be applied to a thermal series circuit exactly as in the case of an electrical series circuit.



(a) Transistor and heat sink (b) Thermal resistance circuit

Figure 8-29
The thermal resistances between the collector-base junction of a transistor and the air surrounding the transistor heat sink constitute a series thermal circuit. The thermal equivalent of Ohm's Law may be applied for circuit analysis.

For an electrical series resistive circuit, $I = E/R$, or,

$$\text{current flow} = \frac{\text{Voltage difference}}{\text{total resistance}}$$

or

For a series thermal resistance circuit,

$$\text{power flow} = \frac{\text{temperature difference}}{\text{total thermal resistance}}$$

or,

$$Q = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} \qquad \textbf{(8-21)}$$

When the temperatures are in degrees Celsius (°C), and the thermal resistances are in *degrees Celsius per watt* (°C/W), Q is the power dissipated in watts (W).

Thermal Characteristic (2N3055)

Characteristic		Max	Unit
Junction-to-case thermal resistance	θ_{JC}	1.52	°C/W

Figure 8-30
Portion of 2N3055 data sheet showing the transistor junction-to-case thermal resistance.

The value of θ_{JC} depends upon the transistor case style, and it is usually specified on the data sheet. See the *2N3055* data sheet portion in Fig. 8-30. θ_{CS} is dependent on the transistor case and

on the mechanical contact between the case and the heat sink. The contact may be *dry*, have a layer of heat-conducting compound, or have an insulating gasket. Table 8-1 shows typical θ_{CS} values for three case styles and three contact conditions. θ_{SA} is determined by the size and style of the heat sink, (see Table 8-2 and Appendix 1-10).

Table 8-1 *Typical case-to-sink thermal resistances for various mechanical connections*

transistor case	θ_{CS} (°C/W) metal-to-metal dry	θ_{CS} (°C/W) metal-to-metal with compound	θ_{CS} (°C/W) with mica insulator and compound
TO-220	1.2	0.7	1.0
TO-3	0.6	0.4	0.5
TO-66	1.5	0.5	2.3

Equation 8-21 may be used to calculate θ_{SA} when all other quantities are known. The smallest heat sink with a thermal resistance equal to or lower than the calculated value is then selected. Alternatively, when a given heat sink is used, Eq. 8-20 may be applied to calculate the transistor junction temperature.

Table 8-2 *Typical sink-to-air thermal resistances for various heat sinks*

Heat sink style	Transistor case	*Wakefield* heat sink type	Natural convection θ_{SA}	Natural convection θ_{SA}
Star-type clip-on	TO-18	201	65°C/W	65°C @ 1 W
Sheet metal with fins	TO-220	289	25°C/W	50°C @ 2 W
Aluminum extrusion	TO-3	401	2.7°C/W	80°C @ 30 W
" "	"	403	1.8°C/W	55°C @ 30 W
" "	"	421	1.2°C/W	58°C @ 50 W
" "	"	423	0.94°C/W	47°C @ 50 W
" "	"	441	0.59°C/W	47°C @ 80 W
" "	"	621	5°C/W	75°C @ 15 W

Another method used to specify heat sink thermal resistances is shown in Table 8-2. For the *Wakefield 621* heat sink, θ_{SA} is listed as *75°C at 15 W* for natural convection. This means that the maximum temperature difference between the case and the

surrounding air will be 75°C when the heat sink is dissipating 15 W. This can be redefined as.

$$\theta_{SA} = \frac{75°C}{15\ W} = 0.5°C/W$$

Example 8-13

A transistor with $V_{CE} = 20$ V and $I_C = 1$ A has a 1°C/W junction-to-case thermal resistance. The *TO-3* case is fastened directly to the heat sink, and conducting compound is used. Calculate the thermal resistance for a heat sink that will keep the maximum junction temperature at 90°C when the ambient temperature is 25°C. Select a suitable heat sink from Appendix 1-10.

Solution

$$Q = V_{CE} I_C = 20\ V \times 1\ A$$
$$= 20\ W$$

From Table 8-1, $\theta_{CS} = 0.4$ °C/W (*TO-3* case, direct contact with compound)

From Eq. 8-21,

$$\theta_{SA} = \frac{T_J - T_A}{Q} - \theta_{JC} - \theta_{CS}$$
$$= \frac{90°C - 25°C}{20\ W} - 1°C/W - 0.4°C/W$$
$$= 1.85°C/W$$

From Table 8-2 (and Appendix 1-10), the *403*, *421*, *423*, and *441* all have θ_{SA} less than 1.85°C/W for natural convection. Select the smaller and least expensive of the three — the *403*.

Practise Problems

8-8.1 A *2N6121* transistor (see Appendix 1-9) is fastened to a heat sink with the use of a mica insulator and compound. Calculate the thermal resistance of a suitable heat sink if the device is to dissipate 10 W, and the maximum junction temperature is to be 100 °C. The ambient temperature is 25°C.

8-8.2 A *TO-3* style transistor with $T_{J(max)} = 140$ °C and $\theta_{JC} = 0.6$°C/W is fastened dry to a heat sink with $\theta_{CA} = 1.3$ °C/W. Determine the maximum power that may be dissipated when $T_A = 40$°C.

Chapter-8 Review Questions

Section 8-1

8-1 Define the following *BJT* quantities listed on a device data sheet: V_{CBO}, V_{CEO}, V_{EBO}, $V_{CE(sat)}$.

8-2 Define the following *BJT* quantities: I_C, I_{CBO}, I_{CO}, h_{FE}, h_{fe}.

Section 8-2

8-3 Write the equations for determining power gains and power level changes in decibels: (a) when two power levels are measured, (b) when two voltage levels are measured.

8-4 Sketch a typical frequency response graph for an amplifier, and identify the upper and lower cutoff frequencies and the bandwidth. Briefly explain.

Section 8-3

8-5 Define $f_{\alpha e}$, $f_{\alpha b}$, and f_T for a *BJT*. Briefly explain.

8-6 Explain *CB* and *CE* junction capacitances, and identify the quantities that determine junction capacitance values.

8-7 Describe Miller effect, and derive an equation for the input capacitance of an inverting amplifier.

Section 8-4

8-8 Identify the quantities that cause the gain of an amplifier to fall of at low frequencies. Briefly explain.

8-9 Discuss the quantities that cause the gain of an amplifier to fall off at high frequencies.

Section 8-5

8-10 Sketch the waveforms of input and output currents for a switching transistor. Show the various switching times involved and explain the origin of each.

Section 8-6

8-11 Explain thermal noise, and discuss the effect of resistor noise at the input of a transistor. Also, define noise figure and noise factor for a transistor.

Section 8-7

8-12 Sketch a typical power-temperature derating graph for a transistor. Briefly explain.

8-13 Describe how a transistor maximum power dissipation graph may be drawn on the I_C/V_{CE} characteristics.

Section 8-8

8-14 Sketch the cross section of a power transistor and heat sink. Identify the thermal resistances in the power dissipation path.

8-15 Draw the thermal resistance equivalent circuit for a transistor and heat sink, and write the equation relating power dissipation, temperature difference, and thermal resistance.

Chapter-8 Problems

Section 8-1

8-1 From Appendix 1-9, determine the following quantities for a *2N6125* transistor: maximum V_{CE}, maximum collector current, maximum V_{BE}, $h_{FE(max)}$ and $h_{FE(min)}$ at $I_C = 1.5$ A.

8-2 From the *2N3055* data sheet in Appendix 1-8, determine the following quantities: maximum collector-base voltage, maximum collector current, maximum emitter-base voltage, h_{FE} minimum and h_{FE} maximum at $I_C = 4$ A.

Section 8-2

8-3 The output power from an amplifier is 100 mW when the signal frequency is 1 kHz. When the signal frequency is increased to 25 kHz, the output power falls to 75 mW. Calculate the decibel change in output power.

8-4 Calculate the power gain for an amplifier with equal input and load resistances when $v_i = 100$ mV and $v_o = 3$ V.

8-5 The output voltage of an amplifier is 2 V when the signal frequency is 1 kHz. Calculate the new level of output voltage when it has fallen by 4 dB.

Section 8-3

8-6 The input capacitance of a *CE* circuit is measured as 800 pF. The circuit has $R_C = 7$ kΩ, and the device parameters are: $h_{fe} = 60$, $h_{ie} = 1.5$ kΩ. If the base-emitter capacitance is 15 pF, calculate the collector-base capacitance.

8-7 A transistor with $h_{fe} = 100$, $h_{ie} = 2.2$ kΩ, $C_{cb} = 3$ pF, $I_C = 1.2$ mA, and $f_T = 4$ MHz is connected as a *CE* amplifier with $R_C \| R_L = 6.8$ kΩ. Calculate the amplifier input capacitance.

8-8 Calculate the new value of C_{in} for the amplifier in Problem 8-7 when a 100 pF capacitor is connected (a) between emitter and base, (b) between collector and base.

8-9 A common emitter amplifier has $A_v = 50$, $C_{in} = 414$ pF, and $C_{bc} = 8$ pF. Determine the base-emitter capacitance.

Section 8-4

8-10 The circuit in Problem 8-7 uses voltage divider bias with $R_1 = 56$ kΩ and $R_2 = 15$ kΩ. The signal source resistance is 3.3 kΩ. Calculate the input capacitance limited upper cutoff frequency for the circuit.

8-11 Repeat Problem 8-10 for the circuit connected to function as a *CB* amplifier.

8-12 A voltage divider bias circuit (as in Fig. 8-23) has the following components: $R_1 = 68$ kΩ, $R_2 = 47$ kΩ, $R_C = 5.6$ kΩ, $R_E = 4.7$ kΩ. The supply voltage is 12 V, and the transistor has: $f_T = 35$ MHz, $C_{bc} = 3.5$ pF. Determine the input capacitance limited upper cutoff frequency when the circuit

is connected as a *CE* amplifier with R_E bypassed. The signal source resistance is 1.5 kΩ.

8-13 Repeat Problem 8-12 for the circuit employed as a *CB* amplifier with the transistor base bypassed to ground.

8-14 The circuit in Problem 8-12 is modified to function as an emitter follower with R_C shorted and the output taken from the emitter. Determine the input capacitance limited upper cutoff frequency for the circuit.

8-15 A transistor employed in an amplifier has $h_{fe} = 75$ and $f_{ab} = 12$ MHz. The collector load is $R_C \| R_L = 20$ kΩ, and there is 100 pF stray capacitance at the output. Determine the stray capacitance limited upper 3 dB frequency.

8-16 A transistor amplifier with $R_C \| R_L = 15$ kΩ has a 75 kHz upper 3 dB frequency. Assuming that f_2 is determined by the stray capacitance at the transistor collector terminal, calculate the value of the stray capacitance.

Section 8-5

8-17 Determine the turn-on and turn-off times for a switching circuit with *2N3251* transistor, (see Appendix 1-7).

8-18 If the circuit in Problem 8-17 has a 2 kHz square wave input at the transistor base, calculate the time from the collector current first reaches 90% of its maximum level until it falls to 10% of maximum.

8-19 A switching circuit is to be turned *on* and *off* by a 1 MHz square wave input. The output rise and fall times are not to exceed 10% of the transistor *on* time. Determine the maximum value for t_r and t_f.

Section 8-6

8-20 An amplifier with a *2N4104* input transistor (see Fig. 8-22) has 3 dB points at 2 kHz and 10 kHz, respectively. The transistor bias conditions are $V_{CE} = 5$ V and $I_C = 5$ μA, and the amplifier voltage gain is 40. Calculate the noise output voltage at 25°C if $R_G = 50$ kΩ and $R_i = 10$ kΩ.

8-21 A transistor amplifier with $A_v = 100$, $B = 15$ kHz, and $R_i = 12$ kΩ has input bias resistors equivalent to $R_G = 33$ kΩ. If the maximum noise voltage at the output is not to exceed 100 μV, determine the largest tolerable noise figure for the input transistor.

8-22 An amplifier with $B = 10$ kHz, $R_G = 5$ kΩ, and $R_i = 3.3$ kΩ has a maximum output noise of 150 μV. Assuming that the transistor is noiseless, determine the amplifier voltage gain.

Section 8-7

8-23 Calculate the maximum ambient temperature for a transistor with a 200 mW power dissipation if $P_{D(25°C)} = 310$ mW, and $D = 2.81$ mW/°C

8-24 The device in Problem 8-23 is to be operated at 80°C maximum ambient, and is to have a 5 mA collector current. Determine the maximum V_{CE} level that may be used.

8-25 Referring to the data sheet in Appendix 1-9, draw a power derating graph for a *2N6121* transistor, and determine the maximum power dissipation at a case temperature of 75°C.

8-26 Calculate the maximum case temperature for a *2N3251* transistor when its power dissipation is 0.25 W.

8-27 A 2N3055 transistor is to be operated at a maximum case temperature of 125°C. Construct a suitable I_C/V_{CE} graph, and draw the maximum power dissipation curve for the device at this temperature.

8-28 For the P_D = 80 W maximum power dissipation curve in Fig. 8-27, draw the dc load line for the smallest possible value of R_C when the circuit supply voltage is 50 V. Determine the value of $R_{C(min)}$.

Section 8-8

8-29 A *2N3055* transistor has V_{CE} = 10 V and I_C = 500 mA. The case temperature is not to exceed 30°C when the ambient is 25°C. The device is fastened to a heat sink using a mica gasket and compound. Calculate the maximum sink-to-air thermal resistance for a suitable heat sink.

8-30 A *2N3055* transistor dissipating 9 W is directly fastened to a *NC403* heat sink using compound, (see Appendix 1-10). If the ambient temperature is 25°C, calculate the transistor case temperature and junction temperature.

8-31 A *2N4900* transistor has a specified maximum power dissipation of 25 W at a case temperature of 25°C, and a derating factor of 0.143 W/°C. If the transistor is to dissipate 20 W, determine its maximum case temperature and calculate the maximum sink-to-air thermal resistance for a suitable heat sink. Assume that the *TO-66* case is directly connected to the heat sink using compound.

8-32 A *TO-220* case style transistor with V_{CE} = 30 V and I_C = 500 mA is fastened to a heat sink using a mica gasket and compound. Calculate the maximum sink-to-air thermal resistance for a suitable heat sink if the transistor maximum junction temperature is 150°C and the junction-to-case thermal resistance is 2.7°C/W.

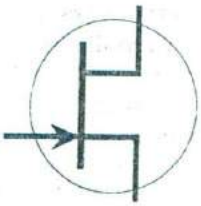
Practise Problem Answers

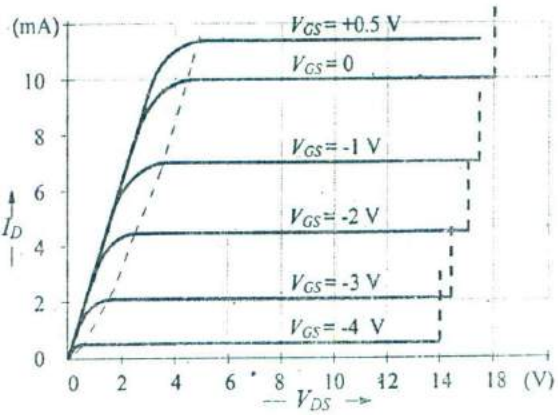
8-1.1 90, 100, 40 V, 5 V, 6 dB
8-2.1 -12 dB
8-3.1 4.86 nF
8-4.1 191 kHz

8-4.2 49.7 pF
8-5.1 22 ns, 27 ns, 127 ns
8-6.1 2.14 mV
8-6.2 4.28 mV
8-7.1 (310 mW, 25°C), (0, 135°C)
8-7.2 (40 V, 4.24 mA), (30 V, 5.65 mA),
(20 V, 8.48 mA), (10 V, 16.95 mA)
8-8.1 3.38°C/W
8-8.2 40 W

Chapter 9

Field Effect Transistors





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Objectives

You will be able to:

1. *Explain the operation of n-channel and p-channel junction field effect transistors (JFETs).*
2. *Draw typical JFET characteristics. Identify the regions of the characteristics and all important current and voltage levels.*
3. *For JFETs, define: saturation current, pinch-off voltage, forward transfer admittance, output admittance, and drain-source ON resistance.*
4. *Determine JFET parameter values from manufacturer's data sheets.*
5. *From the data sheet information, draw the maximum and minimum transfer characteristics for any given JFET type number.*
6. *Solve problems involving JFET characteristics and parameters.*
7. *Show how a JFET can be used for voltage amplification.*
8. *Explain the operation of enhancement-mode and depletion-enhancement-mode MOSFETs.*
9. *Draw typical drain and transfer characteristics for MOSFETs, and discuss the differences between MOSFETs and JFETs.*
10. *Solve problems involving MOSFET characteristics and parameters.*
11. *Explain the operation of VMOSFETs, sketch typical characteristics, and discuss the advantages of VMOS.*
12. *Sketch circuit symbols for JFETs, MOSFETs, and VFETs. Identify all terminals, current directions, and voltage polarities.*

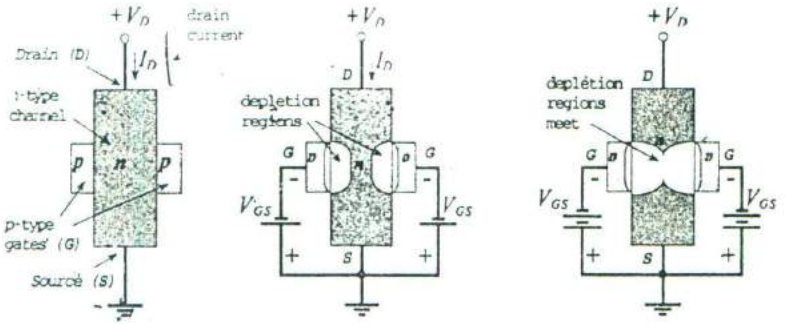
Introduction

A *field effect transistor (FET)* is a voltage-operated device that can be used in amplifiers and switching circuits, similarly to a bipolar transistor. Unlike a bipolar transistor, a *FET* requires virtually no input current. This gives it an extremely high input resistance, which is its most important advantage over a bipolar transistor. There are two major categories of field effect transistors: *junction FETs* and *MOSFETS*. These are further subdivided into *p*-channel and *n*-channel devices.

9-1 Junction Field Effect Transistors

n-Channel JFET

The operating principle of an *n-channel junction field effect transistor (JFET)* is illustrated by the block representation in Fig. 9-1(a). A piece of *n*-type semiconductor material, referred to as the *channel*, is sandwiched between two smaller pieces of *p*-type (the *gates*). The ends of the channel are designated the *drain* (*D*) and the *source* (*S*), and the two pieces of *p*-type material are connected together and their terminal is named the *gate* (*G*).



(a) No gate-source bias voltage

(b) Small negative gate-source bias voltage

(c) Large negative gate-source bias voltage

Figure 9-1
An n-channel JFET consists of an n-type channel with p-type gate regions on each side.

With the gate left unconnected, and a drain-source voltage (V_D) applied (positive at the drain, negative at the source), a *drain current* (I_D) flows, as shown in Fig. 9-1(a). When a gate-source voltage (V_{GS}) is applied with the gate negative with respect to the source [Fig. 9-1(b)], the gate-channel *pn*-junctions are reverse biased. The channel is more lightly doped than the gate material, so the depletion regions penetrate deep into the channel. Because the depletion regions are regions depleted of charge carriers, they behave as insulators. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced. When the negative gate-source bias voltage is further increased, the depletion regions meet as the centre of the channel [Fig. 9-1(c)], and I_D is cut off.

An *ac* signal applied to the gate causes the reverse gate-source voltage to increase as the instantaneous level of the signal goes negative, and to decrease when the signal is positive-going. This causes the gate-channel depletion regions to successively widen and decrease. When the signal goes negative, the depletions widen, the channel resistance is increased, and the drain current decreases. As the signal goes positive, the depletion regions recede, the channel resistance is reduced, and the drain current increases. It is seen that the *FET* gate-source voltage controls the drain current. The gate-channel *pn*-junctions are maintained in reverse bias, so the gate current is normally extremely low; much lower than the base current for a bipolar transistor.

The name, *field effect transistor*, comes from the fact that the depletion regions in the channel are produced by the electric field at the reverse-biased gate-channel junctions. The term *unipolar device* is sometimes applied to a *FET*, because, unlike a bipolar transistor, the current consists of only one type of charge carrier; electrons in the case of an *n*-channel device.

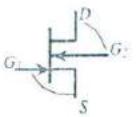
Circuit symbols for an *n*-channel *JFET* are shown in Fig. 9-2. As in the case of all semiconductor device symbols, the arrowhead points from *p*-type to *n*-type. For an *n*-channel device, the arrowhead points from the *p*-type gate to the *n*-type channel. This is the direction of conventional current flow if the junctions become forward-biased. Some device manufacturers use the symbol in Fig. 9-2(a) with the gate directly opposite the source terminal. Others show the gate centralised between the drain and source [Fig. 9-2(b)]. This can sometimes make circuit diagrams confusing unless the drain and source terminals are clearly identified. The symbol in Fig. 9-2(c) is used where the terminals of the two gate regions are provided with separate connecting leads. In this case, the device is referred to as a *tetrode-connected FET*.



(a) Circuit symbol for *n*-channel *JFET*



(b) Alternative circuit symbol



(c) Tetrode-connected *JFET*

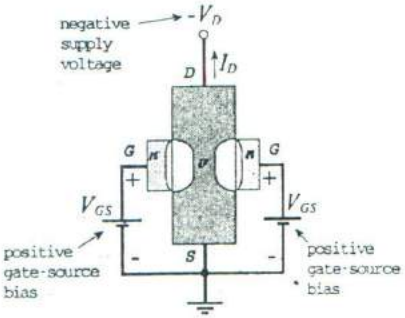
Figure 9-2
Circuit symbols for an n-channel JFET. As with all semiconductor symbols, the arrowheads point from the p-type to the n-type material.

p-Channel JFET

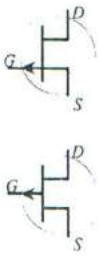
In a *p*-channel *JFET*, shown in block form in Fig. 9-3(a), the channel is *p*-type semiconductor, and the gates are *n*-type. The drain-source voltage (V_D) is applied negative to the drain, positive to the source, as illustrated, and the drain current flows (in the conventional direction) from source to drain. To reverse-bias the gate-channel junctions, the *n*-type gate regions must be made positive with respect to the *p*-type channel. So, the bias voltage is applied positive on the gate terminals, negative on the source.

A positive-going signal at the gate terminal of a *p*-channel *JFET* increases in the gate-channel junction reverse bias, causing the depletions regions to penetrate further into the channel. This increases the channel resistance and decreases the drain current. Conversely, a negative-going signal narrows the depletion regions, reduces the channel resistance, and increases the drain current.

Circuit symbols for a *p*-channel *JFET* are shown in Fig. 9-3(b). The arrowheads again point from the *p*-type material to the *n*-type; in this case, from the *p*-type channel to the *n*-type gate.



(a) *p*-channel *JFET*



(b) Circuit symbols for *p*-channel *JFET*

Figure 9-3
A p-channel JFET operates in exactly the same way as an n-channel device, except that the current directions and voltage polarities are reversed.

JFET Fabrication and Packaging

Junction field-effect transistors are normally manufactured by the diffusion process, (see Chapter 7). This type of construction is illustrated in Fig. 9-4. Starting with a *p*-type substrate, an *n*-channel is diffused, then, *p*-type impurities are diffused into the channel. Finally, metal terminal connections are deposited through holes in the silicon dioxide surface, as illustrated.

The *n*-type region is the *FET* channel, and the two *p*-type regions constitute the gates. With this symmetrical construction, the drain and source terminals are interchangeable. Other fabrication techniques produce device geometry that is not symmetrical. In these cases, interchanging the drain and source terminals would radically affect the device performance characteristics.

Figure 9-5 shows several *FET* packages which are similar to *BJT* enclosures. Note the device terminal identifications in each case.

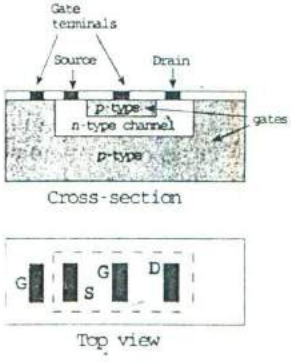


Figure 9-4
Cross-section and top view of n-channel JFET. With this type of construction, the drain and source are interchangable.

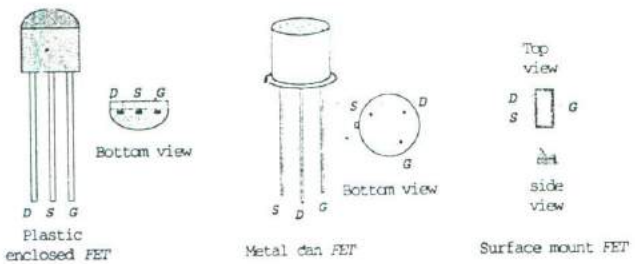


Figure 9-5
Various JFET enclosures

Section 9-1 Review

9-1.1 Sketch a block representation of an *n*-channel *JFET*. Indicate voltages and current direction, and explain the device operation.

9-1.2 Repeat Question 9-1.1 for a *p*-channel *JFET*.

9-1.3 Sketch circuit symbols for *n*-channel and *p*-channel *JFETs*. Identify the terminals and briefly explain.

9-2 JFET Characteristics

Depletion regions

An *n*-channel *JFET* block representation is shown in some detail in Fig. 9-6. With a drain-source voltage applied as illustrated, I_D flows in the direction shown producing voltage drops along the channel. Consider the voltage drops from the source terminal (S) to points *A*, *B*, and *C* within the channel. Point *A* is positive with respect to the source; alternatively, it can be stated that *S* is negative with respect to *A*. Because the gate blocks are connected to S, the gates are negative with respect to point *A* by a voltage V_A. This causes the depletion regions to penetrate into the channel by an amount proportional to V_A.

The voltage drop between point *B* and the source is V_B, which is less than V_A. Consequently, at point *B* on the channel the gates are at $-V_B$ with respect to the channel, and the depletion region penetration is less than at point *A*. From point *C* to the source terminal, the voltage drop (V_C) is less than V_B. Thus, the gate-channel reverse bias (at point *C*) is V_C volts, and the depletion region penetration is less than at point *A* or *B*. The differing voltage drops along the channel, and the resulting variation in gate-channel reverse bias, accounts for the shape of the depletion region penetration of the channel.

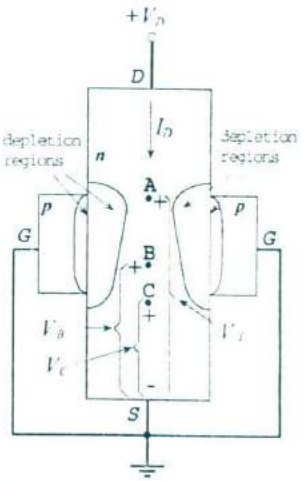


Figure 9-6
Drain current in an n-channel JFET causes voltage drops along the channel which reverse bias the gate channel junctions. This produces different levels of depletion region penetration into the channel.

Drain Characteristics with $V_G = 0$

Figure 9-7 shows a circuit for determining the drain current versus drain-source voltage characteristic for an *n*-channel *JFET* with $V_{GS} = 0$. V_{DS} is increased in convenient steps from zero, and I_D is measured at each V_{DS} level. This produces a table of I_D/V_{DS} values for plotting the characteristic shown in Fig. 9-8.

Referring to the characteristic, it is seen that when $V_{DS} = 0$, $I_D = 0$. There is no channel voltage drop, so the voltage between the gate and all points on the channel is zero, and there is no depletion region penetration. When V_{DS} is increased by a small amount (less than 1 V), a small drain current flows producing some voltage drop along the channel. This results in some depletion penetration of the channel (as explained for Fig. 9-6), but it is so small that it has no significant effect on the channel resistance. With further small increases in V_{DS} the drain current increase is approximately linear, and the channel behaves as an almost constant-value resistance, (see Fig. 9-8).

The channel continues to behave as a fixed-value resistance until the voltage drops along it become large enough to produce considerable depletion region penetration. At this stage the channel resistance begins to be affected by the depletion regions. Further increases in V_{DS} now produce smaller I_D increases, as shown by the curved part of the characteristic. The increased I_D levels, in turn, cause more depletion region penetration and greater channel resistance. Eventually, a *saturation level* of I_D is reached where further V_{DS} increase seems to have no effect on I_D.

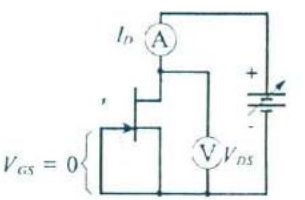


Figure 9-7
Circuit for obtaining the I_D/V_{DS} characteristic for an n-channel junction field effect transistor with $V_{GS} = 0$.

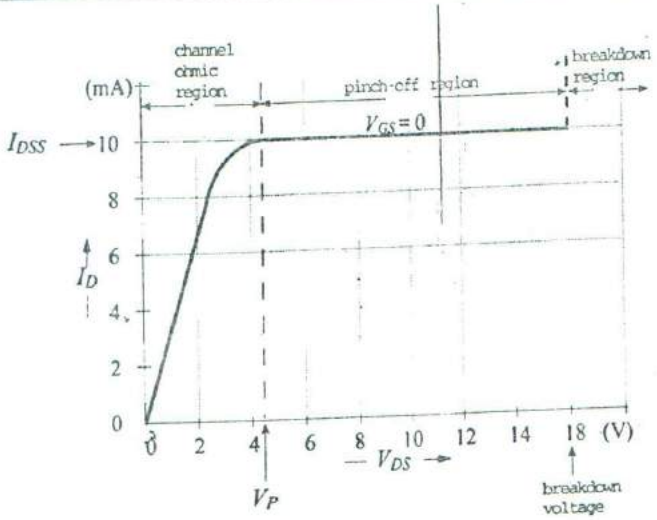


Figure 9-8
I_D/V_{DS} characteristic for an n-channel JFET with $V_{GS} = 0$.

At the point on the characteristic where I_D levels off, the drain current is referred to as the *drain-source saturation current* (I_{DSS}). (10 mA in Fig. 9-8). The shape of the depletion regions in the channel at the I_{DSS} level is such that they appear to *pinch off* the channel, (see Fig. 9-6). So, the drain source voltage at this point is termed the *pinch-off voltage* (V_p). (4.5 V in Fig. 9-8.) The region of the characteristic where I_D is constant is called the *pinch-off region*, as illustrated. The channel mostly behaves like a resistance between $V_{DS} = 0$ and $V_{DS} = V_p$, so this part of the characteristic is referred to as the *channel ohmic region*.

If V_{DS} is continuously increased (in the pinch-off region) a voltage is reached at which the (reverse-biased) gate-channel junctions break down, (see Fig. 9-8). When this occurs, I_D increases rapidly, and the device might be destroyed. The pinch-off region of the characteristic is the normal operating region for the *FET*.

Drain Characteristics with External Bias

A circuit for obtaining the I_D/V_{DS} characteristics for an *n*-channel *JFET* when an external gate-source bias (V_{GS}) is applied is shown in Fig. 9-9. In this case, V_{GS} is set to a convenient (negative) level (such as -1 V). V_{DS} is increased in steps, and the corresponding level of I_D is noted at each V_{DS} step. The I_D/V_{DS} characteristic for $V_{GS} = -1$ V is then plotted as illustrated in Fig. 9-10.

When a -1 V external gate-source bias voltage is applied, the gate-channel junctions are reverse biased even when $I_D = 0$. So, when $V_{DS} = 0$ the depletion regions are already penetrating to some depth into the channel. Because of this, a smaller voltage drop along the channel (smaller than when $V_{GS} = 0$) will increase the depletion regions to the point at which they produce channel pinch-off. Consequently, with $V_{GS} = -1$ V the pinch-off voltage is reached at a lower I_D level than when $V_{GS} = 0$. The $V_{GS} = -1$ V characteristic in Fig. 9-10 has $V_p = 3.5$ V.

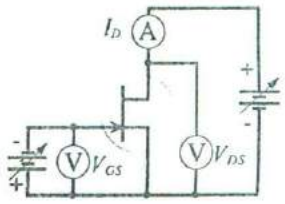


Figure 9-9
Circuit for obtaining the I_D/V_{DS} characteristic for an n-channel junction field effect transistor with various gate-source bias voltages.

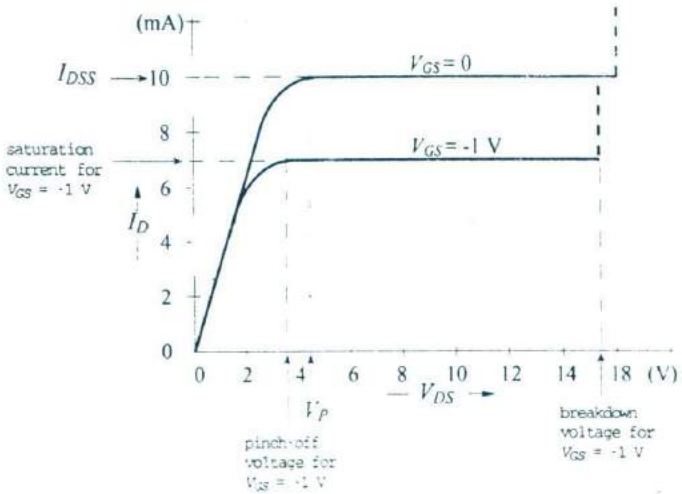


Figure 9-10
I_D/V_{DS} characteristics for V_{GS} = 0 and for V_{GS} = -1 V for an n-channel JFET.

A family of *drain characteristics* can be obtained by using several levels of negative gate-source bias voltage, (see Fig. 9-11). If a positive V_{GS} is used, a higher level of I_D can be produced, as shown by the characteristic for V_{GS} = +0.5 V. However, V_{GS} is normally kept negative to avoid the possibility of forward biasing the gate-channel junctions.

The dashed line on the characteristics in Fig. 9-11 is drawn through the points at which I_D saturates for each level of gate-source bias voltage. When V_{GS} = 0, I_D saturates at I_{DSS}, and the characteristic shows V_P = 4.5 V. When a -1 V external bias is applied, the gate-channel junctions still require -4.5 V to achieve pinch-off. This means that a 3.5 V drop is now required along the channel instead of 4.5 V, and the lower voltage drop is achieved with a lower level of I_D. Similarly, when V_{GS} = -2 V and - 3 V, pinch-off is achieved with 2.5 V and 1.5 V, respectively, along the channel. The 2.5 V and 1.5 V drops are, of course, obtained with further reduced I_D levels.

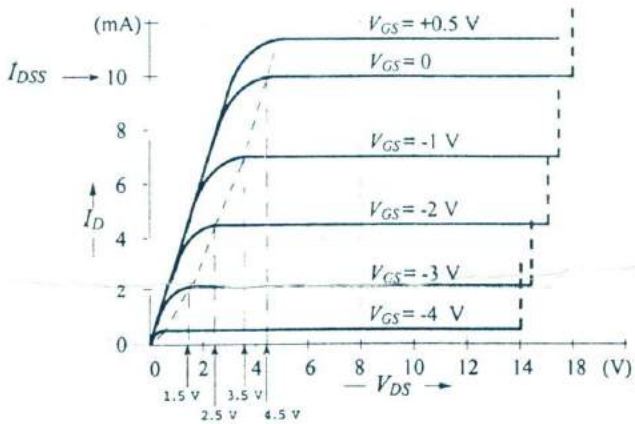


Figure 9-11
Family of I_D/V_{DS} characteristics for an n-channel JFET with various levels of V_{GS}.

Suppose a -4.5 V gate-source bias is applied to a device with the characteristics shown in Fig. 9-11. This is a V_{GS} level equal to the pinch-off voltage V_P. Without any additional channel voltage drop produced by I_D, the depletion regions penetrate so deep into the channel that they meet in the middle, completely cutting I_D *off*. So, a gate-source bias equal to the pinch-off voltage reduces I_D to zero. The bias voltage required to do this is termed the *gate cutoff voltage* ($V_{GS(off)}$), and, as explained, $V_{GS(off)} = V_P$. Note on Fig. 9-11 that the drain-source voltage at which breakdown occurs is reduced as the negative gate-source bias voltage is increased. This is because $-V_{GS}$ adds to the reverse bias at the junctions.

Example 9-1

Plot the I_D/V_{DS} characteristic for a *JFET* from the following table of values obtained with $V_{GS} = 0$. Determine I_{DSS} and V_P from the characteristics.

V_{DS} (V)	0	1	2	2.5	3	3.5	3.75	4	6	9
I_D (mA)	0	3	6	7	7.5	7.8	8	8	8	8

Solution

On Fig. 9-12, plot *point 1* at $V_{DS} = 0$ and $I_D = 0$
Plot *point 2* at $V_{DS} = 1$ V and $I_D = 3$ mA
and so on through $V_{DS} = 9$ V and $I_D = 8$ mA
Draw the drain characteristic for $V_{GS} = 0$ through *pints 1* through *10*.

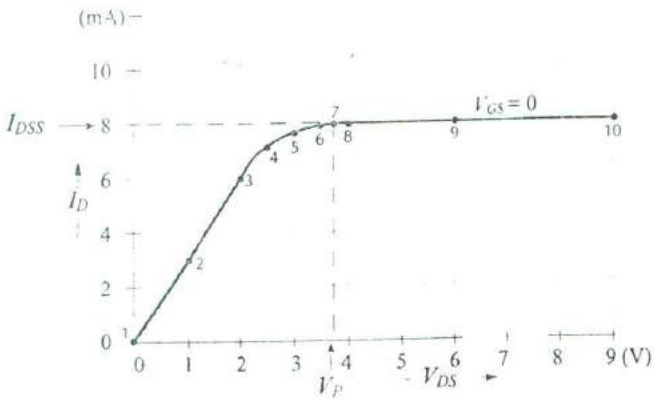
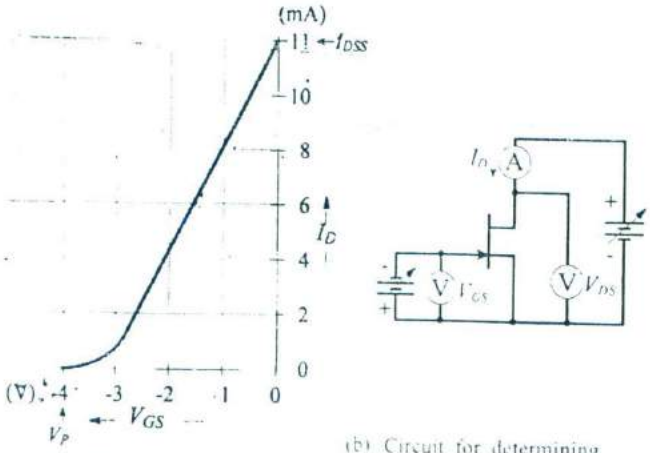


Figure 9-12
FET characteristics for Ex. 9-1.

From the characteristic, $I_{DSS} = 8$ mA and $V_P = 3.75$ V

Transfer Characteristics

The *transfer characteristics* for an *n*-channel *JFET* are a plot of I_D versus V_{GS}. The gate-source voltage of a *FET* controls the level of the drain current, so, the transfer characteristic shows how I_D is controlled by V_{GS}. As illustrated in Fig. 9-13(a), the transfer characteristic extends from $I_D = I_{DSS}$ at $V_{GS} = 0$, to $I_D = 0$ at $V_{GS} = V_P$.



(a) Transfer characteristic

(b) Circuit for determining the transfer characteristic

Figure 9-13
The transfer characteristics for a FET are a plot of I_D versus V_{GS}.

Figure 9-13(b) shows a circuit for experimentally determining a table of quantities for plotting the transfer characteristic of a given *FET*. The drain-source voltage is maintained constant, V_{GS} is adjusted in convenient step, and the corresponding levels of V_{GS} and I_D are recorded. The characteristic shows that, as $-V_{GS}$ is increased, I_D is progressively reduced from I_{DSS} at $V_{GS} = 0$, to $I_D = 0$ at $V_{GS} = -V_P$.

The transfer characteristic for a *FET* can be derived from the drain characteristics. A line is drawn vertically on the drain characteristics to represent a constant V_{DS} level. The corresponding I_D and V_{GS} values along this line are noted and then used to plot the transfer characteristic. The process is demonstrated in Example 9-2.

Example 9-2

Derive the transfer characteristic for $V_{DS} = 8$ V from the *FET* drain characteristics in Fig. 9-11.

Solution

On Fig. 9-11 draw a vertical line at $V_{DS} = 8$ V.
From the intersection of the line and the characteristics read the following quantities:

V_{GS} (V)	0	-1	-2	-3	-4
I_D (mA)	10	7	4.5	2.2	0.5

On Fig. 9-14, plot *point 1* at $V_{GS} = 0$ and $I_D = 10$ mA.
Plot *point 2* at $V_{GS} = -1$ V and $I_D = 7$ mA,
and so on through $V_{GS} = -4$ V and $I_D = 0.5$ mA.
Draw the transfer characteristic through the pints.

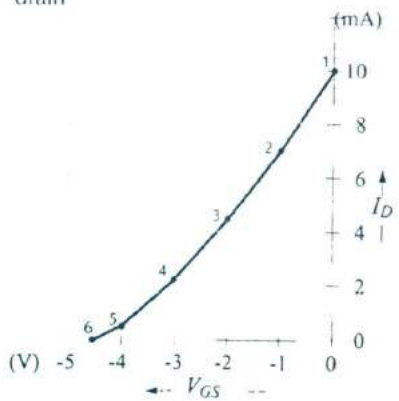


Figure 9-14
Transfer characteristics for Ex. 9-2.

p-channel JFET Characteristics

Figure 9-15 shows a circuit for obtaining the characteristics of a *p*-channel *JFET*. Note the direction of the arrowhead on the *FET* symbol, and the drain current direction. Also, note the supply voltage polarity, and the polarity of the gate-source bias voltage. The drain terminal is negative with respect to the source, and the gate terminal is positive with respect to the source. To obtain a table of quantities to plot a drain characteristic, V_{GS} is maintained constant at the desired (positive) level, $-V_{DS}$ is increased in steps from zero, and the I_D levels are noted at each step.

Typical *p*-channel *JFET* drain characteristics and transfer characteristics are shown in Fig. 9-16. It is seen that these are similar to the characteristics for an *n*-channel *JFET*, except for the voltage polarities. In Fig. 9-16, when $V_{GS} = 0$, $I_{DSS} = 15$ mA, and progressively more positive levels of V_{GS} reduce the level of I_D toward cutoff at $V_P = +6$ V. Using $V_{GS} = -0.5$ V produces a higher level of I_D than when $V_{GS} = 0$. As in the case of the *n*-channel *JFET*, forward bias at the gate-channel junctions should be avoided, consequently, negative V_{GS} levels are normally not used with a *p*-channel *JFET*.

The transfer characteristic for a *p*-channel device can be obtained experimentally, or can be derived from the drain characteristics, just as for an *n*-channel *FET*.

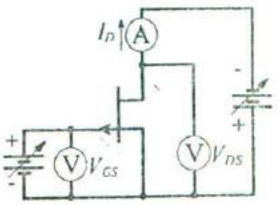


Figure 9-15
Circuit for determining the characteristics of a p-channel JFET.

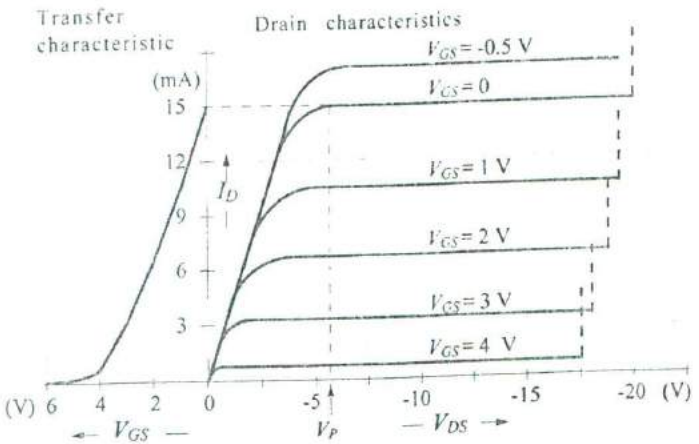


Figure 9-16
Transfer and drain characteristics for a p-channel JFET.

Practise Problems

9-2.1 The following table of I_D/V_{DS} values for a *FET* was obtained with $V_{GS} = 0$. Plot the drain characteristic and determine I_{DSS} and V_P.

V_{DS} (V)	0	1	2	2.5	3	4	6	8	10	12
I_D (mA)	0	2	4.5	5.3	5.5	5.5	5.5	5.5	5.5	5.5

9-3 JFET Data Sheet and Parameters

Maximum Ratings

Typical *FET* data sheets are shown in Appendix 1-11 and 1-12 and a portion of a *FET* data sheet is reproduced in Fig. 9-17. As with other device data sheets, a device type number and brief description is usually given at the start. Maximum ratings follow, and then the electrical characteristics are stated for specific bias conditions. From Fig. 9-17, the maximum drain-source voltage (V_{DS}) for the *2N5457* through *2N5459* devices is 25 V, and the maximum drain-gate voltage (V_{DG}) is also 25 V. This means, for example, that if a -5 V gate-source bias is used, the drain source voltage should not exceed,

$$V_{DS} = V_{DG(max)} - V_{GS} = 25\text{ V} - 5\text{ V}$$
$$= 20\text{ V}$$

2N5457, 2N5458, 2N5459 (Silicon)
N-Channel FET

Silicon N-channel junction field-effect transistors designed for general-purpose audio and switching applications.

(TO-92)

Drain and source may be interchanged

Maximum ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	25	V_{dc}
Drain-Gate voltage	V_{DG}	25	V_{dc}
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	V_{dc}
Gate Current	I_G	10	mA

Figure 9-17
Portion of data sheet for n-channel JFET.

Note on Fig. 9-17 that the maximum reverse gate-source voltage ($V_{G(r)}$) is specified as 25 V. This is considerably greater than the (typically 5 V) maximum base-emitter reverse voltage for a *BJT*.

No maximum drain current is specified in Fig. 9-17, but this can be calculated from the maximum power dissipation and the V_{DS} level. The specified gate current (I_G) is the maximum gate current if the gate-channel junctions become forward biased.

Saturation Current and Pinch-off Voltage

The *drain-source saturation current* (I_{DSS}) and the *pinch-off voltage* (V_P or $V_{GS(off)}$) have already been discussed in Section 9-1. Values for these are listed in the *JFET* data sheet portion showing the *Off Characteristics* and *ON Characteristics* in Fig. 9-18. It is seen that $V_{GS(off)}$ for a *2N5457* (underlined) ranges from a minimum of 0.5 V to a maximum of 6 V. Also, the I_{DSS} level for a *2N5457* (dashed underline) is a minimum of 1 mA and a maximum of 5 mA.

The *FET* transfer characteristic approximately follows the equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \qquad (9\text{-}1)$$

When I_{DSS} and V_P are known, a table of corresponding values of I_D and V_{GS} can be determined from Eq. 9-1. These may be used to construct the *FET* transfer characteristic. Because of the wide range of specified values for I_{DSS} and V_P, the transfer characteristic can differ substantially from one device to another one having the same type number. This creates a problem in *FET* bias circuits (see Chapter 10).

2N5457, 2N5458, 2N5459

Off Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Gate-Source Cutoff Voltage (V_{DS} = 15 V dc, I_D = 10 nA dc)	$V_{GS(off)}$				V dc
2N5457		0.5	—	6.0	
2N5458		1.0	—	7.0	
2N5459		2.0	—	8.0	

ON Characteristics

Zero gate voltage drain current (V_{DS} = 15 V dc, V_{GS} = 0)		I_{DSS}			mA dc
2N5457		1.0	3.0	5.0	
2N5458		2.0	6.0	9.0	
2N5459		4.0	9.0	16.0	

Figure 9-18
Pinch-off voltage and drain-source saturation current specifications for n-channel JFETs.

Example 9-3

Using the information provided on the data sheet (Fig. 9-18) construct the minimum and maximum transfer characteristics for a *2N5459 JFET.*

Solution

From Fig. 9-18; $V_P = V_{GS(off)} = 2$ V (min), 8 V (max)

and, $I_{DSS} = 4$ mA (min), 16 mA (max)

To construct the minimum transfer characteristic, substitute $V_{P(min)}$ *and* $I_{DSS(min)}$ *into Eq. 9-1, together with convenient levels of* V_{GS}.

Eq. 9-1, $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

For $V_{GS} = 0$, $I_D = 4\text{ mA}[1 - (0/2\text{ V})]^2 = 4$ mA

Plot point 1 for the minimum transfer characteristic on Fig. 9-19 at $V_{GS} = 0$ *and* $I_D = 4$ mA.

For V_{GS} = 0.5 V, I_D = 2.25 mA point 2
For V_{GS} = 1 V, I_D = 1 mA point 3
For V_{GS} = 1.5 V, I_D = 0.25 mA point 4
For V_{GS} = 2 V, I_D = 0 point 5

The minimum transfer characteristic is now drawn through points 1 through 5.

For the maximum transfer characteristic, the above process is repeated using V_P = 8 V and I_{DSS} = 16 mA.

For V_{GS} = 0, I_D = 16 mA[1 - (0/8 V)]^2 = 16 mA

Plot point 6 for the maximum transfer characteristic on Fig. 9-19 at V_{GS} = 0 and I_D = 16 mA.

For V_{GS} = 2 V, I_D = 9 mA point 7
For V_{GS} = 4 V, I_D = 4 mA point 8
For V_{GS} = 6 V, I_D = 1 mA point 9
For V_{GS} = 8 V, I_D = 0 point 10

Draw the maximum transfer characteristic through points 6 through 10.

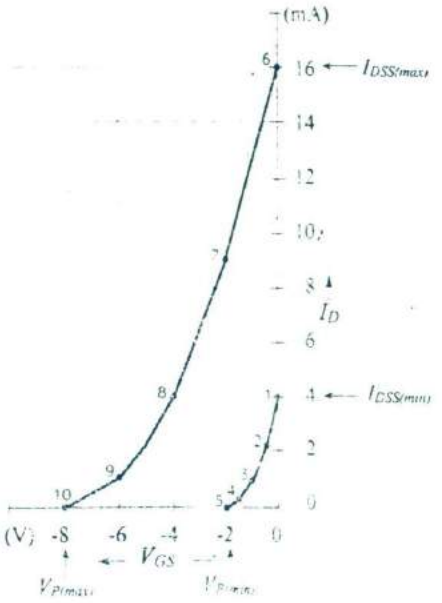


Figure 9-19
Maximum and minimum transfer characteristic for a 2N5459 JFET constructed for Ex. 9-3.

Forward Transfer Admittance

The *forward transfer admittance* (Y_{fs}) [also known as the *transconductance* (g_m or g_{FS})] for a *FET* defines how the drain current is controlled by the gate-source voltage.

$$Y_{fs} = \frac{\text{variation in } I_D}{\text{variation in } V_{GS}} \text{ (When } V_{DS} \text{ remains constant)}$$

$$Y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}\Bigg|_{V_{DS}} \qquad (9\text{-}2)$$

The units used for Y_{fs} are *microSiemens* (μS), which can be restated as *microamps per volt* ($\mu A/V$). *MilliSiemens* (*mS*), or *milliamps/volt* (*mA/V*) might also be used. For a *FET* with Y_{fs} = 2 mA/V, I_D changes by 2 mA when V_{GS} is altered by 1 V. In the portion of a *FET* data sheet in Fig. 9-20, the Y_{fs} units are μmhos. The *mho* (ohm written backwards) is another (older) name for the *Siemen*, the unit of conductance. For the *2N5457* (underlined) the value of Y_{fs} is specified as a minimum of 1000 µmhos, and a maximum of 5000 µmhos. An inverted ohm symbol is also sometimes used instead of the Siemens symbol.

Because Y_{fs} defines the relationship between I_D and V_{GS}, it can be determined from the slope of the *FET* transfer characteristic. This is demonstrated in Ex. 9-4, and illustrated in Fig. 9-21.

2N5457, 2N5458, 2N5459
Dynamic Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Forward Transfer Admittance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1 kHz)	Y_{fs}				μmhos
2N5457		1000	3000	5000	
2N5458		1500	4000	5500	
2N5459		2000	4500	6000	

Figure 9-20
JFET forward transfer admittance specification.

Example 9-4

Determine Y_{fs} at V_{GS} = -1 V and at V_{GS} = -4 V from the *2N5459 FET* transfer characteristic in Fig. 9-21.

Solution

At V_{GS} = -1 V,

Eq. 9-2,
$$Y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{4.3\text{ mA}}{1.25\text{ V}}$$
$$= 3.4\text{ mA/V} = 3400\,\mu\text{S}$$

At V_{GS} = -4 V,
$$Y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{3.8\text{ mA}}{2\text{ V}}$$
$$= 1.9\text{ mA/V} = 1900\,\mu\text{S}$$

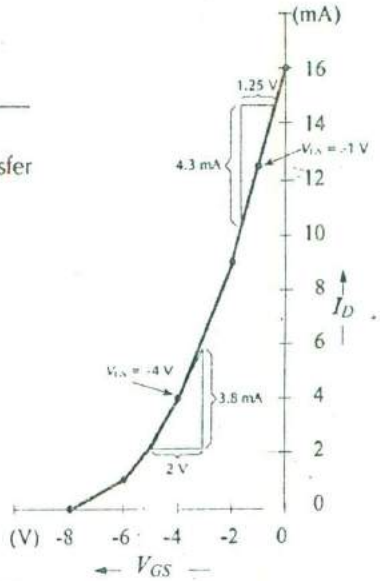


Figure 9-21
The value of the forward transfer admittance for a FET can be determined from the slope of the transfer characteristic.

The transfer characteristic for a *FET* is defined by Eq. 9-1, and Y_{fs} is determined from the slope of the transfer characteristic. So, an equation for Y_{fs} can be derived by differentiating Eq. 9-1.

$$Y_{fs} = \frac{2\,I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad (9\text{-}3)$$

Equation 9-3 may be used to calculate the value of Y_{fs} for any V_{GS} level. As in Eq. 9-1, the negative sign for V_{GS} is already included, so that only the numerical value should be entered.

Example 9-5

Using Eq. 9-3, determine Y_{fs} at V_{GS} = -1 V and at V_{GS} = -4 V for a *2N5458 JFET* with a maximum transfer characteristic, (see Fig. 9-19).

Solution

From the data sheet (Fig. 9-18), the 2N5458 maximum transfer characteristic is defined by;

$$V_{P(max)} = V_{GS(off)(max)} = 7\text{ V}$$

and,
$$I_{DSS(max)} = 9\text{ mA}$$

At V_{GS} = -1 V,

Eq. 9-3, $$Y_{fs} = \frac{2\,I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] = \frac{2 \times 9\text{ mA}}{7\text{ V}}\left[1 - \frac{1\text{ V}}{7\text{ V}}\right]$$

$$= 2200\,\mu S$$

At V_{GS} = -4 V,

Eq. 9-3, $$Y_{fs} = \frac{2\,I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] = \frac{2 \times 9\text{ mA}}{7\text{ V}}\left[1 - \frac{4\text{ V}}{7\text{ V}}\right]$$

$$= 1100\,\mu S$$

Output Admittance

The *drain resistance* (r_d) of a *FET* is the *ac* resistance between drain and source terminals when the device is operating in the pinch-off region of its drain characteristics. It is also the slope of the drain characteristics in the pinch-off region, (see Fig. 9-22). The drain characteristics are almost flat, so, r_d is not easily determined from the characteristic. Because r_d is usually the output resistance of the *FET* at the drain terminal, it may also be expressed as an *output admittance* ($Y_{os} = 1/r_d$).

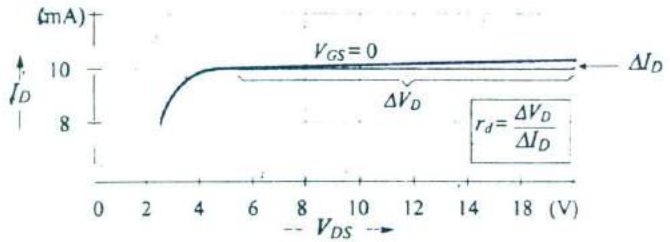


Figure 9-22
The ac drain resistance of a FET (r_d) is the slop of the drain characteristic. The output admittance (Y_{os}) is the inverse of r_d.

The output admittance is defined as,

$$Y_{os} = \frac{\text{variation in } I_D}{\text{variation in } V_{DS}} \text{ (When } V_{GS} \text{ remains constant)}$$

$$\mathbf{Y_{os} = \frac{\Delta I_D}{\Delta V_{DS}}\Bigg|_{V_{GS}}} \qquad \textbf{(9-4)}$$

From Appendix 1-11, Y_{os} for the *2N5457-5459 JFETs* is 10 μS typically, and 50 μS maximum. This corresponds to a drain resistance of 100 kΩ typically, and 20 kΩ minimum.

Drain-Source ON Resistance

The *drain-source ON resistance* ($r_{DS(on)}$) (also designated $R_{D(on)}$), is a *dc* quantity, not to be confused with the *ac* drain-source resistance (r_{ds}). $r_{DS(on)}$ is the resistance of the *FET* channel when

the depletion regions are absent: when the device is biased *ON* in the channel ohmic region of the drain characteristics. (see Fig. 9-23). In this condition, the voltage drop along the channel from drain to source is (I_D x $r_{DS(on)}$). This is the *drain-source ON voltage* ($V_{DS(on)}$), which is similar to the $V_{CE(sat)}$ of a *BJT*.

The drain-source *ON* resistance might typically be 60 Ω, or lower, (see Appendix 1-12). It can be an important quantity for *FETs* used in switching circuits. $V_{DS(on)}$ can be much smaller than $V_{CE(sat)}$, making *FET* gates superior to *BJT* gates for some applications.

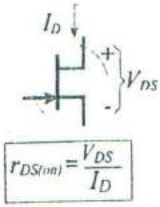
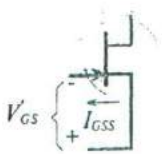


Figure 9-23
The drain-source ON resistance ($r_{DS(on)}$) of a FET is the channel resistance.

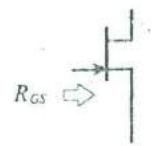
Gate Cutoff Current and Input Resistance

The gate-channel junctions in a *JFET* are *pn*-junctions, and because they are normally reverse biased, a minority charge carrier current flows. This is the *gate-source cutoff current* (I_{GSS}), or *gate reverse current*, [see Fig. 9-24(a)]. For a *2N5457 FET*, I_{GSS} is specified as 1 nA at 25°C, and 200 nA at 100°C. (see Appendix 1-11).

The *gate input resistance* (R_{GS}) is the resistance of the reverse-biased gate-channel junctions [Fig. 9-24(b)], and it is inversely proportional to I_{GSS}. Typical values of R_{GS} for a *JFET* are 10^9 Ω at 25°C and 10^7 Ω at 100°C.



(a) Gate reverse current



(b) Gate input resistance

Figure 9-24
Gate cutoff current and input resistance.

Breakdown Voltage

The are several ways used for expressing *JFET* breakdown voltage. BV_{DGO} is the *drain gate breakdown voltage* with the source terminal open-circuited. BV_{GSS} is the *gate-source breakdown voltage* with the drain terminal shorted to the source. Both are a specification of the voltage at which the gate-channel junctions might break down. Appendix 1-11 shows a BV_{GSS} of 25 V for a *2N5457*. (this is identified as $V_{(BR)GSS}$ on the data sheet).

Noise Figure

A *FET* usually has a much lower level of thermal noise than a *BJT*. This is because there are very few charge carriers crossing junctions in a *FET*. As in the case of a *BJT*, the *FET noise figure (NF)* is specified as a *spot noise figure* at a particular frequency and bias conditions, and for a given resistance at the input. The figure varies if any of these conditions are altered. Noise calculations for a *FET* circuit are performed exactly as for a *BJT* circuit.

Capacitances

Terminal capacitances for *FETs* may be specified as *gate-drain capacitance* (C_{gd}), *gate-source capacitance* (C_{gs}), and *drain-source capacitance* (C_{ds}). The input capacitance is sometimes expressed as the *common-source input capacitance* (C_{iss} or C_{gss}). This is the gate-source capacitance measured with the drain terminal shorted to the source, (Fig. 9-25). In this case, a *reverse transfer capacitance* (C_{rss}) is also specified: C_{rss} being another term for C_{gd}. These quantities are very important for *FET* high-frequency and switching circuits. From the *2N5457* specification in Appendix 1-11, the maximum capacitance values are C_{iss} = 7 pF, and C_{rss} = 3 pF.

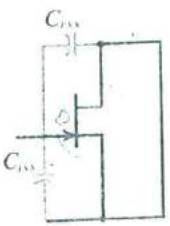


Figure 9-25
FET common-source input capacitances and reverse transfer capacitance.

Practise Problems

9-3.1 Construct the maximum transfer characteristic for a *2N5458 JFET* (see Appendix 1-11). From the transfer characteristic, determine the value of Y_{fs} at V_{GS} = -4 V.

9-3.2 Use Eq. 9-3 to calculate the value of Y_{fs} for a *2N5459 JFET* at V_{GS} = -1 V, and at V_{GS} = -4 V.

9-3.3 From the data sheet in Appendix 1-12, determine the following quantities for a *2N4860 FET:* maximum pinch-off voltage, maximum drain-source saturation current, drain-source *ON* resistance.

9-4 *FET Amplification*

Consider the *n*-channel *JFET* circuit in Fig. 9-26. Note that drain-source terminals are provided with a dc supply (V_{DD}), connected via the drain resistor (R_1). The gate-source junctions are reverse-biased by the gate voltage (V_G). An *ac* signal generator (with voltage v_i) is connected in series with the gate terminal. As already discussed, field effect transistors are voltage-operated devices. The drain current is controlled by the gate-source voltage. A change in gate-source voltage (ΔV_{GS}) produces a change in drain current (ΔI_D), and this causes a variation in the voltage drop across the resistor connected in series with the drain terminal.

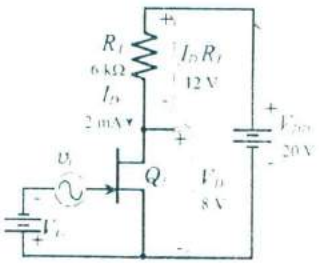


Figure 9-26
FET voltage amplifier circuit. An ac input (v_i) produces a variation in I_D which varies the voltage drop across resistor R_1. This results in an (amplified) ac output voltage.

Suppose that, for the circuit in Fig. 9-26, V_{DD} = 20 V, R_1 = 6 kΩ, and V_G is adjusted to give I_D = 2 mA. Also, assume that the *FET* has a forward transfer admittance of Y_{fs} = 4000 μS. The dc level of the drain voltage is,

$$V_D = V_{DD} - (I_D R_1) = 20 \text{ V} - (2 \text{ mA} \times 6 \text{ k}\Omega)$$
$$= 8 \text{ V}$$

Now assume that the instantaneous level of v_i is +50 mV. This produces an increase,

$$\Delta I_D = Y_{fs} \times v_i = 4000 \text{ μS} \times 50 \text{ mV}$$
$$= 0.2 \text{ mA}$$

The new level of drain voltage is,

$$V_D = V_{DD} - R_1 (I_D + \Delta I_D) = 20 \text{ V} - 6 \text{ k}\Omega(2 \text{ mA} + 0.2 \text{ mA})$$
$$= 6.8 \text{ V}$$

So, V_D changed from 8 V to 6.8 V when the ac input increased from zero to 50 mV.

or, $$\Delta V_D = 6.8 \text{ V} - 8 \text{ V}$$
$$= -1.2 \text{ V}$$

When the instantaneous level of v_i is -50 mV,

$$\Delta I_D = Y_{fs} \times v_i = 4000\ \mu S \times (-50\ mV)$$
$$= -0.2\ mA$$

This gives a new drain voltage,

$$V_D = V_{DD} - R_1 (I_D + \Delta I_D) = 20\ V - 6\ k\Omega(2\ mA - 0.2\ mA)$$
$$= 9.2\ V$$

So,
$$\Delta V_D = 9.2\ V - 8\ V$$
$$= 1.2\ V$$

It is seen that an ac input of $v_i = \pm 50$ mV produces an output voltage change at the *FET* drain terminal of $\Delta V_D = \pm 1.2$ V. This can be stated as an ac output voltage of $v_o = \pm 1.2$ V. The circuit voltage amplification is,

$$A_v = \frac{v_o}{v_i} = \frac{1.2\ V}{50\ mV}$$
$$= 24$$

Example 9-6

A *2N5457 JFET* is used in the amplifier circuit in Fig. 9-27. Calculate the maximum and minimum output voltage produced by a ±100 mV ac input. Also, calculate the circuit voltage gain in each case.

Solution

From Appendix 1-11,

$$Y_{fs(max)} = 5000\ \mu S \text{ and } Y_{fs(min)} = 1000\ \mu S$$

For $Y_{fs(max)}$,
$$\Delta I_D = Y_{fs(max)} \times v_i = 5000\ \mu S \times (\pm 100\ mV)$$
$$= \pm 0.5\ mA$$

and,
$$v_o = \Delta I_D \times R_l = \pm 0.5\ mA \times 5.6\ k\Omega$$
$$= \pm 2.8\ V$$

$$A_v = \frac{v_o}{v_i} = \frac{\pm 2.8\ V}{\pm 100\ mV}$$
$$= 28$$

For $Y_{fs(min)}$,
$$\Delta I_D = Y_{fs(max)} \times v_i = 1000\ \mu S \times (\pm 100\ mV)$$
$$= \pm 0.1\ mA$$

and,
$$v_o = \Delta I_D \times R_l = \pm 0.1\ mA \times 5.6\ k\Omega$$
$$= \pm 0.56\ V$$

$$A_v = \frac{v_o}{v_i} = \frac{\pm 0.56\ V}{\pm 100\ mV}$$
$$= 5.6$$

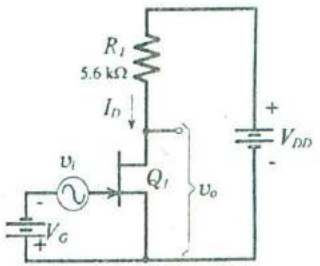


Figure 9-27
FET amplifier circuit for Ex. 9-6.

Practise Problems

9-4.1 A *FET* amplifier circuit, as in Fig. 9-27, has $V_{DD} = 15$ V, $R_1 = 4.7$ kΩ, and $v_i = \pm 30$ mV. If V_G is adjusted to give $I_D = 1.5$ mA, calculate V_D. Also, calculate the typical voltage gain for the circuit if Q_1 is a *2N5459* with $Y_{fs} = 4500\ \mu$S.

9-5 MOSFETs

Enhancement MOSFET

Figure 9-28 shows the construction of a *metal oxide semiconductor FET (MOSFET)*, also known as an *insulated gate FET*. Starting with a high-resistive *p*-type substrate, two blocks of heavily-doped *n*-type material are diffused into the substrate, and then the surface is coated with a layer of silicon dioxide. Holes are cut through the silicon dioxide to make contact with the *n*-type blocks. Metal is deposited through the holes for source and drain terminals, as illustrated, and a metal plate is deposited on the surface area between drain and source. As will be explained, this plate functions as a gate.

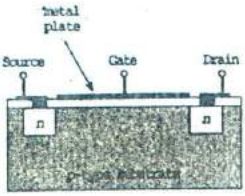
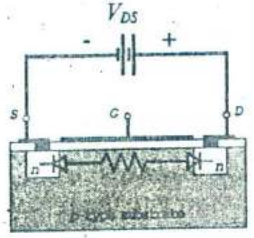


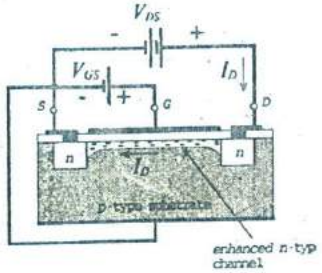
Figure 9-28
Metal oxide semiconductor FET (MOSFET) construction.

Consider the situation illustrated in Fig. 9-29(a). The drain terminal of the *MOSFET* is positive with respect to the source, and the gate is open-circuited. The two *n*-type blocks and the *p*-type substrate form back-to-back *pn*-junctions connected by the resistance of the *p*-type material, as illustrated. The *pn*-junction close to the drain terminal is reverse biased, so only a very small (reverse leakage) current flows from *D* to *S*.



(a) V_{DS} applied and gate open-circuited

Now assume that the source terminal is connected to the substrate, and that a positive gate voltage is applied, as shown in Fig. 9-29(b). Negative (minority) charge carriers within the substrate are attracted to the (positive) plate that constitutes the gate. These charge carriers (electrons) cannot cross the silicon dioxide to the gate, so they accumulate close to the surface of the substrate, as shown. The minority charge carriers constitute an *n*-type channel between drain and source, and as the gate-source voltage is made more positive, more electrons are attracted into the channel causing the channel resistance to decrease. A drain current flows along the channel between the *D* and *S* terminals, and because the channel resistance is controlled by the gate-source voltage (V_{GS}), the drain current is also controlled by the level of V_{GS}. The channel conductivity is said to be *enhanced* by the positive gate-source voltage, so the device is known as an *enhancement-mode MOSFET*, (*E-MOSFET*).



(b) Effect of positive V_{GS}

Figure 9-29
Effect of $+V_{DS}$ on the MOSFET with the gate terminal open-circuited, and with $+V_{GS}$ applied to the gate.

Typical drain and transfer characteristics for an enhancement mode *n*-channel *MOSFET* are shown in Fig. 9-30. Note on both characteristics that the drain current increases as the positive gate-source bias voltage is increased. Because the gate of the *MOSFET* is insulated from the channel, there is no gate-source leakage current, and the device has an extremely high (gate) input resistance; typically $10^{15}\ \Omega$, or greater. Forward transfer admittance

values for this type of (low-power) *MOSFET* typically range from 1 mS (1 mA/V) to a maximum of perhaps 6 mS, which is similar to *JFET* Y_{fs} values.

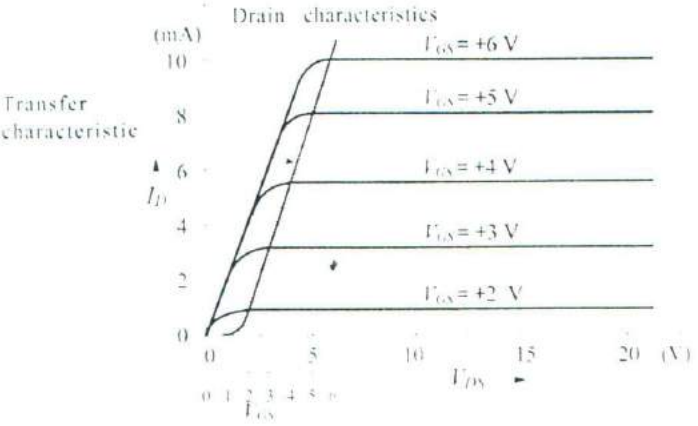


Figure 9-30
Typical drain and transfer characteristics for an n-channel enhancement-mode MOSFET.

Two graphic symbols for the *n*-channel *E-MOSFET* are shown in Fig. 9-31. One symbol shows the source and substrate connected internally, while the other has a separate substrate terminal. The line representing the device channel is broken into three sections, to indicate that the channel does not exist until an appropriate gate voltage is applied. The fact that the device has an insulated gate is illustrated on the symbols by the gate not making direct contact with the channel. The arrowhead points from the *p*-type substrate to the *n*-type channel.

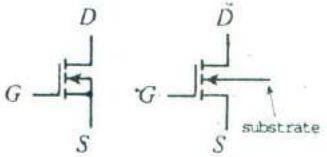
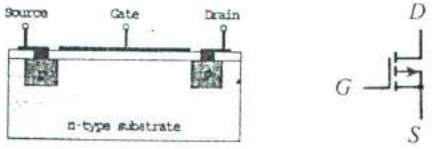


Figure 9-31
Circuit symbols for an n-channel enhancement-mode MOSFET.

A *p*-channel *E-MOSFET* is constructed by starting with an *n*-type substrate and diffusing *p*-type drain and source blocks, as illustrated in Fig. 9-32(a). The device characteristics are similar to those in Fig. 9-30, except that all voltage polarities and current directions are reversed. The drain-source voltage is negative, and a negative gate-source voltage is required to create the *p*-type channel. The arrowhead in the circuit symbols are also reversed, [see Fig. 9-32(b)].



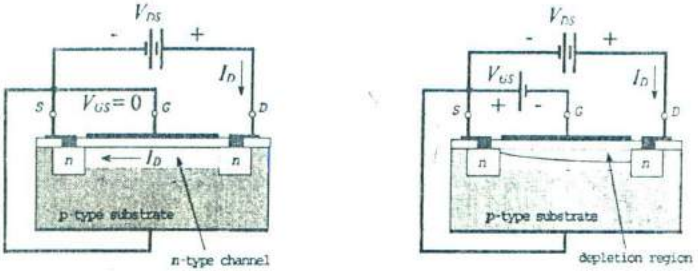
(a) *p*-channel enhancement *MOSFET* (b) Circuit symbol

Figure 9-32
Construction and circuit symbols for a p-channel enhancement-mode MOSFET.

Depletion-Enhancement MOSFET

The device cross-section shown in Fig. 9-33(a) is similar to that for an enhancement-mode *MOSFET*, except that a lightly-doped *n*-type channel is included between the drain and source blocks. When a

positive drain-source voltage (V_{DS}) is applied, a drain current (I_D) flows even when the gate-source voltage (V_{GS}) is zero. If a negative V_{GS} is applied, as shown in Fig. 9-33(b), some of the negative charge carriers are repelled from the gate and driven out of the *n*-type channel. This creates a depletion region in the channel, as illustrated, causing an increase in channel resistance and a decrease in drain current. The effect is similar to that in an *n*-channel *JFET*. Because of the channel depletion regions, the device can be termed a *depletion-mode MOSFET*.



(a) I_D flows even when $V_{GS} = 0$

(b) I_D decreases when V_{GS} is negative, and increases when V_{GS} is positive

Figure 9-33
n-channel depletion-enhancement MOSFET.

Now consider what occurs when a positive gate-source voltage is applied. Additional *n*-type charge carriers are attracted from the substrate into the channel, decreasing its resistance and increasing the drain current. So, the depletion-mode *MOSFET* can also be operated as an enhancement-mode device. Thus, these devices are referred to as *depletion-enhancement MOS*, or *DE-MOS*.

Typical drain and transfer characteristics for a *DE-MOSFET* are shown in Fig. 9-34. The device operates in the depletion-mode when V_{GS} is negative, and in the enhancement-mode when positive levels of V_{GS} are used.

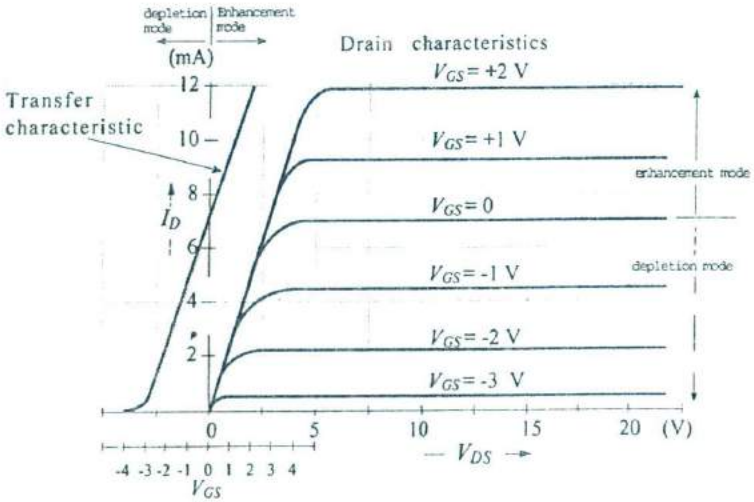


Figure 9-34
Drain and transfer characteristics for an n-channel depletion-enhancement MOSFET.

The circuit symbols used for *DE-MOSFETs* are similar to those already discussed for *E-MOSFETs*, except that the line representing the channel is made solid to show that a channel is present when $V_{GS} = 0$. (see Fig. 9-35).

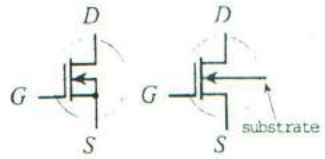


Figure 9-35
Circuit symbols for an n-channel depletion-enhancement MOSFET.

Example 9-7

From the *DE-MOSFET* characteristics in Fig. 9-34, determine the forward transfer admittance at $V_{GS} = 0$.

Solution

At $V_{GS} = -2$ V, $I_D = 2.2$ mA
and at $V_{GS} = +2$ V, $I_D = 11.8$ mA

$$\Delta I_D = 11.8 \text{ mA} - 2.2 \text{ mA} = 9.6 \text{ mA}$$

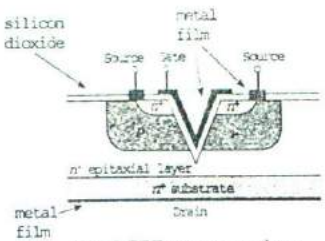
and, $\Delta V_{GS} = +2 \text{ V} - (-2 \text{ V}) = 4 \text{ V}$

Eq. 9-2, $$Y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{9.6 \text{ mA}}{4 \text{ V}}$$

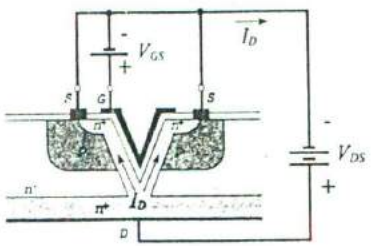
$$= 2.4 \text{ mA/V} = 2400 \, \mu\text{S}$$

VMOS

A disadvantage of the *MOSFET* types already discussed is that the minimum channel length depends upon the dimensions of the photographic masks used in the manufacturing process. Shorter channel lengths can be produced by changing the geometry of the *MOSFET* to create a vertical channel (instead of horizontal). The channel length is then easily determined by the diffusion process. The shorter channel results in lower resistance, greater power dissipation, higher frequency response, and larger forward transfer admittance values than are possible with other *MOSFETs*.



(a) *V-FET* construction



(b) Enhanced channel connects the drain and source

Figure 9-36
VMOSFET construction and operation. The vertical channel gives an improved frequency response, lower channel resistance, and greater power dissipation than other FETs.

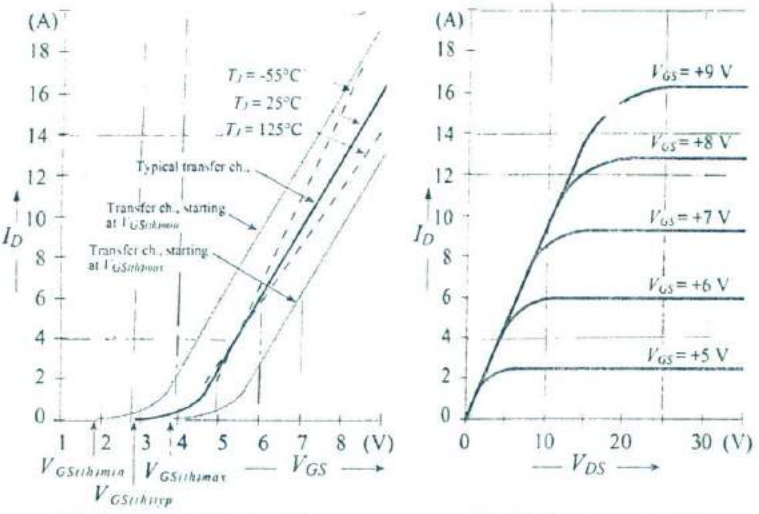
Figure 9-36(a) shows a device referred to as a *VMOSFET* because of its *V*-shaped configuration, and because it uses a vertical channel between drain and source. The *V*-cut penetrates from the surface of the device through n^+, p, and n^- layers almost to the n^+ substrate. The n^+ layers are low-resistive, and the n^- is a high-resistive region. The silicon dioxide layer covers

horizontal surface and the *V*-cut surface. The gate is a metal film deposited on the silicon dioxide surface in the *V*-cut. The drain terminal is at the bottom of the n^+ substrate, and the source connection is made to the top n^+ region and to the *p* region.

The *VFET* operates in the enhancement-mode; no channel exists until a positive gate source voltage is applied. An *n*-type channel is created as shown in Fig. 9-36(b) when V_{GS} is made positive, and a current flows vertically from drain to source.

Some versions of *VMOS* use a vertical channel, but do not use the *V*-cut. *MOTOROLA* currently manufactures devices referred to as *TMOS*®, because the drain current flow tends to be *T*-shaped. *INTERNATIONAL RECTIFIER* use the term *HEXFET*®, because of the hexagonal configuration employed in the device construction.

Typical *VFET* drain and transfer characteristics are shown in Fig. 9-37. It is seen that they are similar to the enhancement-mode device characteristics in Fig. 9-30, although much higher drain current levels are usually involved with a *VFET* than with other *MOSFETs*. The characteristics shown are for a device capable of dissipating 40 W.



(a) Transfer characteristics (b) Drain characteristics

Figure 9-37
Typical transfer and drain characteristics for a VMOSFET.

The *VFET* transfer characteristic is seen to be approximately linear over most of its length, and it is curved (non-linear) only at the low current levels. For the typical characteristic shown, I_D commences at the typical gate threshold voltage ($V_{GSthtyp}$), and the slope of the linear portion of the graph is set by the typical g_{FS} value (same as Y_{FS}). It should be noted that for a device with a given type number, I_D might commence at $V_{GSthjmin}$ or $V_{GSthjmax}$, and that the slope of the characteristic depends upon the actual g_{FS} for the device. Temperature changes can also have a serious effect on the characteristics, as shown by the dashed lines.

The graphic symbols used for *VMOS* devices are the same as for other enhancement-mode *MOSFETs*. However, a *parasitic pn*-junction is present between the p and n layers in a *VFET*, and this must not be allowed to become forward biased. So, the diode is usually shown on the device symbol. (see Fig. 9-38).

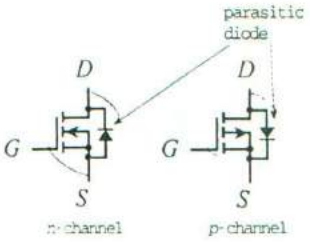


Figure 9-38
Circuit symbols for VMOSFETs.

VMOS devices can be described as high-voltage, *E-MOSFETs*. They are very suitable for high-frequency or fast switching applications. Normally, they have much larger forward transfer admittance (g_{fs}) values and lower drain-source *ON* resistances than other *FETs*. Figure 9-39 lists some performance data for two representative (low-power and high-power) *VMOSFETs*. Note that the 80 mS minimum g_{fs} for the *2N7002* is substantially larger than the 4 mS typical for other *FET* types. The *IRF520* has a typical g_{fs} of 2.9 S, which is greater again than that for the *2N7002*. *FET* voltage amplification is directly proportional to the forward transfer admittance, so *VMOS* circuits can have much greater voltage gains than circuits using other *FETs*.

MOSFET specifications normally list *gate threshold voltage* ($V_{GS(th)}$) values. The drain current remains at zero with gate-source voltage levels below $V_{GS(th)}$, and commences to flow when V_{GS} is increased above $V_{GS(th)}$. So, $V_{GS(th)}$ is similar to the pinch-off voltage for a *JFET*. Like the *JFET* pinch-off voltage, $V_{GS(th)}$ has maximum and minimum values for each device type number.

For a *JFET*, I_{DSS} is the drain current at $V_{GS} = 0$. The *E-MOSFET* parameter identified as I_{DSS} is still the drain current at zero gate-source voltage. However, because the device is *off* at $V_{GS} = 0$, I_{DSS} is a drain-source leakage current with a level measured in microamps. For *E-MOSFET* devices, I_D is usually specified as $I_{D(on)}$ at $V_{GS} = 10$ V.

2N7002

$V_{DS(max)}$	$I_{D(max)}$	$P_{D(max)}$	$r_{d(on)}$	g_{FS}	$V_{GS(th)}$
60 V	115 mA	200 mW	7.5 Ω	80 mS (min)	1 V (min) 2.5 V (max)

IRF520

$V_{DS(max)}$	$I_{D(max)}$	$P_{D(max)}$	$r_{d(on)}$	g_{FS}	$V_{GS(th)}$
100 V	8 A	40 W	0.3 Ω	1.5 S (min) 2.9 S (typ)	2 V (min) 4 V (max)

Figure 9-39
Performance data for low-power and high-power VMOSFETs.

E-MOSFETs are often applied in situations where they are biased *on* to a low drain current level, and then I_D is increased to a desired higher level by the application of a signal voltage. The precise levels of the required gate-source bias and signal voltages can only be determined from the transfer characteristic for each individual device. However, for a given I_D level beyond the curved portion of the characteristic, a rough approximation for the required V_{GS} can be calculated from the maximum $V_{GS(th)}$ and the typical g_{fs} values.

$$V_{GS} \approx V_{GS(th)max} + \frac{I_D}{g_{FS(typ)}} \qquad (9\text{-}5)$$

Example 9-8

Using the information in Fig. 9-39, calculculate the approximate gate-source voltage required to produce a 7 A drain current in an *IRF520*. Also, determine the drain-source *ON* voltage and the device power dissipation at I_D = 7 A.

Solution

Eq. 9-5, $$V_{GS} \approx V_{GS(th)(max)} + \frac{I_D}{g_{FS(typ)}} = 4\text{ V} + \frac{7\text{ A}}{2.9\text{ S}}$$

$$= 6.4\text{ V}$$

$$V_{DS(on)} = I_D \times r_{D(on)} = 7\text{ A} \times 0.3\ \Omega$$

$$= 2.1\text{ V}$$

$$P_D = I_D \times V_{DS(on)} = 7\text{ A} \times 2.1\text{ V}$$

$$= 14.7\text{ W}$$

Handling MOSFETs

Figure 9-40 shows the kind of label normally found on packages containing *MOSFETs*. This indicates that the devices can be very easily destroyed by *electrostatic discharge (ESD)*; that is, discharge of static electricity that accumulates on individuals or objects. Usually, the very thin layer of silicon dioxide at the gate breaks down when an excessive gate-source voltage is applied. Special precautions are necessary to protect *MOSFETs* from *ESD*:

1. Always store *MOSFETs* in closed conductive containers. Usually, they are packaged with the terminals inserted into conducting foam rubber.
2. Use a work station with a grounded anti-static bench-top pad and a grounded anti-static floor pad.
3. Wear anti-static clothing and grounded wrist bands.
4. Use a soldering iron with a grounded tip.
5. Avoid touching the device terminals.

Some *MOSFETs* have built-in protection against static electricity. Back-to-back series-connected Zener diodes are located between the gate and source terminals, as illustrated in Fig. 9-41. When the gate-source voltage is high enough to reverse bias one of the diodes into breakdown, the other diode is forward biased. Thus, the gate-source voltage cannot exceed $\pm(V_Z + V_F)$.



Figure 9-40
Packaging symbol used for indicating that the enclosed devices can be destroyed by static electricity.

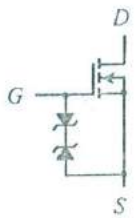


Figure 9-41
MOSFET with built-in Zener diodes for protection against static electricity.

Section 9-5 Review

9-5.1 Using illustrations, explain the operation of *n-channel E-MOS*.

9-5.2 Sketch circuit symbols for *n*-channel and *p*-channel *E-MOS* and *DE-MOS* field effect transistors.

9-5.3 Sketch typical transfer characteristics for *DE-MOS* devices.

9-5.4 Briefly explain the operation of *VMOS*.

Practise Problems

9-5.1 Determine the forward transfer admittance at I_D = 8 mA for the *E-MOS* device with the characteristics in Fig. 9-30.

9-5.2 Calculate the approximate gate-source voltage required to produce a 7.5 A drain current in an *E-MOSFET* that has maximum $V_{GS(th)}$ = 2.5 V and typical g_{fs} = 1.5 S.

Chapter-9 Review Questions

Section 9-1

9-1 Sketch a block representation for an *n*-channel *JFET*, showing bias voltages, depletion regions, and current directions. Identify the device terminals and explain its operation. Also explain the effect of increasing levels of negative gate-source voltage.

9-2 Repeat question 9-1 for a *p*-channel *JFET*, explaining the effect of increasing levels of positive gate-source voltage.

9-3 Sketch circuit symbols for *n*-channel and *p*-channel *JFETs*. Identify the terminals in each case, show supply and bias voltage polarities, and indicate the drain current directions.

9-4 Sketch the cross-section of a diffused *JFET*. Identify all parts of the device and briefly explain.

Section 9-2

9-5 Draw a circuit diagram for obtaining the drain and transfer characteristics for an *n*-channel *JFET*. Briefly explain how a table of values should be determined for each characteristic.

9-6 Sketch a typical drain characteristic for V_{GS} = 0 for an *n*-channel *JFET*. Explain the shape of the characteristic, identify the regions, and indicate the important current and voltage levels.

9-7 Draw a typical drain characteristics family for an *n*-channel *JFET*. Identify the V_{GS} for each characteristic. Briefly explain.

9-8 Draw a typical transfer characteristic for an *n*-channel *JFET*. Identify the drain-source saturation current and pinch-off voltage.

9-9 Sketch typical drain and transfer characteristics for a *p*-channel *JFET*. Show typical current and voltage scales and gate-source voltage levels.

Section 9-3

9-10 Define the saturation current and pinch-off voltage for a *JFET*, and state typical values for each quantity.

9-11 Define forward transfer admittance, transconductance, output admittance, and drain resistance for a *JFET*. State typical values for each quantity.

9-12 Define drain-source *ON* resistance, drain-source *ON* voltage and gate cutoff current for a *JFET*. State typical values.

Section 9-4

9-13 Sketch a basic voltage amplifier circuit using a *JFET*, and explain its operation.

Section 9-5

9-14 Draw a cross-section diagram for an enhancement-mode *MOSFET*. Identify all parts of the device and explain its operation.

9-15 Sketch typical drain and transfer characteristics for an *n*-channel *E-MOSFET*. Show typical current and voltage scales and gate-source voltage levels.

9-16 Sketch graphic symbols for *n*-channel and *p*-channel *E-MOSFETs*. Identify the terminals in each case, show the supply and bias voltage polarities, and indicate the drain and source current directions.

9-17 Draw a diagram of the cross-section of a depletion-enhancement-mode *MOSFET*. Identify all parts of the device and explain its operation.

9-18 Sketch typical drain and transfer characteristics for an *n*-channel *DE-MOSFET*. Show typical current and voltage scales and gate-source voltage levels.

9-19 Sketch graphic symbols for *n*-channel and *p*-channel *DE-MOSFETs*. Identify the terminals in each case, show the supply and bias voltage polarities, and indicate the drain and source current directions.

9-20 Draw a diagram of the cross-section of a *V-MOSFET*. Identify all parts of the device, explain its operation, and discuss its advantages compared to other *MOSFETs*.

9-21 Sketch typical drain and transfer characteristics for an *n*-channel *V-MOSFET*. Briefly explain the characteristics.

9-22 Sketch graphic symbols for *n*-channel and *p*-channel *V-MOSFETs*. Identify the terminals in each case, show the supply and bias voltage polarities, and indicate the drain and source current directions.

Chapter 9 Problems

Section 9-2

9-1 Plot the I_D/V_{DS} characteristic for an *n*-channel *JFET* from the following table of current and voltage levels. Determine I_{DSS} and V_P from the characteristics.

$V_{GS} = 0$	V_{DS} (V)	0	1.25	2	2.5	5	10	15	25
	I_D (mA)	0	2	3	4	4.8	4.9	4.95	5

$V_{GS} = -1$ V	V_{DS} (V)	0	1	2	2.5	5	10	15	25
	I_D (mA)	0	1	2	2.3	2.4	2.5	2.6	2.7

$V_{GS} = -2$ V	V_{DS} (V)	0	1	1.5	5	10	15	25
	I_D (mA)	0	0.5	0.8	0.9	0.95	0.99	1

9-2 Derive the device transfer characteristic from the drain characteristics plotted for Problem 9-1.

9-3 Plot the I_D/V_{DS} characteristic for a *p*-channel *JFET* from the following table of current and voltage levels. Determine I_{DSS} and V_P from the characteristics.

$V_{GS} = 0$	$-V_{DS}$ (V)	0	1	2.2	3	5	7	9.5	15	25
	I_D (mA)	0	2	4	6	8	8.6	9	9.2	9.3

$V_{GS} = +1$ V	$-V_{DS}$ (V)	0	1	2.5	3	5	6	10	25
	I_D (mA)	0	2	4	5	5.8	6	6.2	6.3

$V_{GS} = +2$ V	$-V_{DS}$ (V)	0	1.2	2.4	3	5	6	10	25
	I_D (mA)	0	2	3	3.5	3.9	4	4.2	4.3

9-4 Derive the device transfer characteristic from the drain characteristics plotted for Problem 9-3.

Section 9-3

9-5 Determine the value of Y_{fs} at V_{GS} = -2 V from the transfer characteristics constructed for Problem 9-2.

9-6 Determine the value of Y_{fs} at V_{GS} = 1 V from the transfer characteristics constructed for Problem 9-4.

9-7 From the data sheet information in Appendix 1-12, determine the following quantities for a *2N4857 JFET*: maximum drain-source voltage, maximum power dissipation, maximum pinch-off voltage, maximum drain-source saturation current, drain-source *ON* resistance.

9-8 Using the data sheet information in Appendix 1-11, construct the maximum transfer characteristics for a *2N5457 JFET*.

9-9 Determine the value of Y_{fs} at V_{GS} = -4 V and at V_{GS} = -2 V from the transfer characteristic constructed for Problem 9-8.

9-10 Using the data sheet information in Appendix 1-12, construct the maximum transfer characteristics for a *2N4858 JFET*.

9-11 Determine the value of Y_{fs} at V_{GS} = -2 V and at V_{GS} = -1 V from the characteristic constructed for Problem 9-10.

9-12 Using the maximum values of I_{DSS} and $V_{GS(off)}$ for a *2N5457 JFET*, calculate Y_{fs} at V_{GS} = -4 V, and at V_{GS} = -2 V.

9-13 Using the maximum values of I_{DSS} and $V_{GS(off)}$ for a *2N4858 JFET*, calculate Y_{fs} at V_{GS} = -2 V, and at V_{GS} = -1 V.

9-14 Calculate Y_{os} and r_d from the following measurements made on a *JFET*: [I_D = 9 mA when V_{GS} = 0 and V_{DS} = 5 V], [I_D = 9.25 mA when V_{GS} = 0 and V_{DS} = 15 V].

9-15 Referring to the specification in Appendix 1-11, determine the following quantities for a *2N5457 JFET*: maximum drain-source voltage, maximum power dissipation, maximum pinch-off voltage, maximum drain-source saturation current.

Section 9-4

9-16 The circuit in Fig. 9-42 uses a *2N5459 JFET* with the maximum transfer characteristics shown in Fig. 9-19. Calculate V_{DS} when V_{GS} = -1 V and when V_{GS} = -2 V. Also, calculate the circuit voltage gain.

9-17 The *2N5459* in the circuit in Fig. 9-42 is replaced with a *2N5457*. Calculate the maximum and minimum variations in V_{DS} produced by a ±0.1 V change at the gate. Also, calculate the circuit voltage gain.

9-18 Determine a suitable *JFET* forward transfer admittance for the amplifier circuit in Fig. 9-42 to have a minimum voltage gain of 15, when R_1 is changed to 2.2 kΩ.

9-19 A *JFET* amplifier circuit, as in Fig. 9-42, is to have a minimum voltage gain of 5. If the *FET* used is a *2N5458*, determine a suitable resistance for R_1.

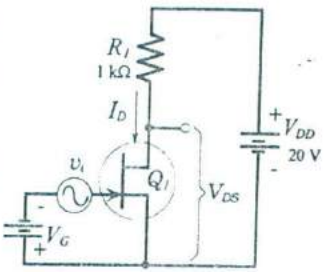


Figure 9-42

Section 9-5

9-20 Plot the transfer characteristics for a *DE-MOSFET* from the following table of measured current and voltage levels. From the characteristics, determine the value of Y_{fs} at V_{GS} = 0.

V_{GS} (V)	-3	-2	-1	0	+1	+2	+3
I_D (mA)	0.5	2.7	4.8	7	9	11.3	13.4

9-21 A *VMOSFET* has $r_{d(on)}$ = 0.5 Ω, g_{FS} = 2.5 S, and $V_{GS(th)}$ = 2 V. Calculate the approximate level of V_{GS} required to produce a 5 A drain current. Also, calculate $V_{DS(on)}$ and the device power dissipation when I_D = 5 A.

9-22 From the *2N7002* data sheet information in Fig. 9-39, determine $V_{DS(on)}$ and the power dissipation when I_D = 50 mA.

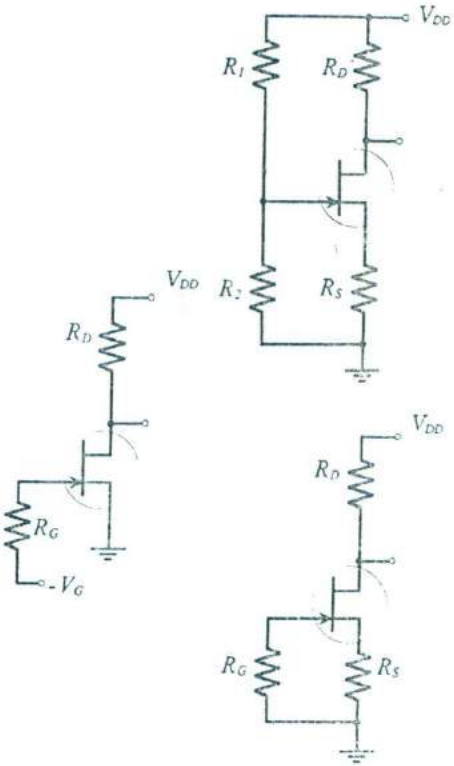
9-23 Calculate the approximate gate-source voltage, drain-source *ON* voltage, and power dissipation in a *IRF520* with a 5 A drain current. Refer to the partial specification in Fig. 9-39.

Practise Problem Answers

9-2.1 5.5 mA, 3 V
9-3.1 1127 μS
9-3.2 3160 μS, 1975 μS
9-3.3 -6 V, 100 mA, 40 Ω
9-4.1 7.95 V, 21.15
9-5.1 5 mS
9-5.2 7.5 V

Chapter 10

FET Biasing



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Objectives

You will be able to:

1. *Draw dc load lines for FET circuits, identify circuit Q-points, and estimate the maximum circuit output voltage variations.*
2. *Sketch gate bias, self bias, and voltage divider bias circuits, and explain the operation of each circuit.*
3. *Analyze various types of FET bias circuits using the device maximum and minimum transfer characteristics to determine circuit voltage and current levels.*
4. *Trouble-shoot non-operational FET bias circuits.*
5. *Design gate bias, self bias, and voltage divider bias circuits, and select appropriate standard value components.*
6. *Sketch constant current and other unusual bias circuit types, and explain the operation of each circuit.*
7. *Analyze and design each of the bias circuit types referred to in item 6.*
8. *Construct a universal transfer characteristic, and use it in analysis and design of FET bias circuits.*
9. *Sketch various bias circuits for MOSFET devices and explain the operation of each circuit.*
10. *Analyze and design MOSFET bias circuits.*
11. *Analyze and design bias circuits used with FET switches.*

Introduction

Like bipolar transistor circuits, field effect transistors used in amplifier (or other) circuits must be biased into an *on* state with constant current and terminal voltage levels. The widely differing maximum and minimum transfer characteristics for a FET can result in a wide range of drain current levels. This is similar to the situation caused by $h_{FE(max)}$ and $h_{FE(min)}$ in a *BJT* bias circuit. For reasonable upper and lower drain current limits in a *FET* circuit, source resistors and voltage divider networks must be employed. A graphical approach is most convenient for analysis or design of *FET* bias circuits.

10-1 DC Load Line and Bias Point

DC Load Line

The *dc load line* for a *FET* circuit is drawn on the device output characteristics (or drain characteristics) in exactly the same way as for a *BJT* circuit, (see Section 5-1). Refer to the *n*-channel *FET* circuit in Fig. 10-1. The source terminal is grounded, the gate is biased via resistor R_G to a negative voltage ($-V_G$), and the drain terminal is supplied from $+V_{DD}$ via resistor R_D. The *dc* load line for this circuit is a graph of drain current (I_D) versus drain-source voltage (V_{DS}), for a given value of drain resistance and a given supply voltage.

From Fig. 10-1, the drain-source voltage is,

V_{DS} = (supply voltage) - (voltage drop across R_D)

or,
$$\mathbf{V_{DS} = V_{DD} - I_D R_D} \qquad \textbf{(10-1)}$$

Substituting V_{DD}, R_D, and convenient levels of I_D into Eq. 10-1, produces corresponding V_{DS} and I_D values. These values are then plotted on the device characteristics, and the *dc* load line is drawn through them.

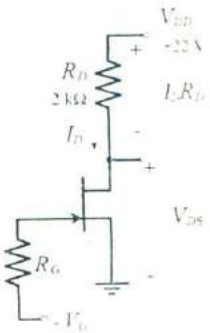


Figure 10-1
FET circuit with dc load resistor (R_D), supply voltage ($+V_{DD}$), and gate bias ($-V_G$).

Example 10-1

Draw the *dc* load line for the circuit in Fig. 10-1 on the *FET* characteristics in Fig. 10-2.

Solution

when $I_D = 0$,
Eq. 10-1, $V_{DS} = V_{DD} - I_D R_D = 22\text{ V} - 0$
$= 22\text{ V}$

Plot *point A* on Fig. 10-2 at,
$I_D = 0$ and $V_{DS} = 22\text{ V}$

when $V_{DS} = 0$,
from Eq. 10-1, $0 = V_{DD} - I_D R_D$

giving,
$$I_D = \frac{V_{DD}}{R_D} = \frac{22\text{ V}}{2\text{ k}\Omega}$$
$$= 11\text{ mA}$$

Plot *point B* on Fig. 10-2 at,

$$I_D = 11\text{ mA and } V_{DS} = 0\text{ V}$$

Draw the *dc* load line through *points A* and *B*.

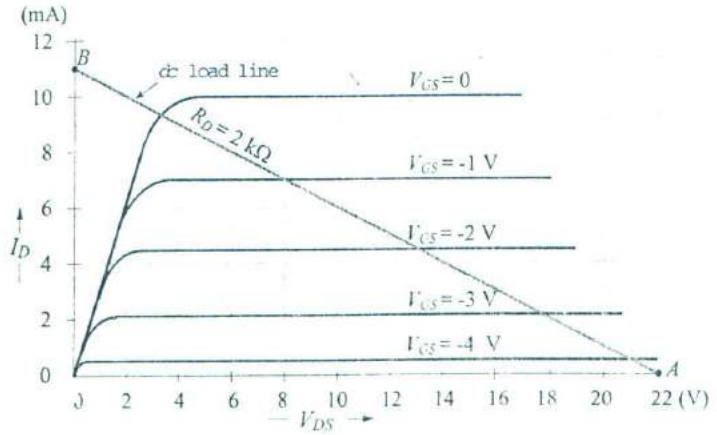


Figure 10-2
DC load line drawn upon FET drain characteristics.

As already explained, the *dc* load line represents all corresponding I_D and V_{DS} levels that can exist in a *FET* circuit, as represented by Eq. 10-1. A point plotted at V_{DS} = 16 V and I_D = 10 mA on Fig. 10-2 does not appear on the load line, and so this combination of voltage and current cannot exist in this particular circuit (Fig. 10-1). The straight line drawn in Ex. 10-1 is the *dc* load line for R_D = 2 kΩ and V_{DD} = 22 V. If either of these two quantities is changed, a new load line must be drawn.

Bias Point (Q-Point)

Just as in the case of a *BJT* circuit, the *dc bias point*, or *quiescent point (Q-point)*, identifies the device current and terminal voltages when there is no *ac* input signal. When a signal is applied to the gate, I_D varies according to the instantaneous amplitude of the signal, producing a variation in V_{DS}.

For a *FET* amplifier circuit, V_{DS} must remain in the pinch-off region of the characteristics. This means that it must not be allowed to fall below the the device pinch-off voltage (V_P in Fig. 10-3), to avoid going into the channel ohmic region. Therefore, in a *FET* bias circuit the drain-source voltage should always be a minimum of (V_P + 1 V), as illustrated.

$$\boldsymbol{V_{DS(min)} = V_P + 1\text{ V}} \qquad \textbf{(10-2)}$$

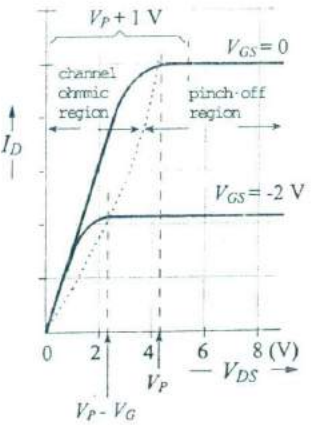


Figure 10-3
In a FET amplifier circuit the drain-source voltage must be a minimum of V_P + 1 V.

Where an external bias voltage (V_G) is included (as in Fig. 10-1), the pinch-off voltage for that bias level on the device characteristics is (V_P - V_G), (see Fig. 10-3). Consequently, the minimum drain-source voltage may be reduced to,

$$V_{DS(min)} = V_P - V_G + 1\ V \qquad \textbf{(10-3)}$$

The bias point for a *BJT* can be selected half-way along the load line, to give the maximum possible symmetrical output voltage variation, (see Section 5-1). To achieve the same result with a *FET*, the bias point must be half way between $V_{DS} = V_{DD}$ and $V_{DS} = V_P$. This is illustrated at Q_1 in Fig. 10-4. When maximum V_{DS} variations are not required, the *FET* bias point can be selected at any convenient point on the *dc* load line (Q_2 in Fig. 10-4), just as in the case of a *BJT* amplifier.

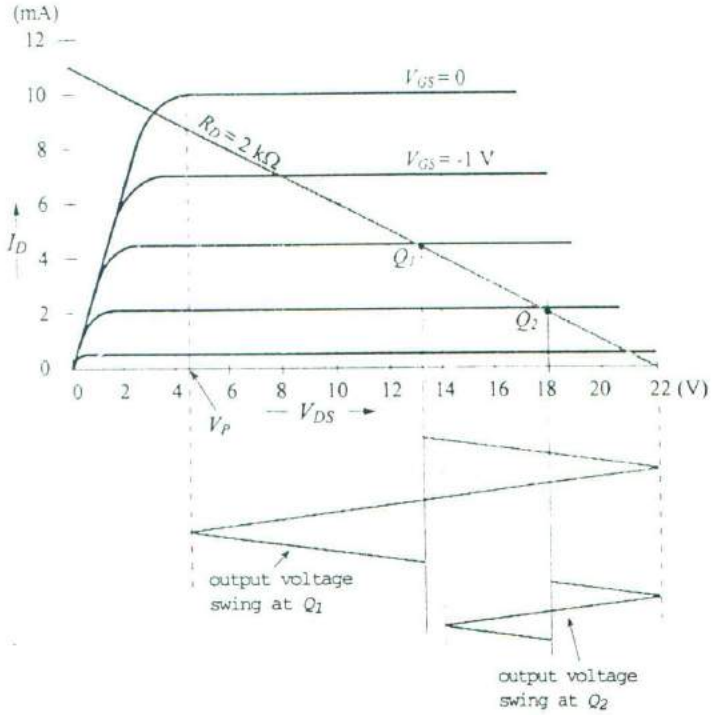


Figure 10-4
The maximum output voltage swing from a FET amplifier circuit depends upon the Q point.

Example 10-2

Estimate the maximum symmetrical output voltage swing for the 2 kΩ load line in Fig. 10-4 when the *FET* is biased to give a Q-point at V_{DS} = 11 V, and when it is biased to give V_{DS} = 20 V.

Solution

For a Q-point at V_{DS} = 11 V:
when I_D *is reduced to zero,* $\Delta V_{DS} = 22\ V - 11\ V$
$= 11\ V$

when I_D is increased to 9 mA, $\Delta V_{DS} = 11\text{ V} - 4\text{ V}$
$= 7\text{ V}$

So, the maximum symmetrical output voltage swing is,

$$V_{o(max)} = \pm 7\text{ V}$$

For a Q-point at $V_{DS} = 20$ V:
when I_D is reduced to zero, $\Delta V_{DS} = 22\text{ V} - 20\text{ V}$
$= 2\text{ V}$

when I_D is increased to 9 mA, $\Delta V_{DS} = 20\text{ V} - 4\text{ V}$
$= 16\text{ V}$

So, the maximum symmetrical output voltage swing is,

$$V_{o(max)} = \pm 2\text{ V}$$

Effect of Source Resistor

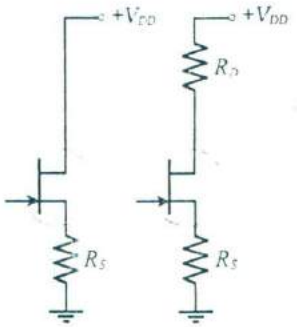
Figure 10-5(a) shows a circuit that has a resistor (R_S) in series with the *FET* source terminal, and the supply voltage connected directly to the drain. In this case R_S is the *dc* load, and Eq. 10-1 is rewritten as,

$$V_{DS} = V_{DD} - I_D R_S$$

The dc load line is drawn exactly as discussed.

In Fig. 10-5(b) drain and source resistors R_D and R_S are both present, and the total *dc* load in series with the *FET* is $(R_D + R_S)$. For drawing the dc load line, Eq. 10-1 is modified to,

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$



(a) R_{Load} = R_S (b) R_{Load} = $R_D + R_S$

Figure 10-5
When a source resistor (R_S) is included in a circuit, R_S is the dc load or part of the total load.

Practise Problems

10-1.1 A 1 kΩ source resistor (R_S) is added to the circuit of Fig. 10-1, as in Fig. 10-5(b). Draw the *dc* load line on the characteristic in Fig. 10-2, and determine V_{DS} when $V_{GS} = -2$ V.

10-1.2 Determine the maximum symmetrical output voltage swing for the circuit in Problem 10-1.1 when the Q-point is at $V_{DS} = 17$ V.

10-2 Gate Bias

Circuit Operation

Consider the *gate bias* circuit shown in Fig. 10-6. The *FET* gate terminal is connected via resistor R_G to a bias voltage V_G. If the gate is directly connected to the bias source (instead of using R_G), any *ac* signal applied to the gate would be short-circuited to V_G.

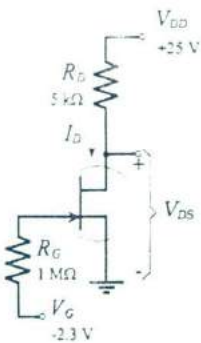


Figure 10-6
FET circuit with gate bias. The gate-source voltage is, $V_{GS} = -V_G$.

There is no gate current to produce a voltage drop across R_G, so the gate-source voltage remains constant at V_G. Depending on the device transfer characteristics, V_G sets the level of I_D in the *FET*. The I_D level can be readily determined, if the transfer characteristic is available for the particular *FET* used in the circuit. If the device is replaced, I_D is determined by the transfer characteristic of the new device. Like the base current in a *BJT* base bias circuit, the *FET* gate voltage does not change when the device characteristics change.

Circuit Analysis

As discussed in Section 9-3, each *FET* of a given type number has maximum and minimum transfer characteristics, and these must be employed to determine the maximum and minimum possible levels of I_D in the circuit. A gate bias circuit is most easily analyzed by drawing a *bias line* vertically on the transfer characteristics from $V_{GS} = -V_G$. The levels of $I_{D(min)}$ and $I_{D(max)}$ are read from the intersections of the bias line with the transfer characteristics, and the maximum and minimum drain-source voltages can then be calculated using these I_D levels.

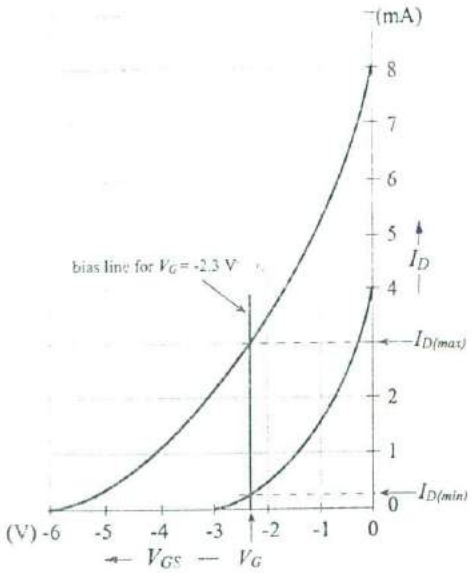


Figure 10-7
The possible drain current levels in a gate bias circuit are determined simply by drawing a bias line vertically on the transfer characteristics at $V_{GS} = V_G$.

Example 10-3

The gate bias circuit in Fig. 10-6 uses a *FET* with the transfer characteristics shown in Fig. 10-7. Determine the maximum and minimum levels of I_D and V_{DS} for the circuit.

Solution

Draw the bias line on the transfer characteristics at,

$$V_{GS} = V_G = -2.3 \text{ V}$$

From the bias line, $I_{D(min)} = 0.25$ mA, and $I_{D(max)} = 3$ mA

$$V_{DS(min)} = V_{DD} - (I_{D(max)} R_D) = 25 \text{ V} - (3 \text{ mA} \times 5 \text{ k}\Omega)$$
$$= 10 \text{ V}$$

$$V_{DS(max)} = V_{DD} - (I_{D(min)} R_D) = 25 \text{ V} - (0.25 \text{ mA} \times 5 \text{ k}\Omega)$$
$$= 23.75 \text{ V}$$

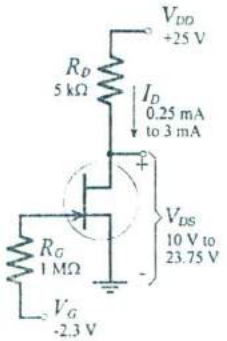


Figure 10-8
Maximum and minimum voltage and current levels for the gate bias circuit in Ex. 10-3.

The maximum and minimum I_D and V_{DS} levels determined in Ex. 10-3 are illustrated by the circuit current and voltage levels in Fig. 10-8, and by the *Q-points* plotted in Fig. 10-9. As already discussed, *JFETs* with a given type number have a wide range of transfer characteristics, so

FET maximum and minimum transfer characteristics should always be used for practical circuit analysis.

The gate bias technique produces a wide range of I_D and V_{DS} levels for any *FET* with a particular type number. It is possible to adjust V_G to set V_{DS} to a desired voltage. However, this is normally done only in an experimental situation. Slightly more complicated bias circuit must be employed for more predictable voltage and current conditions.

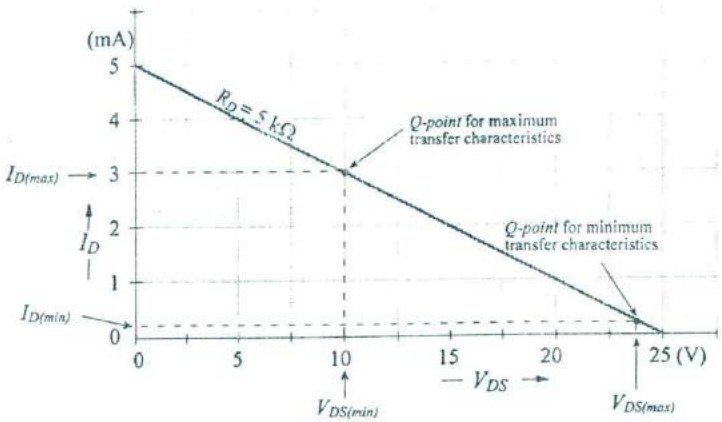


Figure 10-9
Q-points produced by the maximum and minimum transfer characteristics with the gate bias circuit in Ex. 10-3.

Analysis of a gate bias circuit can be performed without drawing the *FET* transfer characteristics. Equation 9-1 is used for plotting the transfer characteristics, so the equation can be applied directly to determine the drain current levels.

Example 10-4
Use Eq. 9-1 to determine $I_{D(max)}$ and $I_{D(min)}$ for the bias circuit in Ex. 10-3.

Solution
From Fig. 10-7, $I_{DSS(max)} = 8$ mA, and $V_{P(max)} = 6$ V

Eq. 9-1, $I_{D(max)} = I_{DSS(max)}\left[1 - \frac{V_{GS}}{V_{P(max)}}\right]^2 = 8\text{ mA}\left[1 - \frac{2.3\text{ V}}{6\text{ V}}\right]^2$

$= 3.04\text{ mA}$

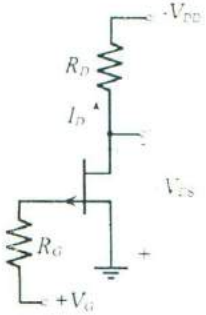
From Fig. 10-7, $I_{DSS(min)} = 4\text{ mA}$, and $V_{P(min)} = 3\text{ V}$

Eq. 9-1, $I_{D(min)} = I_{DSS(min)}\left[1 - \frac{V_{GS}}{V_{P(min)}}\right]^2 = 4\text{ mA}\left[1 - \frac{2.3\text{ V}}{3\text{ V}}\right]^2$

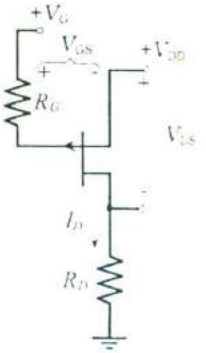
$= 0.22\text{ mA}$

Gate Bias for a p-channel JFET

A gate bias circuit using a *p*-channel *JFET* is shown in Fig. 10-10(a). This is similar to *n*-channel *JFET* gate bias circuits except that V_{DD} is a negative voltage and V_G is a positive quantity. Figure 10-10(b) shows the same *p*-channel *JFET* circuit with a positive supply voltage. In this case, the *FET* source terminal is connected to V_{DD}, and R_D is connected to ground. To reverse bias the gate-channel junctions, the gate terminal must be positive with respect to the source. So, gate bias voltage V_G must be positive with respect to V_{DD}, as illustrated. The *p*-channel gate bias circuit can be analyzed in exactly the same way as an *n*-channel circuit.



(a) *p*-channel *FET* circuit using $-V_{DD}$



(b) *p*-channel *FET* circuit using $+V_{DD}$

Figure 10-10
JFET gate bias circuits using p-channel devices.

Practise Problem

10-2.1 A gate bias circuit has $V_{DD} = 20\text{ V}$, $R_D = 2.7\text{ k}\Omega$, $R_G = 1\text{ M}\Omega$, and $V_G = -1.5\text{ V}$. If the *FET* has the characteristics shown in Fig. 10-7, determine the maximum and minimum V_{DS} levels for the circuit.

10-2.2 The *FET* in the circuit in Problem 10-2.1 is changed to one that has $I_{DSS} = 6\text{ mA}$ and $V_P = 4.5\text{ V}$. Calculate the circuit V_{DS}.

10-3 Self Bias

Circuit Operation

In a *self bias JFET* circuit, gate-source bias is provided by the voltage drop across a resistor in series with the device source terminal. Consider the *n*-channel *JFET* self-bias circuit illustrated in Fig. 10-11. The voltage drop across resistor R_S is,

$$V_S = I_D R_S$$

If $I_D = 1\text{ mA}$ and $R_S = 1\text{ k}\Omega$, then $V_S = 1\text{ V}$. This means that the source terminal in Fig. 10-11 is 1 V positive with respect to ground. Alternatively, ground can be said to be 1 V negative with respect to the source terminal. Because the *FET* gate terminal is grounded via R_G (and there is no voltage drop across R_G), the gate is 1 V negative with respect to the source. That is, the gate-source bias voltage is $V_{GS} = -1\text{ V}$. So, for a self-bias circuit,

$$\boldsymbol{V_{GS} = -I_D R_S} \qquad \textbf{(10-4)}$$

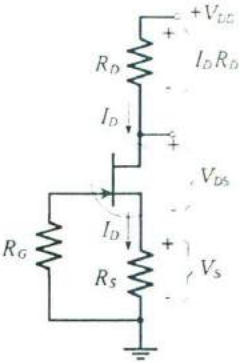


Figure 10-11
JFET self bias circuit using an n-channel device. The gate-source bias voltage is $V_{GS} = -I_D R_S$.

The fact that I_D determines V_{GS}, and that V_{GS} sets the I_D level, means that there is a feedback effect tending to control I_D. Thus, if I_D increases when the device is changed, the increased voltage across R_S results in an increased (negative) gate-source voltage that tends to reduce I_D back toward its original level. Similarly, a fall in I_D produces a reduced V_{GS} which tends to increase I_D toward its original level.

Circuit Analysis

As for all *FET* bias circuits, a graphical technique is most convenient for analysis of a self-bias circuit. In this case, the bias line drawn on the transfer characteristics is quite different from that for the gate bias circuit. The value of R_S and convenient I_D levels are inserted into Eq. 10-4 to determine corresponding V_{GS} levels. The I_D and V_{GS} values are plotted on the transfer characteristics, and the bias line is drawn through them, (see Fig 10-12). The intersection points of the bias line and the transfer characteristics gives the maximum and minimum I_D levels.

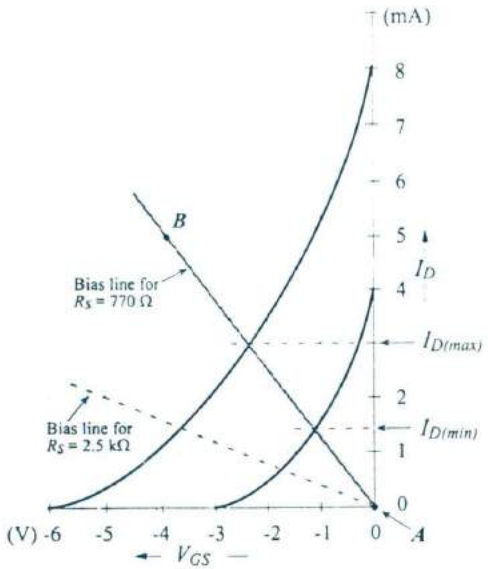


Figure 10-12
The bias line for a self bias circuit is drawn from $I_D = 0$ and $V_{GS} = 0$ at a slope determined by R_S.

Summing the voltage drops across R_D, R_S, and the *FET* drain-source terminals in Fig. 10-11 gives,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S \qquad (10\text{-}5)$$

Equation 10-5 may be used to calculate the maximum and minimum levels of V_{DS} when $I_{D(max)}$ and $I_{D(min)}$ have been determined.

Example 10-5

Analyze the self-bias circuit in Fig. 10-13 to determine $I_{D(max)}$, $I_{D(min)}$, $V_{DSmax)}$, and $V_{DSmin)}$. The transfer characteristics for the *FET* are given in Fig. 10-12.

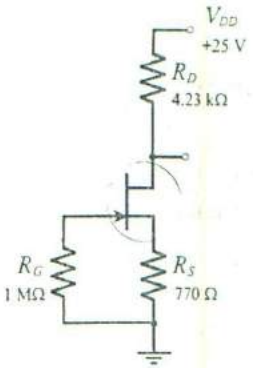


Figure 10-13
FET self bias circuit for Ex. 10-5.

Solution

when $I_D = 0$,

Eq. 10-4, $V_{GS} = -I_D R_S = 0$

Plot *point A* on Fig. 10-12 at,

$$I_D = 0 \text{ and } V_{GS} = 0$$

when $I_D = 5$ mA,

Eq. 10-4, $V_{GS} = -I_D R_S = -(5 \text{ mA} \times 770\ \Omega)$
$= -3.85$ V

Plot *point B* on Fig. 10-12 at,

$$I_D = 5 \text{ mA and } V_{GS} = -3.85 \text{ V}$$

Draw the bias line for $R_S = 770\ \Omega$ through *points A* and *B*.

Where the bias line intersects the transfer characteristics, read

$$I_{D(max)} = 3 \text{ mA and } I_{D(min)} = 1.4 \text{ mA}$$

From Eq. 10-5, $V_{DS(min)} = V_{DD} - I_{D(max)}(R_D + R_S)$
$= 25 \text{ V} - 3 \text{ mA}(4.23 \text{ k}\Omega + 770\ \Omega)$
$= 10$ V

and, $V_{DS(max)} = V_{DD} - I_{D(min)}(R_D + R_S)$
$= 25 \text{ V} - 1.4 \text{ mA}(4.23 \text{ k}\Omega + 770\ \Omega)$
$= 18$ V

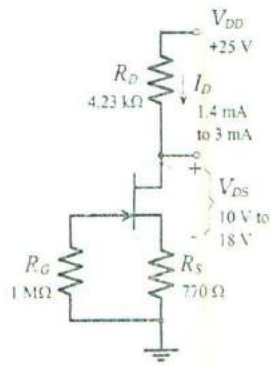


Figure 10-14
Maximum and minimum voltage and current levels for the self bias circuit in Ex. 10-5.

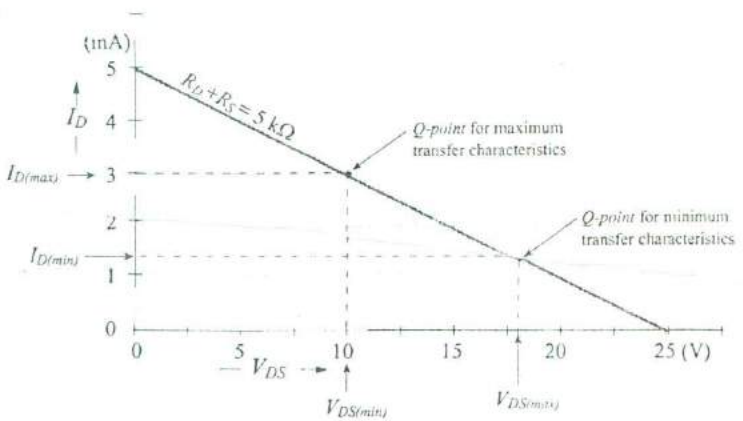


Figure 10-15
Q-points produced by the maximum and minimum transfer characteristics with the self bias circuit in Ex. 10-5.

The maximum and minimum I_D and V_{DS} levels determined in Ex. 10-5 are shown in the circuit in Fig. 10-14, and are illustrated by the *Q-points* plotted in Fig. 10-15. Consideration of Ex. 10-5 shows that closer levels of $I_{D(max)}$ and $I_{D(min)}$ could be obtained by using a larger resistance for R_S. However, as shown by the (dashed) bias line for R_S = 2.5 kΩ in Fig. 10-12, I_D is substantially reduced when larger values of R_S are used.

Self-Bias for a p-channel JFET

A self-biased circuit using a *p*-channel *JFET* is shown in Fig. 10-16. The gate-source bias voltage is once again provided by the voltage drop across source resistor R_S. In this case, the source is negative with respect to the supply voltage ($+V_{DD}$). Because the gate is connected to $+V_{DD}$ via R_G, the gate is is positive with respect to the source terminal. The positive level of V_{GS} provides the reverse bias at the gate-channel junctions of the *p*-channel *FET*. A *p*-channel self-biased circuit can be analyzed in exactly the same way as an *n*-channel circuit.

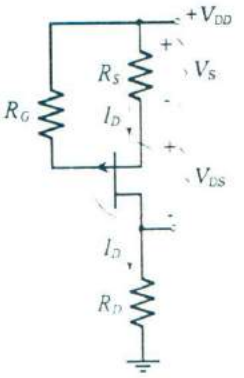


Figure 10-16
JFET self bias circuit using a p-channel device.

Practise Problems

10-3.1 A self bias circuit has V_{DD} = 22 V, R_D = 3.3 kΩ, R_G = 1 MΩ, and R_S = 3.3 kΩ. Using the *FET* characteristics in Fig. 10-12, analyze the circuit to determine the maximum and minimum V_{DS} levels.

10-4 Voltage Divider Bias

Circuit Operation

For the self-bias circuit, it was seen that increasing the resistance of R_S brings $I_{D(max)}$ and $I_{D(min)}$ closer together, but that increased R_S values result in lower I_D levels. As will be demonstrated, *voltage divider bias* allows R_S to be increased without making I_D very small.

Figure 10-17 shows that a voltage divider bias circuit combines the use of a source resistor (R_S) with a gate bias voltage (V_G). The gate bias voltage is derived from the supply voltage by means of the voltage divider (R_1 and R_2), and the source voltage (V_S) depends upon R_S and I_D. The gate terminal and the source terminal are both positive with respect to ground, and the gate-source voltage (V_{GS}) is the difference between V_G and V_S. Because V_S is larger than V_G, the *FET* source terminal is at a higher level than the gate. So, the gate is negative with respect to the source, and the gate-channel junctions are reverse biased.

As in the case of a self-biased circuit, the voltage drop across R_S increases if I_D increases. This produces an increase in $-V_{GS}$, which drives I_D back toward its original level. A decrease in I_D causes a reduction in $-V_{GS}$ which tends to increase I_D.

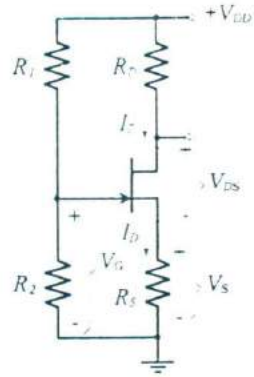


Figure 10-17
JFET voltage divider bias circuit. The gate-source voltage is,
$V_{GS} = V_G - V_S$

Circuit Analysis

Once again, the graphical technique of drawing a bias line on the *FET* transfer characteristics is most convenient for analyzing a

voltage divider bias circuit. An equation relating V_{GS} and I_D must be derived, so that corresponding values of each quantity may be calculated for plotting the bias line.

As discussed,

$$V_{GS} = V_G - I_D R_S \qquad \textbf{(10-6)}$$

Because there is no gate current,

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2} \qquad \textbf{(10-7)}$$

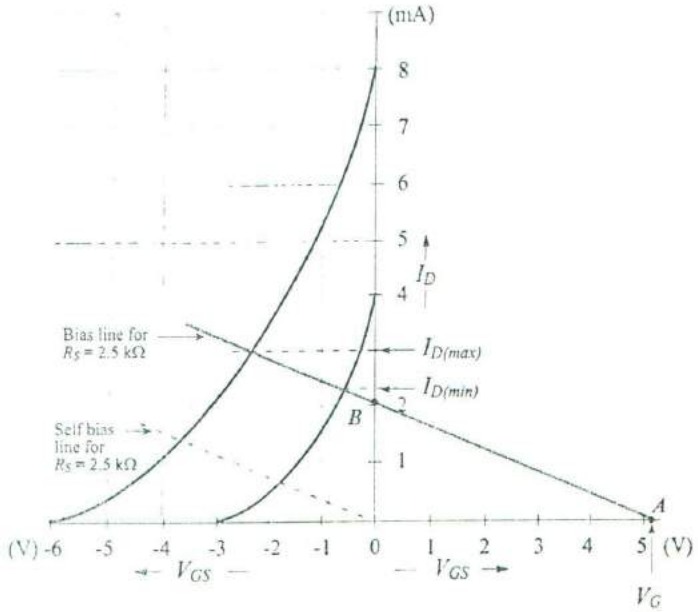


Figure 10-18
The bias line for a voltage divider bias circuit is drawn from the point where $I_D = 0$ and $V_{GS} = +V_G$ at a slope determined by R_S.

Referring to Eq. 10-6, it is seen that

when $I_D = 0$, $\qquad V_{GS} = V_G$

This is a positive quantity, so the bias line is drawn from $+V_G$, as shown in Fig. 10-18. It is seen that this gives higher drain current levels than those obtained when the bias line is drawn from $I_D = 0$ and $V_{GS} = 0$, (dashed line in Fig. 10-18). The analysis of a voltage divider bias circuit is demonstrated in Ex. 10-6.

Example 10-6

Analyze the bias circuit in Fig. 10-19 to determine $I_{D(max)}$, $I_{D(min)}$, $V_{DSmax)}$, and $V_{DSmin)}$. Figure 10-18 shows the transfer characteristics for the *FET*.

Solution

Eq. 10-7, $\qquad V_G = \dfrac{V_{DD} \times R_2}{R_1 + R_2} = \dfrac{25\ \text{V} \times 1\ \text{M}\Omega}{3.8\ \text{M}\Omega + 1\ \text{M}\Omega}$

$= 5.2\ \text{V}$

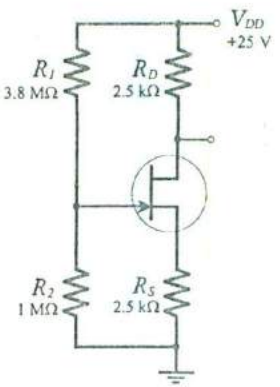


Figure 10-19
FET voltage divider bias circuit for Ex. 10-6.

when $I_D = 0$,

Eq. 10-6, $V_{GS} = V_G - I_D R_S = 5.2\text{ V} - 0$

$= 5.2\text{ V}$

Plot *point A* on Fig. 10-18 at,

$I_D = 0$ and $V_{GS} = +5.2\text{ V}$

when $V_{GS} = 0$,

from Eq. 10-6, $I_D = \dfrac{V_G}{R_S} = \dfrac{5.2\text{ V}}{2.5\text{ k}\Omega}$

$= 2.08\text{ mA}$

Plot *point B* on Fig. 10-18 at,

$I_D = 2.08\text{ mA}$ and $V_{GS} = 0$

Draw the bias line for $R_S = 2.5\text{ k}\Omega$ through *points A* and *B*.

Where the bias line intersects the transfer characteristics, read

$I_{D(max)} = 3\text{ mA}$ and $I_{D(min)} = 2.3\text{ mA}$

From Eq. 10-5, $V_{DS(min)} = V_{DD} - I_{D(max)}(R_D + R_S)$

$= 25\text{ V} - 3\text{ mA}(2.5\text{ k}\Omega + 2.5\text{ k}\Omega)$

$= 10\text{ V}$

and, $V_{DS(max)} = V_{DD} - I_{D(min)}(R_D + R_S)$

$= 25\text{ V} - 2.3\text{ mA}(2.5\text{ k}\Omega + 2.5\text{ k}\Omega)$

$= 13.5\text{ V}$

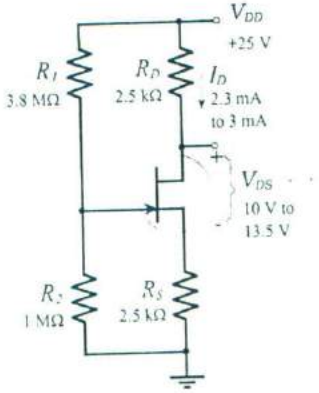


Figure 10-20
Maximum and minimum voltage and current levels for the voltage divider bias circuit in Ex. 10-6.

The maximum and minimum I_D and V_{DS} levels determined for the voltage divider bias circuit in Ex. 10-6 are shown on the circuit diagram in Fig. 10-20, and are illustrated by the *Q*-points plotted in Fig. 10-21.

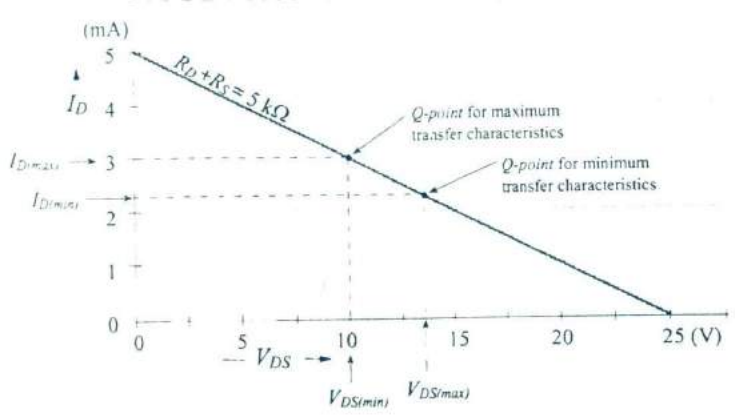


Figure 10-21
Q-points produced by the maximum and minimum transfer characteristics with the voltage divider bias circuit in Ex. 10-6.

Voltage Divider Bias for a p-channel JFET

A voltage divider bias circuit using a *p*-channel *JFET* is shown in Fig. 10-22. As for the *n*-channel circuit, the gate-source bias voltage is the difference between V_G and V_S. In this case, these are both negative with respect to the positive supply voltage (V_{DD}). Because V_S is larger than V_G, the gate terminal is positive with respect to the source, and this reverse biases the gate-channel junctions. A *p*-channel voltage divider bias circuit is analyzed in exactly the same way as an *n*-channel circuit.

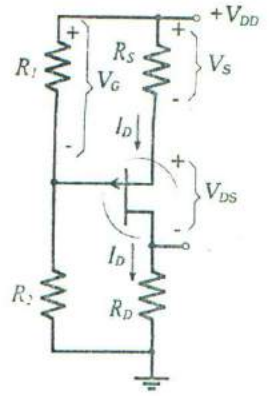


Figure 10-22
JFET voltage divider bias circuit using a p-channel device.

Practise Problems

10-4.1 A voltage divider bias circuit has V_{DD} = 30 V, $R_D = R_S$ = 4.7 kΩ, R_1 = 1 MΩ, and R_2 = 150 kΩ. Using the *FET* characteristics in Fig. 10-18, determine the circuit maximum and minimum V_{DS} levels.

10-5 Comparison of Basic JFET Bias Circuits

The three basic *FET* bias circuits (gate bias, self-bias, and voltage divider bias) are similar in performance to the three basic *BJT* bias circuits, (base bias, collector-to-base bias, and voltage divider bias). Comparing the performance of *FET* bias circuits, it should be recalled that each *FET* type number has maximum and minimum transfer characteristics. The particular transfer characteristic for each individual transistor is normally not known. Therefore, as already stated, *the specified maximum and minimum transfer characteristics must be used when analysing (or designing) a FET bias circuit.*

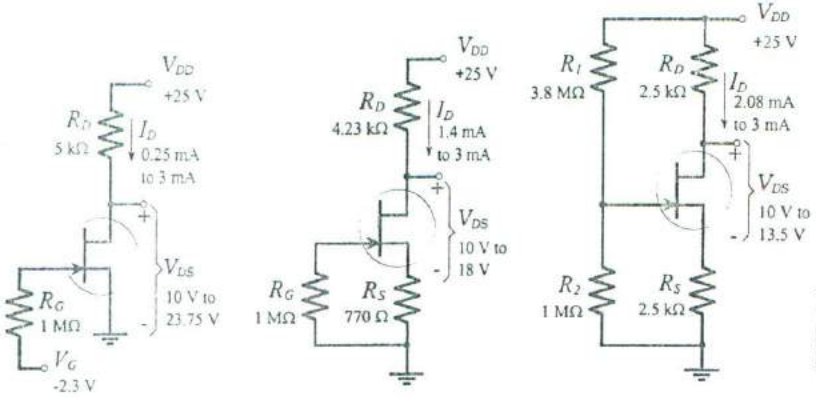


Figure 10-23
Comparison of similar JFET gate bias, self bias, and voltage divider bias circuits.

Consider the basic *JFET* bias circuits reproduced in Fig. 10-23. Each circuit uses a 25 V supply and a 5 kΩ (total) load resistance, and each uses a *FET* with the same maximum and minimum transfer characteristics. The circuits are analysed in Examples 10-3, 10-5, and 10-6 to determine the maximum and minimum I_D and

V_{DS} levels. The calculated quantities are indicated on each circuit in Fig. 10-23, and the Q point ranges are illustrated in Fig. 10-24.

If the *FET* in the gate bias circuit fails and has to be replaced with another (same type number) device, the new V_{DS} level could be anywhere from 10 V to 23.75 V. The self-bias circuit in the same circumstance (with the same *FET* type number) would have a V_{DS} ranging from 10 V to 18 V when the *FET* is replaced. For the voltage divider bias circuit in this situation, the measurable V_{DS} range with a new device would be 10 V to 13.5 V. Clearly, self-bias gives more predictable bias conditions than gate bias, and voltage divider bias gives the most predictable bias conditions. Because of its better performance, voltage divider bias is usually preferred.

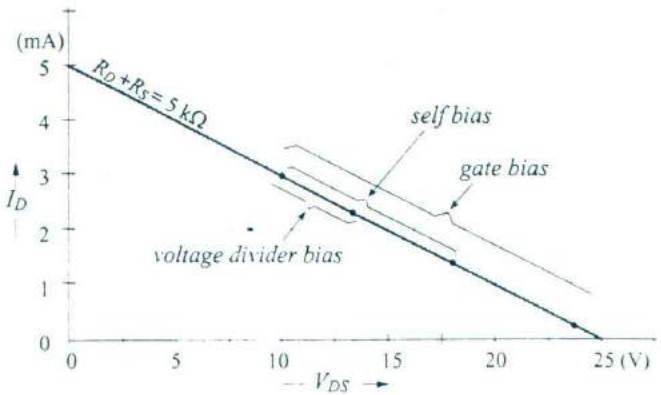


Figure 10-24
Q-point ranges for the gate bias, self bias, and voltage divider bias circuits shown in Fig. 10-23.

Note that, for all three basic bias circuits in Fig. 10-23, the minimum I_D and V_{DS} levels are 3 mA and 10 V, respectively. In Section 10-7, it is shown how *FET* bias circuits may be designed for a given minimum V_{DS}.

Section 10-5 Review

10-5.1 Briefly discuss the three basic *FET* bias circuits, comparing the effect of the bias lines on the maximum and minimum I_D levels.

10-6 Trouble-Shooting JFET Bias Circuits

Voltage Measurement

Trouble-shooting procedures for *FET* bias circuits are similar to those for *BJT* bias circuits. The major difference is that there is only one junction in the *FET* (the gate-channel junction) that might become short-circuited or open-circuited. To determine if the circuit is functioning correctly, the *FET* terminal voltages should all be measured with respect to ground, as illustrated in Fig. 10-25. This is exactly as done for a *BJT* circuit, and, here again, if the voltage levels are not satisfactory, the circuit must be further investigated to locate the fault.

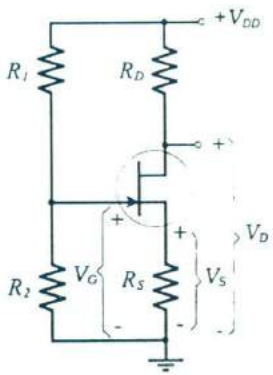


Figure 10-25
When testing a FET bias circuit, all voltage levels should first be measured with respect to the ground or negative supply terminal.

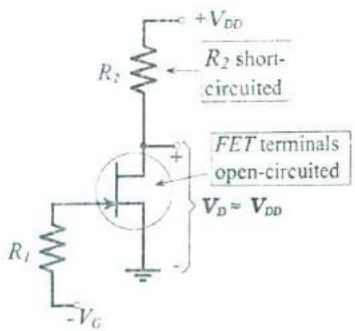
Common Errors

Before proceeding further, the following list of common errors (reproduced from Section 5-6) should be considered. These apply equally to *FET* and *BJT* circuits.

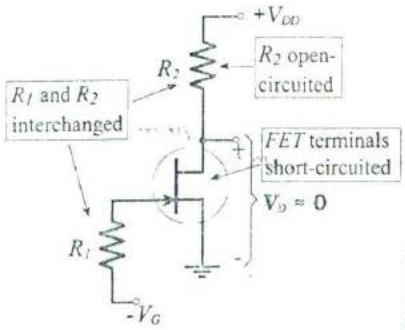
- Power supply not switched *on*.
- Power supply current limiter control incorrectly set.
- Cables incorrectly connected to the power supply.
- Volt-Ohm-Milliammeter (*VOM*) function incorrectly selected.
- Wrong *VOM* terminals used.
- Incorrect component connections.
- Incorrect resistor values.
- Resistors in the wrong places.

Gate Bias

Figure 10-26 illustrates typical error sources in a gate bias circuit. Normally, the gate should be negative with respect to ground, and the drain voltage should be anywhere in the range of perhaps 3 V to (V_{DD} - 2 V). If $V_D \approx V_{DD}$, as in Fig. 10-26(a), the *FET* terminals might be open-circuited, or R_2 might be shorted. When $V_G \approx 0$, as in Fig. 10-26(b), R_1 and R_2 might be interchanged (the high-value and low-value resistors in the wrong places). Other possibilities are that R_2 is open-circuited, or the *FET* terminals are short-circuited.



(a) Drain voltage equal to supply voltage

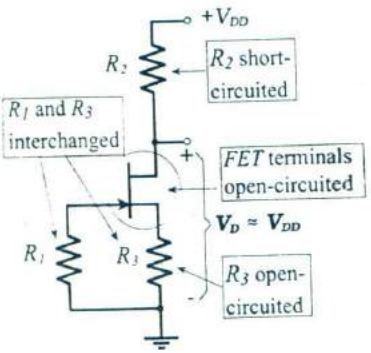


(b) Drain voltage equal to zero

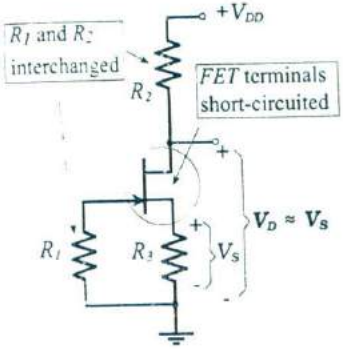
Figure 10-26
The measured FET terminal voltages in a gate bias circuit can indicate possible circuit errors.

Self Bias

Possible reasons for incorrect voltage levels in a self-bias circuit are illustrated in Fig. 10-27. These are similar to those discussed for gate bias. If V_D is approximately equal to V_{DD} [Fig 10-27(a)], resistor R_3 or one of the transistor terminals could to be open-circuited, or R_1 and R_3 might be interchanged. Alternatively, R_2 might be short circuited. If V_D equals V_S [Fig 10-27(b)], the *FET* transistor terminals might be short-circuited, or R_1 and R_2 might be in the wrong places (interchanged).



(a) Drain voltage equal to supply voltage

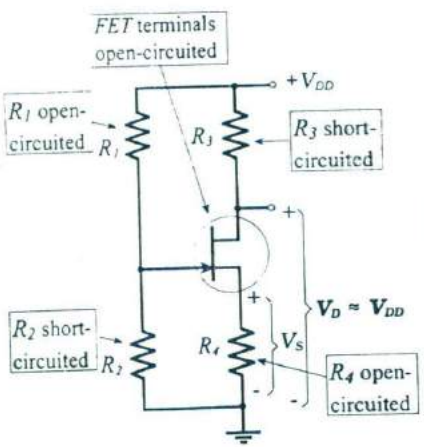


(b) Drain voltage equal to source voltage

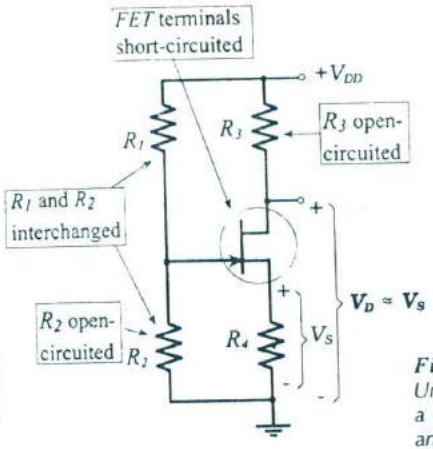
Figure 10-27
Typical incorrect terminal voltages in a FET self bias circuit, and probable circuit faults.

Voltage Divider Bias

Unsatisfactory voltage measurements and probable errors in a voltage divider bias circuit are shown in Fig. 10-28. If V_D equals V_{DD} [Fig. 10-28(a)], R_1 or R_4 might be open-circuited. Alternatively, R_2 or R_3 might be short-circuited, or the *FET* terminals might be open-circuited. When V_D approximately equals V_S [Fig. 10-28(b)], R_2 might be open-circuited, or R_1 and R_2 might be interchanged. Another possibility is that the *FET* terminals are short-circuited.



(a) Drain voltage equal to supply voltage



(b) Drain voltage equal to source voltage

Figure 10-28
Unsatisfactory terminal voltages in a FET voltage divider bias circuit, and probable circuit faults.

Section 10-6 Review

10-6.1 Briefly discuss the proceedure for testing *FET* bias circuits. List possible faults for each bias circuit type (a) when $V_{DS} \approx 0$, (b) when $V_D \approx V_{DD}$.

10-7 JFET Bias Circuit Design

Design Approach

Design of *FET* bias circuits is just as simple as design of *BJT* bias circuits. One major difference is that *FET* circuit design normally uses a graphical approach involving the drawing of a bias line on the device transfer characteristics, as in the case of *FET* circuit analysis. Normally the type number of the *FET* to be used in the circuit is known, and the maximum and minimum transfer characteristics are available or can be plotted. A maximum drain current ($I_{D(max)}$) is selected at a point on the maximum transfer characteristic (see Fig. 10-29), and the bias line is drawn through this point. As will be explained, this procedure applies to all types of bias circuits. The selected level of $I_{D(max)}$ is used to calculate the values of resistors connected to the drain and source terminals.

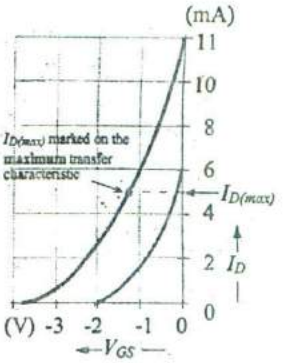


Figure 10-29
The first step in FET bias circuit design is selection of I_D on the maximum transfer characteristic.

Instead of using the maximum transfer characteristics, suppose that the minimum characteristics, or some characteristic between the maximum and minimum, is used in the circuit design. Now, if the *FET* happens to have the maximum transfer characteristic for the device type number, I_D will be larger than the design value. Consequently, the resistor voltage drops ($I_D R_D$ and $I_D R_S$) will be greater than intended (see Fig. 10-30). In this case, V_{DS} will be smaller than its design level, the *FET* might be forced into the channel ohmic region of its characteristics, and the circuit is unlikely to function correctly. Therefore,

always use the device maximum transfer characteristic when designing a FET bias circuit.

As already explained, a *FET* has a very high input resistance, so high-value bias resistors can be used at the gate terminal. However, there are disadvantages to using extremely high resistance values. A charge accumulated at the gate can take a long time to *leak off* through a very high resistance. In this case, the gate voltage might not be a stable quantity, and consequently, the drain current could be unpredictable. High-value bias resistors also generate unwanted thermal noise (see Section 8-6), and they readily pick-up stray radio-frequency signals. For these reasons, 1 MΩ is normally a reasonable upper limit for bias resistors.

In all situations where resistor values are calculated, the closest standard-value components are selected, (see Appendix 2-1). Normally, ±10% tolerance resistors are always used, and the more expensive ±5% and ±1% components are employed only where greater precision is required.

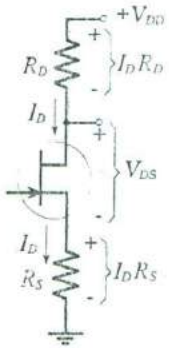


Figure 10-30
*When the maximum transfer characteristic is **not** used in FET circuit design calculations, the I_D level can be greater than the design value, and the FET can be forced into the channel ohmic region of its characteristic.*

Gate Bias Circuit Design

Design of a gate bias circuit is very simple. As explained, the desired maximum I_D level is marked on the maximum transfer characteristics for the *FET*. The bias line is drawn vertically through this point, and the required gate bias voltage ($-V_G$) is indicated where the bias line intersects the V_{GS} scale. Alternatively, V_{GS} can be calculated by rewriting Eq. 9-1,

$$V_{GS} = V_P\left[1 - \sqrt{(I_D/I_{DSS})}\right] \qquad (10\text{-}8)$$

Because the circuit design uses $I_{D(max)}$, the voltage drop across R_D is a maximum, and consequently, the drain-source voltage (V_{DS}) is a minimum. So, the drain resistor is calculated as,

$$R_D = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} \qquad (10\text{-}9)$$

As discussed, the bias resistor (R_G) is usually selected as 1 MΩ, although a lower resistance value may be used.

Figure 10-31 shows the equations involved in designing a gate bias circuit, and Ex. 10-7 demonstrates the design procedure.

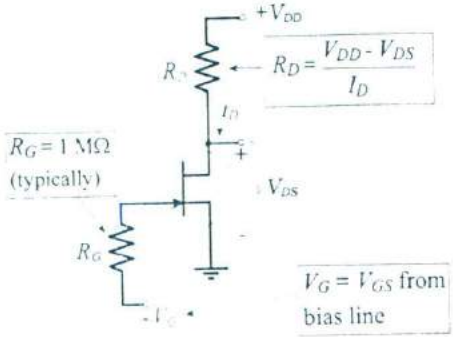


Figure 10-31
FET gate bias circuit design.

Example 10-7

Design a gate bias circuit (as in Fig. 10-31) to have $I_{D(max)}$ = 3 mA and $V_{DS(min)}$ = 10 V. The FET to be used has the transfer characteristics in Fig. 10-32, and the supply voltage is V_{DD} = 25 V.

Solution

On the maximum transfer characteristic, mark

$I_{D(max)}$ = 3 mA (point *X* on Fig. 10-32)

Draw the bias line vertically through point *X*.

Read the required bias voltage where the bias line intersects the V_{GS} scale,

V_{GS} = -2.3 V

Alternatively,

Eq. 10-8, $V_{GS} = V_P\left[1 - \sqrt{(I_D/I_{DSS})}\right]$

$= -6\text{ V}[1 - \sqrt{(3\text{ mA}/8\text{ mA})}]$

$= -2.3$ V

Select R_G = 1 MΩ (see text)

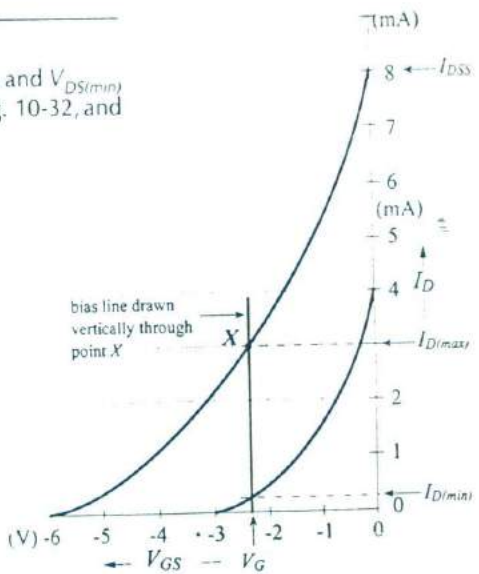


Figure 10-32
FET transfer characteristic and bias line for Ex. 10-7.

Eq. 10-9, $$R_D = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} = \frac{25\text{ V} - 10\text{ V}}{3\text{ mA}}$$

$$= 5\text{ k}\Omega \text{ (use 4.7 k}\Omega\text{ standard value)}$$

From Fig. 10-32, note that, $I_{D(min)} = 0.25$ mA

The calculated resistor values are shown in Fig. 10-33, and the circuit is analyzed in Ex. 10-3.

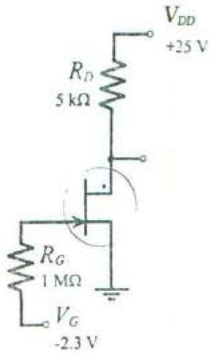


Figure 10-33
FET gate bias circuit designed in Ex. 10-7.

Self Bias Circuit Design

As for gate bias, the procedure for designing a self bias circuit (Fig. 10-34) commences with $I_{D(max)}$ being marked on the *FET* maximum transfer characteristic (Fig. 10-35). The bias line is then drawn through this point and the point where $I_{DS} = 0$ and $V_{GS} = 0$. The value of the source resistor (R_S) is determined from the slope of the bias line.

$$R_S = \frac{\Delta V_{GS}}{\Delta I_D} \qquad \textbf{(10-10)}$$

The total resistance in series with the *FET* drain-source terminals (Fig. 10-34) is ($R_D + R_S$). So, Eq. 10-9 can be modified to calculate this quantity.

$$R_D + R_S = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} \qquad \textbf{(10-11)}$$

With R_S already known, R_D is easily determined. Gate resistor R_G is normally selected as 1 MΩ, or lower, as discussed.

Figure 10-34 shows the equations for designing a self bias circuit, and Ex. 10-8 demonstrates the design procedure.

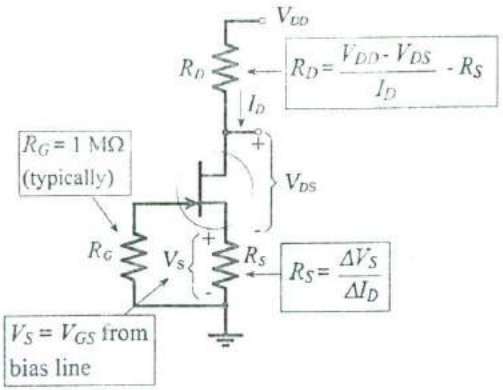


Figure 10-34
FET self bias circuit design.

Example 10-8

Design a self bias circuit (as in Fig. 10-34) to have $I_{D(max)} = 3$ mA and $V_{DS(min)} = 10$ V. The *FET* transfer characteristics are shown in Fig. 10-35, and the supply voltage is $V_{DD} = 25$ V.

Solution

On maximum the transfer characteristics, mark

$$I_{D(max)} = 3 \text{ mA (point } X \text{ on Fig. 10-35)}$$

Mark point Y at $I_D = 0$ and $V_{DS} = 0$

Draw the bias line through points X and Y.

From the bias line: $\Delta V_{GS} = 2.3$ V, and $\Delta I_D = 3$ mA

Eq. 10-10, $$R_S = \frac{V_{GS}}{I_D} = \frac{2.3 \text{ V}}{3 \text{ mA}}$$

$$\approx 770\ \Omega \text{ (use 750 } \Omega, \pm 5\% \text{ standard value)}$$

Eq. 10-11, $$R_D + R_S = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} = \frac{25 \text{ V} - 10 \text{ V}}{3 \text{ mA}}$$

$$= 5 \text{ k}\Omega$$

$$R_D = (R_D + R_S) - R_S = 5 \text{ k}\Omega - 770\ \Omega$$

$$= 4.23 \text{ k}\Omega \text{ (use 3.9 k}\Omega \text{ standard value)}$$

Select $R_G = 1$ MΩ (see text)

From Fig. 10-35, note that $I_{D(min)} = 1.4$ mA

The calculated resistor values are shown in Fig. 10-36, and the circuit is analyzed in Ex. 10-5.

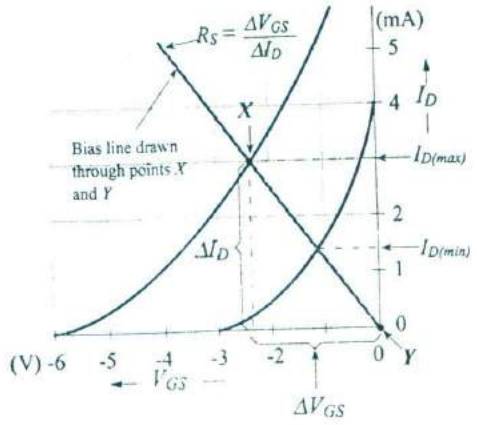


Figure 10-35
FET transfer characteristic and bias line for Ex. 10-8.

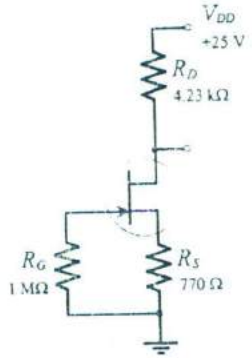


Figure 10-36
FET self bias circuit designed in Ex. 10-8.

Voltage Divider Bias Circuit Design

As always, circuit design commences with the specification of V_{DD}, $I_{D(max)}$, and $V_{DS(min)}$. The maximum drain current is plotted on the device maximum transfer characteristic, then either the resistance of R_S or the level of V_G must be determined before the bias line can be drawn for a voltage divider bias circuit.

With $V_{DS(min)}$ specified, the remaining portion of the supply voltage (V_{DD} - $V_{DS(min)}$) is split between V_S and V_{RD}. It is shown in Chapter 11 that the voltage gain of a *FET* amplifier stage is directly proportional to R_D. Maximum gain is achieved by selecting R_D as large as possible, and for a given level of I_D this requires the greatest possible voltage V_{RD}. However, the best bias stability is achieved by selecting R_S as large as possible, and this dictates maximum V_S. A reasonable compromise between these two conflicting requirements (maximum V_{RD} and maximum V_S) is to simply make the two voltage drops (and the two resistors) equal. Equation 10-11 is used to calculate ($R_D + R_S$), and this is divided to give two equal resistors.

Once R_S is determined, the bias line can be drawn through $I_{D(max)}$ with the slope of the line set by R_S. This requires that the V_{GS} scale be extended positively, as shown in Fig. 10-37.

From Eq. 10-10,

$$\Delta V_{GS} = \Delta I_D \times R_S \qquad \textbf{(10-12)}$$

The gate bias voltage (V_G) is read from the intersection of the bias line and the (extended) V_{GS} scale (Fig. 10-37). R_2 is normally the smallest resistor in the voltage divider. So, R_2 is usually selected as 1 MΩ, for the reasons already discussed for R_G in the gate bias and self bias circuits. R_1 is then calculated from R_2 and the resistor voltage drops. From Eq. 10-7,

$$R_1 = \frac{(V_{DD} - V_G) \times R_2}{V_G} \qquad \textbf{(10-13)}$$

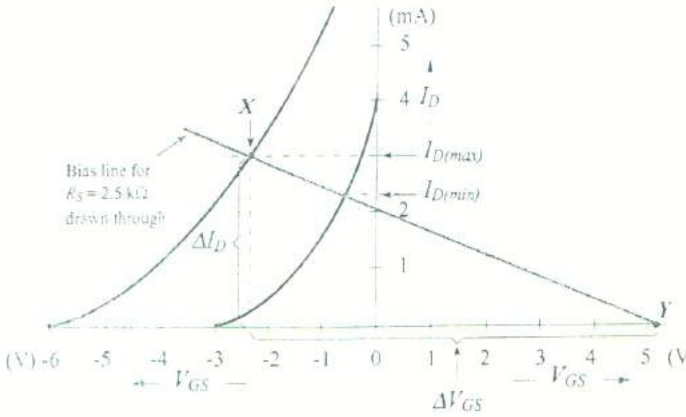


Figure 10-37
FET transfer characteristic and bias line for voltage divider bias circuit design.

Another approach that can be used to determine R_S is to specify a minimum drain current, and mark $I_{D(min)}$ on the minimum drain characteristic (after marking $I_{D(max)}$). The bias line is then drawn through the $I_{D(max)}$ and $I_{D(min)}$ points. The slope of the bias line and its intersection with the V_{GS} scale dictates R_S and V_G, respectively.

The design equations for a voltage divider bias circuit are shown on Fig. 10-38, and Ex. 10-9 demonstrates the design procedure.

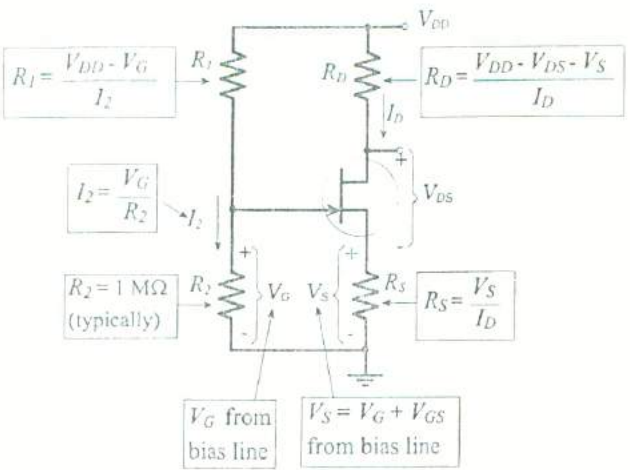


Figure 10-38
FET voltage divider bias circuit design.

Example 10-9

Design a voltage divider bias circuit (as in Fig. 10-38) to have $I_{D(max)} = 3$ mA and $V_{DS(min)} = 10$ V. Use the *FET* transfer characteristics in Fig. 10-37, and a supply voltage of $V_{DD} = 25$ V.

Solution

Eq. 10-11,
$$R_D + R_S = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} = \frac{25\text{ V} - 10\text{ V}}{3\text{ mA}}$$
$$= 5\text{ k}\Omega$$

Select,
$$R_D = R_S = \frac{R_D + R_S}{2} = \frac{5\text{ k}\Omega}{2}$$
$$= 2.5\text{ k}\Omega \text{ (use 2.2 k}\Omega\text{ standard value)}$$

On the maximum transfer characteristics, mark

$I_{D(max)} = 3$ mA (point *X* on Fig. 10-37)

For $\Delta I_D = 3$ mA,

Eq. 10-12,
$$\Delta V_{GS} = \Delta I_D \times R_S = 3\text{ mA} \times 2.5\text{ k}\Omega$$
$$= 7.5\text{ V}$$

Mark point *Y* at $\Delta I_D = 3$ mA and $\Delta V_{DS} = 7.5$ V from point *X*.

Draw the bias line through points *X* and *Y*.

From the bias line: $V_G = 5.2$ V

Alternatively,

Eq. 10-8,
$$V_{GS} = V_P\left[1 - \sqrt{(I_D/I_{DSS})}\right] = -6\text{ V}[1 - \sqrt{(3\text{ mA}/8\text{ mA})}]$$
$$= -2.3\text{ V}$$

$$V_S = I_D \times R_S = 3\text{ mA} \times 2.5\text{ k}\Omega$$
$$= 7.5\text{ V}$$

$$V_G = V_S - V_{GS} = 7.5\text{ V} - 2.3\text{ V}$$
$$= 5.2\text{ V}$$

Select $R_2 = 1\text{ M}\Omega$ (see text)

Eq. 10-13,
$$R_1 = \frac{(V_{DD} - V_G) \times R_2}{V_G} = \frac{(25\text{ V} - 5.2\text{ V}) \times 1\text{ M}\Omega}{5.2\text{ V}}$$
$$= 3.8\text{ M}\Omega \text{ (use 3.9 M}\Omega\text{ standard value)}$$

From Fig. 10-37, note that $I_{D(min)} = 2.3$ mA

The calculated resistor values are shown in Fig. 10-39, and the circuit is analyzed in Ex. 10-6.

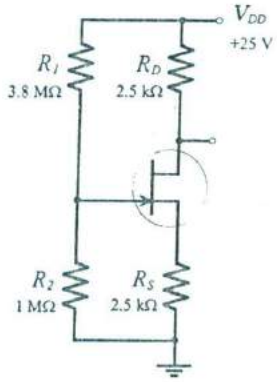


Figure 10-39
FET voltage divider bias circuit designed in Ex. 10-9.

Designing with Standard-Value Resistors

Each time a resistor value is calculated the nearest (higher or lower) standard value should be selected, as shown in the preceding examples. Sometimes it will be appropriate to select a resistance higher than the calculated value, and sometimes a lower value should be used. For example, if a resistance is calculated using a minimum current level, it is usually best to select a lower resistance value so that the current is higher than the specified minimum. Regardless of how the standard values are selected, the new current level or voltage drop produced by the standard value component should be calculated before proceeding with the design. This approach is employed in design examples in the next section.

Practise Problems

10-7.1 A *JFET* gate bias circuit using $V_{DD} = 30$ V is to have $I_{D(max)} = 4$ mA and $V_{DS(min)} = 11$ V. Design the circuit using the transfer characteristics in Fig. 10-32.

10-7.2 Design a *JFET* self bias circuit to have $I_{D(max)} = 2$ mA and $V_{DS(min)} = 8$ V. The supply voltage is $V_{DD} = 20$ V, and the *FET* transfer characteristics are shown in Fig. 10-35.

10-7.3 Design a *JFET* voltage divider bias circuit to have $I_{D(max)} = 1.5$ mA and $V_{DS(min)} = 10$ V. The supply voltage is $V_{DD} = 27$ V, and the *FET* transfer characteristics are shown in Fig. 10-37.

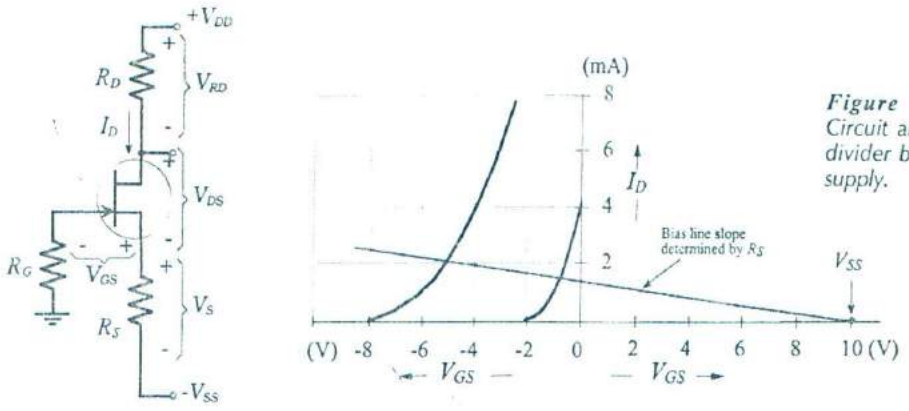
10-8 More JFET Bias Circuits

Use of Plus/Minus Supplies

When plus/minus supply voltages are to be used with a *FET* bias circuit, the gate terminal is usually grounded via R_G, as illustrated in Fig. 10-40(a). In this case, the circuit is essentially a voltage divider bias circuit with the gate bias voltage equal to the level of the negative supply voltage, ($V_G = V_{SS}$). The (reverse) gate-source bias voltage ($-V_{GS}$) makes the source terminal $+V_{GS}$ above ground. So,

$$V_S = V_{SS} + V_{GS} \qquad \textbf{(10-14)}$$

When the voltage levels are understood, the type of circuit in Fig. 10-40(a) can be designed using a procedure similar to that for a voltage divider bias circuit. $I_{D(max)}$ is plotted on the maximum transfer characteristics, and V_{GS} is read from the horizontal axis. V_{GS} can also be determined by substituting $I_{D(max)}$, $I_{DSS(max)}$, and $V_{P(max)}$ into Eq. 10-8. Then, with the desired maximum voltage drops known, R_D and R_S are readily calculated. R_G is selected as 1 MΩ, or less, for the reasons already discussed.



(a) Circuit using ± supply (b) bias line for circuit using ± supply

Figure 10-40
Circuit and bias line for voltage divider bias using a plus/minus supply.

Analysis procedure for this circuit is also like that for a voltage divider bias circuit. One point on the bias line is plotted on the transfer characteristics at $V_G = V_{SS}$, as shown on Fig. 10-40(b), and the bias line is drawn at the slope determined by R_S. As always, the bias line intersections with the maximum and minimum characteristics gives the $I_{D(max)}$ and $I_{D(min)}$ levels.

Drain Feedback

The *drain feedback* bias circuit in Fig. 10-41 is essentially a voltage divider bias circuit. However, instead of V_G being derived from the supply voltage, the *FET* drain voltage (V_D) is divided by R_1 and R_2 to produce V_G. Modifying Eq. 10-7,

$$V_G = \frac{V_D \times R_2}{R_1 + R_2} \qquad \textbf{(10-15)}$$

The circuit is designed for a particular level of V_D and I_D, and the voltage drop across R_S helps to stabilise I_D, as in other voltage divider bias circuits. The voltage drop across R_D also provides feedback that helps to correct changes in I_D. When I_D is greater than the design value, V_{RD} is increased, V_D is reduced, and thus V_G is lowered to drive I_D back toward its original level. The two feedback effects (V_{RD} changes and V_{RS} changes) tend to keep $I_{D(min)}$ and $I_{D(max)}$ closer than in an ordinary voltage divider bias circuit.

Design procedure for this circuit is the same as for voltage divider bias with the exception that the voltage drop across R_1 is $(V_D - V_G)$ instead of $(V_{DD} - V_G)$. For circuit analysis a bias line should be drawn on the transfer characteristics, as always. This requires the equation relating V_{GS} and I_D.

$$V_{GS} = \frac{R_2 (V_{DD} - I_D R_D)}{R_1 + R_2} - I_D R_S \qquad \textbf{(10-16)}$$

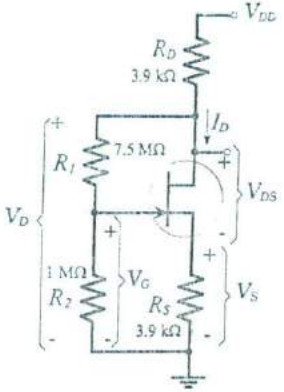


Figure 10-41
FET drain feedback bias circuit.

Example 10-10

Design the drain feedback circuit in Fig. 10-41 to use a *2N5458 FET* with a 20 V supply, and to have $I_{D(max)} = 1.5$ mA and $V_{DS(min)} = 8$ V.

Solution

Eq. 10-11, $$R_D + R_S = \frac{V_{DD} - V_{DS(min)}}{I_{D(max)}} = \frac{20\text{ V} - 8\text{ V}}{1.5\text{ mA}}$$

$$= 8\text{ k}\Omega$$

Select, $$R_D = R_S = \frac{R_D + R_S}{2} = \frac{8\text{ k}\Omega}{2}$$

$$= 4\text{ k}\Omega \text{ (use 3.9 k}\Omega\text{ standard value)}$$

From Appendix 1-11, $I_{DSS(max)} = 9$ mA, and $V_{P(max)} = 7$ V (for a *2N5458*)

Eq. 10-8, $$V_{GS(max)} = V_P\left[1 - \sqrt{(I_D/I_{DSS})}\right] = -7\text{ V}\left[1 - \sqrt{(1.5\text{ mA}/9\text{ mA})}\right]$$

$$= -4.14\text{ V}$$

$$V_S = I_D R_S = 1.5\text{ mA} \times 3.9\text{ k}\Omega$$

$$= 5.85\text{ V}$$

$$V_G = V_S + V_{GS(max)} = 5.85\text{ V} - 4.14\text{ V}$$

$$= 1.7\text{ V}$$

$$V_D = V_{DD} - I_D R_D = 20\text{ V} - (1.5\text{ mA} \times 3.9\text{ k}\Omega)$$

$$= 14.2\text{ V}$$

Select $R_2 = 1\text{ M}\Omega$

From Eq. 10-15, $$R_1 = \frac{(V_D - V_G) \times R_2}{V_G} = \frac{(14.2\text{ V} - 1.7\text{ V}) \times 1\text{ M}\Omega}{1.7\text{ V}}$$

$$= 7.4\text{ M}\Omega \text{ (use 7.5 M}\Omega\text{, }\pm 5\%\text{ standard value)}$$

Constant Current Bias

As already discussed, the bias lines with the smallest slope give the closest levels of $I_{D(min)}$ and $I_{D(max)}$. In the two circuits in Fig. 10-42 the bipolar transistor (Q_2) keeps the *FET* source current constant. Consequently, as illustrated in Fig. 10-43, the bias line is drawn horizontally on the transfer characteristics, showing $I_{D(min)} = I_{D(max)}$, with different V_{GS} levels.

Both circuits provide bias voltage V_B to the base of Q_2, to give,

$$\boldsymbol{I_D = I_C \approx I_E = \frac{V_B - V_{BE}}{R_E}} \qquad \textbf{(10-17)}$$

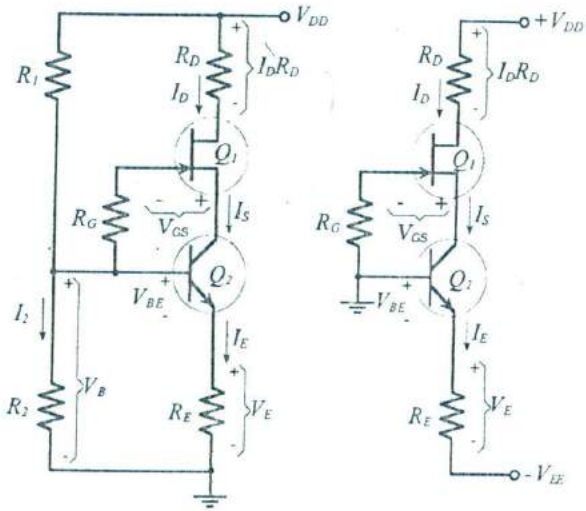
The circuit in Fig. 10-42(a) uses voltage divider bias to derive V_B from V_{DD}, and in Fig. 10-42(b) $V_B = V_{EE}$. In both cases, the *FET* gate is connected to the base of Q_2 via resistor R_G, and $V_{GS} = -V_{CB}$.

Design of each of the circuit in Fig. 10-42 simply involves

selection of appropriate voltage and current levels and calculation of the resistors. The emitter resistor voltage drop (V_E) should typically be a minimum of 5 V, but satisfactory results can be obtained with 3 V. It can, of course, be much larger than 5 V, as would normally be the case in Fig. 10-42(b). In both circuits,

$$V_B = V_E + V_{BE}$$

The level of V_B calculated in this way can be used to determine the ratio of R_1 and R_2 in Fig. 10-42(a). For the circuit in Fig. 10-42(b), V_{EE} dictates the V_B and V_E levels.



(a) Voltage divider bias with constant current source

(b) Circuit with a ± supply and a constant current source

Figure 10-42
FET circuits with BJT constant current bias circuits. In each case I_S is held constant at the I_C level.

The maximum V_{GS} level is determined by plotting I_D on the maximum transfer characteristic for the *FET*, and then reading $V_{GS(max)}$ at I_D. Alternatively, V_{GS} can be calculated from Eq. 10-8. The source terminal voltage is more positive than the gate. The equation for V_S

$$V_S = V_B - V_{GS} \qquad \textbf{(10-18)}$$

Analysis of each of the circuits in Fig. 10-42 is very simple. Once V_B is determined, I_D is calculated using Eq. 10-17. $V_{GS(max)}$ and $V_{GS(min)}$ are found by drawing the bias line for I_D on the transfer characteristics, or by substituting I_D, V_P, and I_{DSS} into Eq. 10-8.

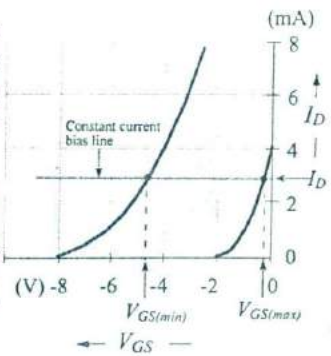


Figure 10-43
Bias line for FET constant current bias circuits.

Example 10-11

Design the constant current bias circuit in Fig. 10-42(b) to use a *2N5459 FET* with a ±20 V supply, and to have $I_{D(max)} = 3$ mA and $V_{DS(min)} = 9$ V.

Solution

$$V_E = V_{EE} - V_{BE} = 20\text{ V} - 0.7\text{ V}$$
$$= 19.3\text{ V}$$

$$R_E = \frac{V_E}{I_D} = \frac{19.3\text{ V}}{3\text{ mA}}$$
$$= 6.4\text{ k}\Omega \text{ (use 6.8 k}\Omega\text{ standard value)}$$

I_D becomes $$\frac{V_E}{R_E} = \frac{19.3\text{ V}}{6.8\text{ k}\Omega}$$
$$= 2.83\text{ mA}$$

From Appendix 1-11, $I_{DSS(max)} = 16$ mA, and $V_{P(max)} = 8$ V (for a *2N5459*)

Eq. 10-8. $$V_{GS(max)} = V_P[1 - \sqrt{(I_D/I_{DSS})}]$$
$$= -8\text{ V}[1 - \sqrt{(2.83\text{ mA}/16\text{ mA})}]$$
$$= -4.6\text{ V}$$

Eq. 10-18. $$V_S = V_B - V_{GS} = 0 - (-4.6\text{ V})$$
$$= +4.6\text{ V}$$

$$V_{RD} = V_{DD} - V_{DS(min)} - V_S = 20\text{ V} - 9\text{ V} - 4.6\text{ V}$$
$$= 6.4\text{ V}$$

$$R_D = \frac{V_{RD}}{I_D} = \frac{6.4\text{ V}}{2.83\text{ mA}}$$
$$= 2.26\text{ k}\Omega \text{ (use 2.2 k}\Omega\text{ standard value)}$$

Select $R_G = 1\text{ M}\Omega$

Figure 10-44 shows the circuit voltage and current levels when the *FET* has $I_{DSS(max)}$ and $V_{P(max)}$ as used in the design. When the *FET* does not have the maximum parameters, only V_{GS} and V_{DS} should change.

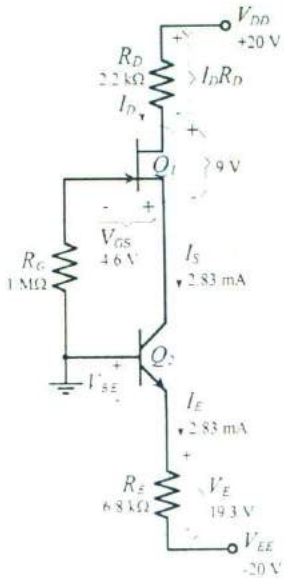


Figure 10-44
Constant current bias circuit designed in Ex. 10-11.

Practise Problems

10-8.1 Design the voltage divider bias circuit in Fig 10-40(a) to use $V_{DD} = \pm 18$ V. The circuit is to have $I_{D(max)} = 2.5$ mA and $V_{DS(min)} = 7$ V, and the *FET* has the transfer characteristics in Fig. 10-37.

10-8.2 The constant current bias circuit in Fig. 10-42(b) is to have a *2N5457 FET*, $V_{DD} = 30$ V, and $V_{EE} = -12$ V. The bias conditions are to be $I_{D(max)} = 2$ mA and $V_{DS(min)} = 8$ V. Design the circuit.

10-8.3 Design a drain feedback bias circuit, as in Fig. 10-41, to have $I_{D(max)} = 2.5$ mA and $V_{DS(min)} = 9$ V. A *2N5457 FET* is the be used, and the supply is $V_{DD} = 24$ V.

10-9 Use of Universal Transfer Characteristic

Universal Transfer Characteristic

A *universal transfer characteristic* for a *FET* is simply a transfer characteristic plotted with $I_{DSS} = 1$ and $V_P = 1$. Then, instead of the scales being calibrated in milliamps and volts, they are marked as the ratios I_D/I_{DSS} and V_{GS}/V_P. To construct the universal transfer characteristic, Eq. 9-1 is rewritten,

$$\frac{I_D}{I_{DSS}} = \left[1 - \frac{V_{GS}}{V_P}\right]^2 \qquad \textbf{(10-18)}$$

Now, by substituting convenient values for V_{GS}/V_P into Eq. 10-18 corresponding values of I_D/I_{DSS} are calculated, and these are used to plot the characteristic shown in Fig. 10-45.

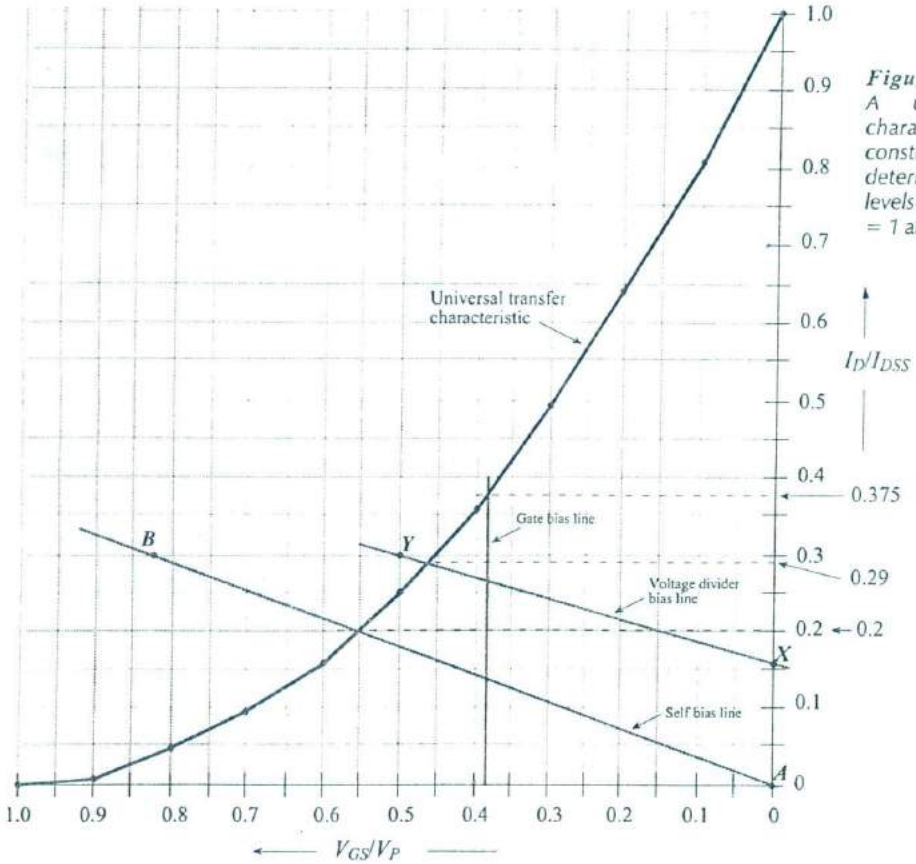


Figure 10-45
A universal transfer characteristic for a FET is constructed using Eq. 9-1 to determine corresponding levels of I_D and V_{GS} with $I_{DSS} = 1$ and $V_P = 1$.

The universal transfer characteristic can be applied to analyze or design a circuit using virtually any *JFET*. This saves the necessity of plotting the transfer characteristics for each device. The specified values of I_{DSS} and V_P must be known for the device. Then, the

characteristic is used in the same way as an actual transfer characteristic, except that V_{GS} levels must be converted to V_{GS}/V_P ratios, and I_D levels must be converted to I_D/I_{DSS} before they can be plotted on the graph. Similarly, readings taken from the graph are converted back to V_{GS} and I_D levels by multiplying them by V_P and I_{DSS}, respectively.

Circuit Analysis

Consider the gate bias circuit analyzed in Ex. 10-3, and reproduced in Fig. 10-46. The gate voltage is given as -2.3 V, and the device used has $I_{DSS(max)} = 8$ mA and $V_{P(max)} = -6$ V. The bias line is drawn vertically on the universal transfer characteristic at,

$$-\frac{V_{GS}}{V_P} = \frac{2.3\text{ V}}{6\text{ V}} = 0.38$$

The gate bias line drawn (at $V_{GS}/V_P = 0.38$) on Fig. 10-45 intersects the universal characteristic at the point where $I_D/I_{DSS} = 0.375$,

giving, $$I_{D(max)} = 0.375\ I_{DSS} = 0.375 \times 8\text{ mA} = 3\text{ mA}$$

This is the $I_{D(max)}$ level determined in Ex. 10-3.

The minimum I_D for a gate bias circuit can be determined from the universal transfer characteristic, by using the $I_{DSS(min)}$ and $V_{P(min)}$ values. Bias lines can also be drawn for analysis of self bias circuits and voltage divider bias circuits. Examples 10-12 and 10-13 demonstrate the analysis procedures.

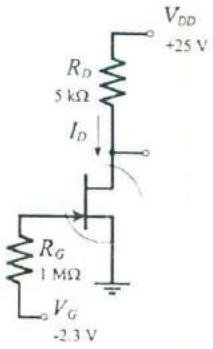


Figure 10-46
The gate bias circuit in Ex. 10-3 can be analyzed by use of the universal transfer characteristic.

Example 10-12

Use the *FET* universal transfer characteristic to determine $I_{D(max)}$ and $V_{DS(min)}$ in the self bias circuit shown in Fig. 10-47.

Solution

From Appendix 1-11, the *2N5457* has, $I_{DSS(max)} = 5$ mA and $V_{P(max)} = 6$ V

when $I_D = 0$, $V_{GS} = V_S = 0$

so, $I_D/I_{DSS} = 0$ and $V_{GS}/V_P = 0$

Plot point *A* on the universal transfer characteristic in Fig. 10-45 at

$$I_D/I_{DSS} = 0 \text{ and } V_{GS}/V_P = 0$$

when $I_D = 1.5$ mA, $V_{GS} = I_D \times R_S = 1.5\text{ mA} \times 3.3\text{ k}\Omega = 4.95$ V

now, $$\frac{I_D}{I_{DSS}} = \frac{1.5\text{ mA}}{5\text{ mA}} = 0.3$$

and, $$\frac{V_{GS}}{V_P} = \frac{4.95\text{ V}}{6\text{ V}} = 0.825$$

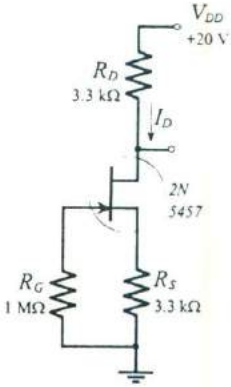


Figure 10-47
Self bias circuit for Ex. 10-12.

Plot point B on the universal transfer characteristic at,

$$I_D/I_{DSS} = 0.3 \text{ and } V_{GS}/V_P = 0.825$$

Draw the self bias line through points A and B,and where the bias line intersects the universal transfer characteristic read,

$$I_D/I_{DSS} = 0.2$$

giving,
$$I_{D(max)} = 0.2\, I_{DSS} = 0.2 \times 5 \text{ mA} = 1 \text{ mA}$$

$$V_{DS(min)} = V_{DD} - I_D(R_D + R_S) = 20 \text{ V} - 1 \text{ mA}(3.3 \text{ k}\Omega + 3.3 \text{ k}\Omega) = 13.4 \text{ V}$$

Example 10-13

Using the *FET* universal transfer characteristic, determine $I_{D(max)}$ and $V_{DS(min)}$ for the voltage divider bias circuit in Fig. 10-48.

Solution

From Appendix 1-11, the *2N5458* has, $I_{DSS(ma)} = 9$ mA and $V_{P(max)} = 7$ V

Eq. 10-7,
$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2} = \frac{22 \text{ V} \times 1 \text{ M}\Omega}{4.7 \text{ M}\Omega + 1 \text{ M}\Omega} = 3.9 \text{ V}$$

when $V_{GS} = 0$, $V_{GS}/V_P = 0$

and, $I_D R_S = V_G$

so,
$$I_D = \frac{V_G}{R_S} = \frac{3.9 \text{ V}}{2.7 \text{ k}\Omega} = 1.4 \text{ mA}$$

and,
$$\frac{I_D}{I_{DSS}} = \frac{1.4 \text{ mA}}{9 \text{ mA}} = 0.16$$

Plot point X on the universal transfer characteristic in Fig. 10-45 at

$$I_D/I_{DSS} = 0.16 \text{ and } V_{GS}/V_P = 0$$

when $V_{GS}/V_P = 0.5$, $V_{GS} = 0.5\, V_P = 0.5 \times (-7 \text{ V}) = -3.5 \text{ V}$

from Eq. 10-6, $I_D R_S = V_G - V_{GS} = 3.9 \text{ V} - (-3.5 \text{ V}) = 7.4 \text{ V}$

so,
$$I_D = \frac{I_D R_S}{R_S} = \frac{7.4 \text{ V}}{2.7 \text{ k}\Omega} = 2.7 \text{ mA}$$

$$\frac{I_D}{I_{DSS}} = \frac{2.7 \text{ mA}}{9 \text{ mA}} = 0.3$$

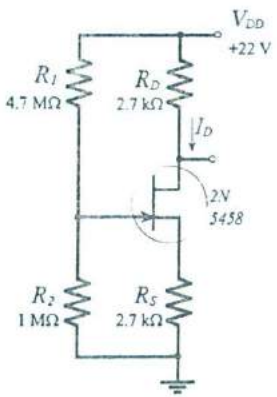


Figure 10-48
Voltage divider bias circuit for Ex. 10-13.

Plot point Y on the universal transfer characteristic at

$$I_D/I_{DSS} = 0.3 \text{ and } V_{GS}/V_P = 0.5$$

Draw the voltage divider bias line through points X and Y,and where the bias line intersects the universal transfer characteristic read,

$$I_D/I_{DSS} = 0.29$$

giving,

$$\begin{aligned} I_D &= 0.29\, I_{DSS} = 0.29 \times 9 \text{ mA} \\ &= 2.61 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 22 \text{ V} - 2.61 \text{ mA}(2.7 \text{ k}\Omega + 2.7 \text{ k}\Omega) \\ &= 7.9 \text{ V} \end{aligned}$$

Practise Problems

10-9.1 The self bias circuit in Fig. 10-47 has its *FET* changed to a *2N5458*. Use the *FET* universal transfer characteristic to determine $I_{D(max)}$ and $V_{DS(min)}$ for the circuit.

10-9.2 Using the *FET* universal transfer characteristic, analyze the circuit in Example 10-6 to determine $V_{DS(min)}$.

10-9.3 A gate bias circuit, as in Fig. 10-46, has a *2N5458*, $V_{DD} = 20$ V, $V_G = -4.5$ V, and $R_D = 4.7$ kΩ. Use the *FET* universal transfer characteristic to determine $I_{D(max)}$ and $V_{DS(min)}$.

10-10 MOSFET Biasing

DE-MOSFET Bias Circuits

DE-MOSFET bias circuits are similar to *JFET* bias circuits. Any of the *FET* bias circuits already discussed can be used to produce a negative V_{GS} level for an *n*-channel *MOSFET*, or a positive V_{GS} for a *p*-channel device. In this case, both devices would be operating in the depletion mode, just like *JFETs*. To operate an *n*-channel *DE-MOSFET* in the enhancement mode, the gate terminal must be made positive with respect to the source. A *p*-channel *DE-MOSFET* in the enhancement mode requires the gate to be negative with respect to the source.

Consider the four *MOSFET* bias circuits shown in Fig. 10-49, and assume that each device has the transfer characteristics in Fig. 10-50. In Fig. 10-49(a) the gate-source bias voltage is zero, so, the bias line is drawn on the transfer characteristics at $V_{GS} = 0$, as shown in Fig 10-50. The *FET* in Fig. 10-49(b) has a positive gate-source bias voltage, consequently, its bias line must be drawn vertically at $V_{GS} = +V_G$. The self bias circuit in Fig. 10-49(c) has its bias line drawn from $I_D = 0$ and $V_{GS} = 0$ at a slope determined by R_S, exactly as for a *JFET* self bias circuit. Similarly, the bias line for the voltage divider bias circuit in Fig. 10-49(d) is drawn from the point where $I_D = 0$ and $V_{GS} = +V_G$ with a slope set by R_S.

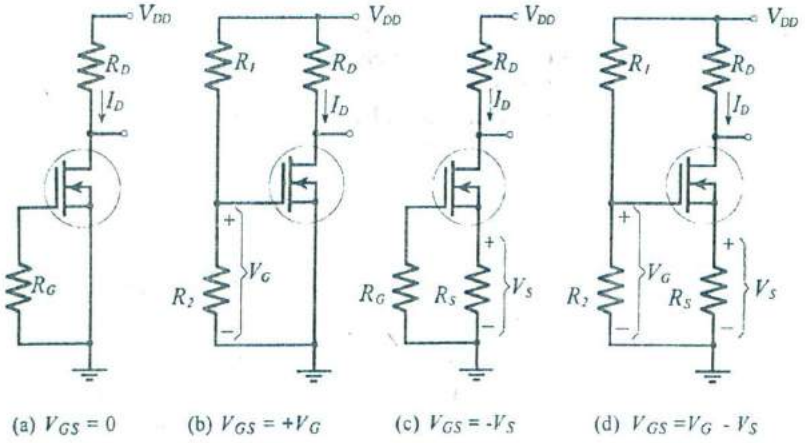


Figure 10-49
DE-MOSFET bias circuits.

As always, $I_{D(min)}$ and $I_{D(max)}$ for any circuit are indicated by the bias line intersections with the maximum and minimum transfer characteristics. Fig. 10-50 shows that in some cases the *FET* is operating in depletion mode, and in other cases it is operating in enhancement mode. Analysis and design procedures for these circuits are essentially the same as for similar *JFET* bias circuits.

MOSFETs can also be used with a plus/minus supply voltage, as discussed in Section 10-8.

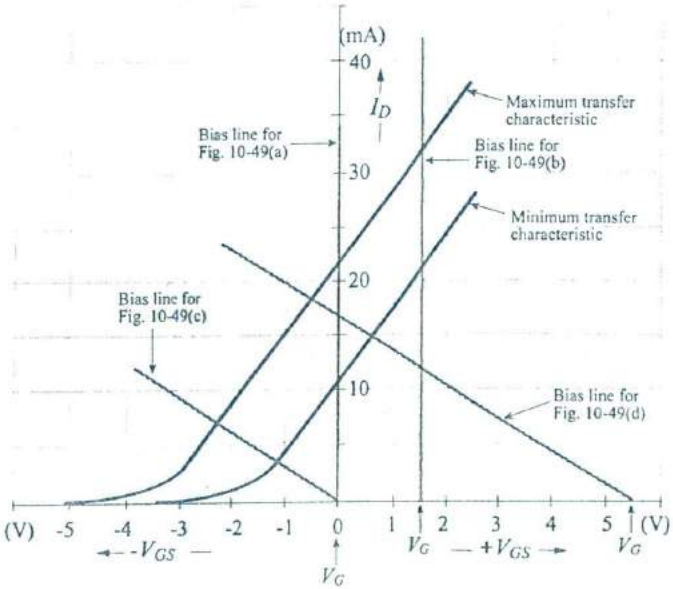


Figure 10-50
DE-MOSFET transfer characteristics and bias lines for the circuits in Fig. 10-49.

E-MOSFET Bias Circuits

Enhancement *MOSFETs* (such as the *VMOS* and *TMOS* devices discussed in Section 9-5) must have positive gate-source bias voltages in the case of *n*-channel devices, and negative V_{GS} levels for a *p*-channel *FET*. Thus, the gate bias circuit in Fig. 10-49(b) and the voltage divider bias circuit in Fig. 10-49(d) are suitable. In each case, the bias line is drawn exactly as already discussed.

Example 10-14

Determine I_D and V_{DS} for the bias circuit in Fig. 10-51, assuming that the device has the transfer characteristic in Fig. 10-52.

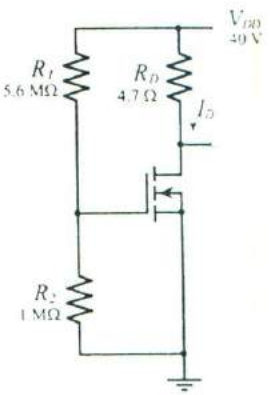


Figure 10-51
E-MOSFET gate bias circuit for Ex. 10-14.

Solution

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2} = \frac{40\ \text{V} \times 1\ \text{M}\Omega}{5.6\ \text{M}\Omega + 1\ \text{M}\Omega}$$

$$= 6.06\ \text{V}$$

Draw the bias line vertically on the transfer characteristic at $V_{GS} = 6.06$ V, (see Fig. 10-52).

From the point where the bias line intersects the transfer characteristic,

$$I_D = 6.2\ \text{A}$$

$$V_{DS} = V_{DD} - I_D R_D = 40\ \text{V} - (6.2\ \text{mA} \times 4.7\ \Omega)$$

$$= 10.9\ \text{V}$$

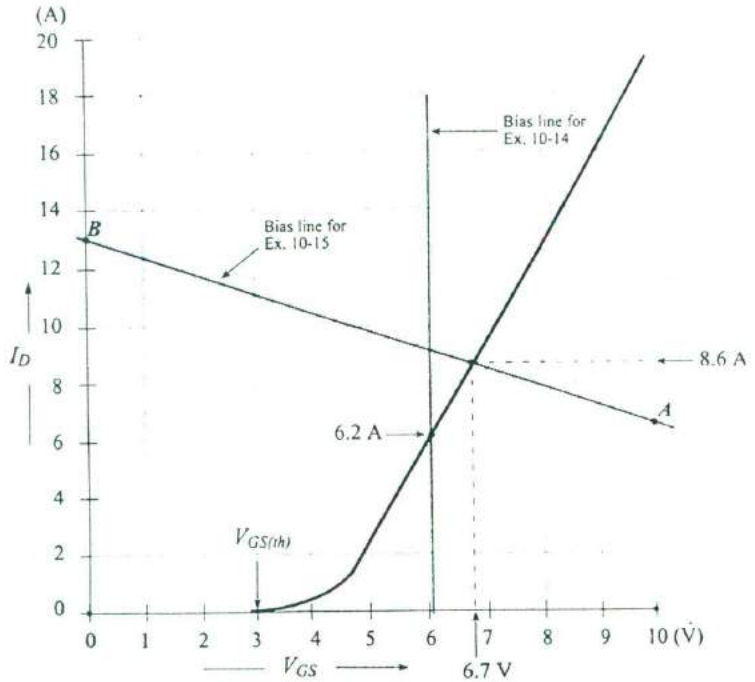


Figure 10-52
E-MOSFET transfer characteristic and bias lines.

The *drain-to-gate* bias circuit shown in Fig. 10-53 is uniquely suitable for an *E-MOSFET*. The *FET* gate is directly connected to the drain terminal via resistor R_G, so that $V_{GS} = V_{DS}$. Also,

$$V_{GS} = V_{DD} - I_D R_D \qquad \textbf{(10-19)}$$

If the drain current is higher than the design level, a higher voltage drop is produced across R_D, and this tends to reduce V_{GS}, and thus reduce I_D back toward the design level. Similarly, a lower than intended I_D level produces a lower $I_D R_D$ voltage drop, and results in a higher V_{GS} that drives I_D back up toward the desired current. Corresponding levels of I_D and V_{GS} can be calculated from Eq. 10-19. These are then plotted on the device transfer characteristics to draw the circuit bias line.

Example 10-15

Analyze the bias circuit in Fig. 10-53 to determine the typical levels of I_D and V_{DS}. Figure 10-52 shows the typical transfer characteristic for the device.

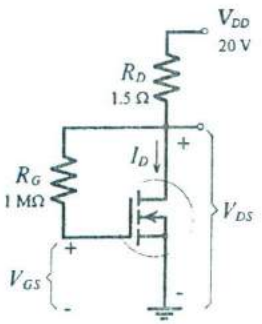


Figure 10-53
E-MOS drain-to-gate bias circuit.

Solution

when $V_{GS} = 10$ V,

from Eq. 10-19, $$I_D = \frac{V_{DD} - V_{GS}}{R_D} = \frac{20\text{ V} - 10\text{ V}}{1.5\ \Omega}$$

$$= 6.7\text{ A}$$

Plot *point A* on Fig. 10-52 at, $V_{GS} = 10$ V and $I_D = 6.7$ A

when $V_{GS} = 0$,

from Eq. 10-19, $$I_D = \frac{V_{DD} - V_{GS}}{R_D} = \frac{20\text{ V} - 0}{1.5\ \Omega}$$

$$= 13\text{ A}$$

Plot *point B* on Fig. 10-52 at, $V_{GS} = 0$ and $I_D = 13$ A

Draw the bias line for $R_D = 1.5\ \Omega$ through *points A* and *B*.

Where the bias line intersects the transfer characteristics,

$$I_D = 8.6\text{ A and } V_{GS} = 6.7\text{ V}$$

$$V_{DS} = V_{GS} = 6.7\text{ V}$$

Practise Problems

10-10.1 The *MOSFET* voltage divider bias circuit in Fig. 10-49(d) has $V_{DD} = 30$ V, $R_1 = 330$ kΩ, $R_2 = 150$ kΩ, and $R_D = R_S = 680\ \Omega$. The *FET* has the transfer characteristics in Fig. 10-50. Analyze the circuit to determine $V_{DS(min)}$ and $V_{DS(max)}$.

10-10.2 A drain-to-gate bias circuit, as in Fig. 10-53, has $V_{DD} = 35$ V, and a *MOSFET* with the transfer characteristics in Fig. 10-52. Calculate an approximate resistance for R_D, to give $V_{DS} = 5$ V.

10-11 Biasing FET Switching Circuits

JFET Switching

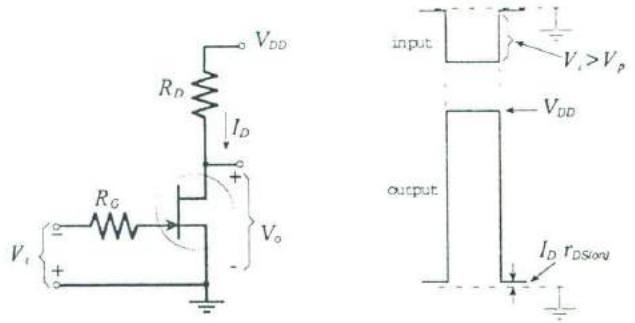
A field effect transistor in a switching circuit is normally in an *off* state with zero drain current, or in an *on* state with a very small drain-source voltage. When the *FET* is *off*, there is a drain-source leakage current so small that it can almost always be neglected. When the device is *on*, the drain-source voltage drop depends on the channel resistance ($r_{DS(on)}$) and the drain current (I_D).

$$V_{DS(on)} = I_D r_{DS(on)} \qquad \textbf{(10-20)}$$

Field effect transistors designed specifically for switching applications have very low channel resistances. For example, the *2N4856* has $r_{DS(on)} = 25\ \Omega$, (see Appendix 1-12). With low I_D levels, $V_{DS(on)}$ can be much smaller than the 0.2 V typical $V_{CE(sat)}$ for a *BJT*. This is an important advantage of a *FET* switch over a *BJT* switch.

Direct-Coupled JFET Switching Circuit

A direct-coupled *JFET* switching circuit is shown in Fig. 10-54(a), and the circuit waveforms are illustrated in Fig. 10-54(b). When $V_i = 0$, the *FET* gate and source voltages are equal, and there is no depletion region penetration into the channel. The output voltage is now $V_o = V_{DS(on)}$, as expressed by Eq. 10-20. When V_i exceeds the *FET* pinch-off voltage, the device is switched *off*, and the output voltage goes to V_{DD}, as illustrated.



(a) Direct-coupled JFET switch (b) Circuit waveforms

Figure 10-54
Direct-coupled JFET switching circuit, and the waveforms of the circuit input and output voltages.

Assuming that $V_{DS(on)}$ is very small, the drain current level is determined from,

$$V_{DD} \approx I_D R_D \qquad \textbf{(10-21)}$$

Equation 10-21 can be used to determine R_D when V_{DD} and I_D are specified, or to calculate I_D when R_D is known. The I_D level can then be employed to determine $V_{DS(on)}$. The lowest drain current that can be used must be very much greater than the specified drain-source leakage current for the device.

To switch the *FET off*, V_i should exceed the maximum pinch-off voltage. However, V_i must not be so large that the drain-gate voltage ($V_{DG} = V_{DD} + V_i$) approaches the breakdown voltage. A rule-of-thumb is to select the input voltage 1 V larger than $V_{P(max)}$.

$$V_i = -(V_{P(max)} + 1\ V) \qquad (10\text{-}22)$$

The gate resistor (R_G) in the circuit in Fig. 10-54 is provided solely to limit any gate current in the event that the gate-source junctions become forward biased. The circuit might operate satisfactorily with R_G selected as 1 MΩ, however, high-value resistors can slow the switching speed of the circuit, so, quite small resistance values are often used for R_G.

Example 10-16

Design the *JFET* switching circuit in Fig. 10-54 to have $V_{DS(on)}$ not greater than 200 mV. A *2N4856 FET* is to be used with a 12 V supply.

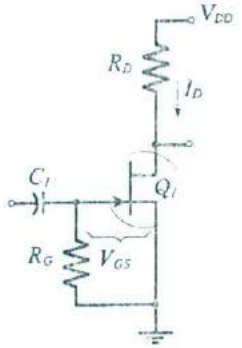
Solution

From Appendix 1-12, $r_{DS(on)} = 25\ \Omega$ and $V_{GS(off)} = 10$ V (max)

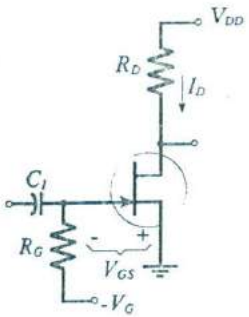
From Eq. 10-20,
$$I_D = \frac{V_{DS(on)}}{r_{DS(on)}} = \frac{200\ \text{mV}}{25\ \Omega}$$
$$= 8\ \text{mA}$$

From Eq. 10-21,
$$R_D \approx \frac{V_{DD}}{I_D} = \frac{12\ \text{V}}{8\ \text{mA}}$$
$$= 1.5\ \text{k}\Omega \text{ (standard value)}$$

Eq. 10-22,
$$V_i = -(V_P + 1\ \text{V}) = -(10\ \text{V} + 1\ \text{V})$$
$$= -11\ \text{V}$$



(a) Normally-*on* circuit



(b) Normally-*off* circuit

Figure 10-55
Normally-on and normally-off capacitor-coupled JFET switching circuits.

Capacitor-Coupled JFET Switching Circuits

Two capacitor-coupled *JFET* switching circuits are shown in Fig. 10-55. The *FET* in Fig. 10-55(a) is normally-*on* because it has $V_{GS} = 0$, and the device in Fig. 10-55(b) is normally-*off* with $-V_{GS}$ greater than the pinch-off voltage. In both circuits, the *FET* is switched *on* or *off* by a capacitor-coupled input pulse. The design procedure for these circuits uses the equations already discussed for the direct-coupled *JFET* switching circuit.

MOSFET Switching

Figure 10-56 shows two capacitor-coupled *MOSFET* switching circuits. In Fig. 10-56(a), the *FET* is biased *off* because $V_{GS} = 0$. A positive-going input signal is required to turn the device *on*. The *FET* in Fig. 10-56(b) is biased *on* by the positive V_{GS} provided by R_1 and R_2. In this case, a negative-going input voltage must be applied to turn the *FET off*. Equations 10-20 and 10-21 can be applied to these circuits to calculate I_D and $V_{DS(on)}$. To turn the

device *on* to a desired level of drain current, the transfer characteristics can be employed if they are available. Alternatively, Eq 9-5 can be used to estimate the required gate-source bias voltage, as explained in Section 9-5. To ensure that the *FET* is *off*, the gate-source voltage must be driven below the minimum threshold voltage for the device.

Example 10-17

The *MOSFET* in the switching circuit in Fig. 10-56(b) is to be biased *on* to have the smallest possible $V_{DS(on)}$. Determine suitable resistances for R_1 and R_2, and calculate $V_{DS(on)}$. The device has the transfer characteristics shown in Fig. 10-52, and its drain-source *on* resistance is 0.25 Ω.

Solution

From Eq. 10-21, $$I_D \approx \frac{V_{DD}}{R_D} = \frac{50\text{ V}}{10\ \Omega}$$

$$= 5\text{ A}$$

Referring to the transfer characteristics in Fig. 10-52,

at $I_D = 5$ A, $V_{GS} \approx 5.7$ V

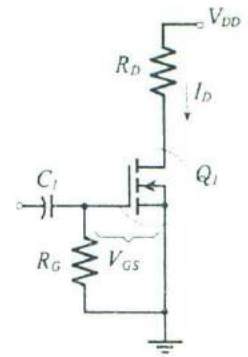
Select $R_2 = 1\ \text{M}\Omega$

From Eq. 10-15, $$R_1 = \frac{(V_D - V_{GS}) \times R_2}{V_G} = \frac{(50\text{ V} - 5.7\text{ V}) \times 1\ \text{M}\Omega}{5.7\text{ V}}$$

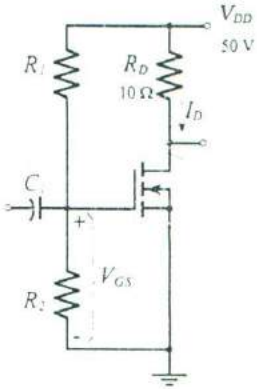
$= 7.7\ \text{M}\Omega$ (use 6.8 MΩ to make $V_{GS} > 5.7$ V to ensure that the *FET* is biased *on*)

Eq. 10-20, $V_{DS(on)} = I_D r_{DS(on)} = 5\text{ A} \times 0.25\ \Omega$

$= 1.25$ V



(a) Normally-*off* circuit



(b) Normally-*on* circuit

Figure 10-56
MOSFET normally-on and normally-off capacitor-coupled switching circuits.

Practise Problems

10-11.1 A normally-*off* *JFET* switching circuit, as in Fig. 10-55(b), is to use a *2N4861 FET* with a 30 V supply, and is to have $I_{D(max)} = 10$ mA. Calculate R_D, $V_{DS(on)}$, and the required V_G level.

10-11.2 The normally-*off* *MOSFET* switching circuit in Fig. 10-56(a) is to be employed to pass 15 A through a 3 Ω resistor. The device used has the transfer characteristics shown in Fig. 10-52, and $r_{DS(on)} = 0.2\ \Omega$. Calculate approximate levels for the supply and input voltages.

Chapter-10 Review Questions

Section 10-1

10-1 Identify the components that constitute the *dc* load in a *FET* bias circuit. Explain the procedure for drawing the *dc* load line on the *FET* drain characteristics.

10-2 Explain the selection of a Q point on a *FET dc* Load line, and discuss the limitations on the output voltage swing.

Section 10-2

10-3 Sketch a gate bias circuit using an *n*-channel *JFET*. Identify the polarities of V_{DD}, V_{DS}, V_G, and V_{GS}. Also show the I_D direction. Briefly explain the circuit operation.

10-4 Repeat Question 10-3 for a gate bias circuit using a *p*-channel *JFET*.

10-5 Write equations for $V_{DS(max)}$ and $V_{DS(min)}$ for a *JFET* gate bias circuit.

10-6 State a typical maximum resistance for gate resistor R_G in a gate bias circuit. Briefly explain.

10-7 Explain why the device maximum and minimum transfer characteristics should be used in *FET* bias circuit analysis.

Section 10-3

10-8 Sketch a self bias circuit using an *n*-channel *JFET*. Identify the polarities of V_{DD}, V_{DS}, V_S, V_G, and V_{GS}. Briefly explain the circuit operation.

10-9 Repeat Question 10-8 for a self bias circuit using a *p*-channel *JFET*.

10-10 Write equations for $V_{DS(max)}$ and $V_{DS(min)}$ for a *FET* self bias circuit. Also, write the equation used for drawing the circuit bias line on the transfer characteristics.

Section 10-4

10-11 Sketch a voltage divider bias circuit using an *n*-channel *JFET*. Identify the polarities of V_{DD}, V_{DS}, V_S, V_G, and V_{GS}. Briefly explain the circuit operation.

10-12 Repeat Question 10-11 for a voltage divider bias circuit using a *p*-channel *JFET*.

10-13 Write equations for $V_{DS(max)}$ and $V_{DS(min)}$ for a *FET* voltage divider bias circuit. Also, write the equation used for drawing the circuit bias line on the transfer characteristics.

Section 10-5

10-14 Compare the performance of the three basic *JFET* bias circuits in terms of the differences between $I_{D(max)}$ and $I_{D(min)}$ in each circuit and the predictability of circuit Q-points.

Section 10-6

10-15 Briefly explain the procedure for testing a *FET* bias circuit. List common errors made when testing bias circuits.

10-16 List possible errors in a *JFET* bias circuit with $V_D \approx V_{DD}$ in the case of (a) gate bias, (b) self bias, (c) voltage divider bias.

10-17 List possible errors in a *JFET* bias circuit with $V_{DS} \approx 0$ in the case of (a) gate bias, (b) self bias, (c) voltage divider bias.

Section 10-7

10-18 Write the equation for calculating R_D in a gate bias circuit.

10-19 Explain why the *FET* maximum drain characteristics should be used when designing a *JFET* bias circuit.

10-20 Write equation for calculating R_D and R_S in a *JFET* self bias circuit.

10-21 Write equation for determining R_D, R_S, R_1 and R_2 in a *JFET* voltage divider bias circuit.

Section 10-8

10-22 Sketch an *n*-channel *JFET* voltage divider bias circuit using a plus-minus supply. Identify the polarities of V_{DD}, V_{DS}, V_S, V_G, and V_{GS}. Briefly explain the circuit operation.

10-23 Repeat Question 10-22 for a similar circuit using a *p*-channel *JFET*.

10-24 Sketch an *n*-channel *JFET* drain feedback bias circuit. Identify all voltage polarities, and explain the circuit operation.

10-25 Repeat Question 10-24 for a drain feedback bias circuit using a *p*-channel *JFET*.

10-26 Sketch an *n*-channel *JFET* constant current bias circuit using voltage divider bias at the gate. Identify all voltage polarities and current directions, and explain the circuit operation.

10-27 Repeat Question 10-26 for a constant current bias circuit using a *p*-channel *JFET*.

10-28 Sketch an *n*-channel *JFET* constant current bias circuit using a plus-minus supply. Identify all voltage polarities and current directions, and explain the circuit operation.

10-29 Repeat Question 10-28 for a constant current bias circuit using a *p*-channel *JFET*.

Section 10-9

10-30 Write the equation used for constructing a *JFET* universal transfer characteristic. Briefly explain the universal transfer characteristic and its application.

Section 10-10

10-31 Sketch *n*-channel *DE-MOSFET* gate bias circuits using (a) $V_{GS} = 0$, (b) $V_{GS} = +V_G$. Identify all voltage polarities and current directions, explain the operation of each circuit.

10-32 Draw the diagram of a self bias circuit using an *n*-channel *DE-MOSFET*. Identify all voltage polarities and current

directions, and explain the circuit operation.

10-33 Draw a voltage divider bias circuit using an *n*-channel *DE-MOSFET*. Identify all voltage polarities and current directions, and explain the circuit operation.

10-34 Sketch approximate maximum and minimum transfer characteristics for a *DE-MOSFET*. On the transfer characteristics, draw typical bias lines for the circuits in Questions 10-31 through 10-33. Briefly explain.

10-35 Draw a circuit diagram for a drain-to-gate bias circuit using an *n*-channel *E-MOSFET*. Explain the circuit operation.

10-36 Draw a circuit diagram for a drain-to-gate bias circuit using a *p*-channel *E-MOSFET*. Explain.

Section 10-11

10-37 Sketch a circuit diagram for a direct-coupled switching circuit using an *n*-channel *JFET*. Sketch input and output waveforms, and explain the circuit operation.

10-38 Draw circuit diagrams for normally-*on* and normally-*off* capacitor-coupled *JFET* switching circuits. Explain the operation of each circuit.

10-39 Sketch circuit diagrams for normally-*on* and normally-*off* capacitor-coupled switching circuits using *E-MOSFETs*. Explain the operation of each circuit.

Chapter-10 Problems

Section 10-1

10-1 The circuit in Fig. 10-57 has a *JFET* with the characteristics in Fig. 10-58. Draw the *dc* load line for the circuit, and select a suitable gate voltage to give the maximum possible symmetrical output voltage swing.

10-2 Estimate the maximum possible symmetrical output voltage swing for the circuit in Problem 10-1 when $V_G = -2$ V.

10-3 A *JFET* circuit like the one in Fig. 10-57 is to have $V_{DS} = 10$ V and $I_D = 2$ mA. If $V_{DD} = 18$ V, draw the *dc* load line on the drain characteristics in Fig. 10-58, and determine the required resistance for R_D.

10-4 Using the drain characteristics in Fig. 10-58, draw the *dc* load line for the circuit in Fig. 10-59.

10-5 Determine the I_D and V_{DS} levels in the circuit in Problem 10-4 if the gate-source voltage is -1.5 V.

10-6 A *JFET* circuit as in Fig. 10-57 has $R_D = 4.7$ kΩ. The bias conditions are to be $V_{DS} = 8$ V and $I_D = 1.5$ mA. Draw the *dc* load line on the drain characteristics in Fig. 10-58, and determine a suitable supply voltage.

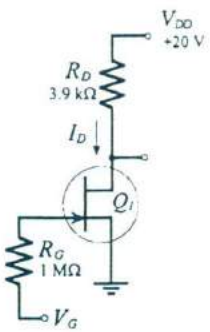


Figure 10-57

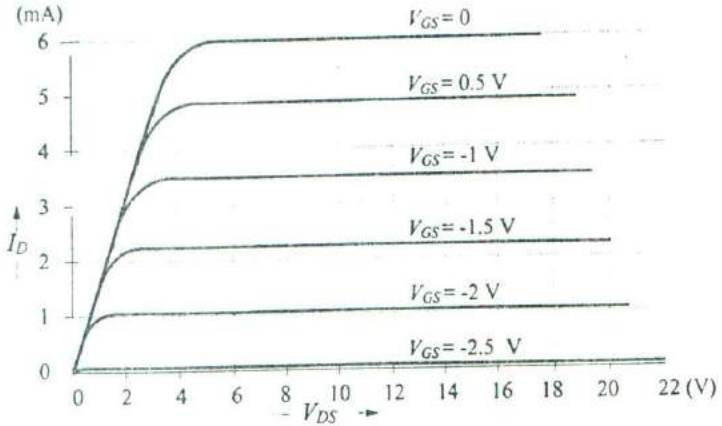


Figure 10-58

Section 10-2

10-7 The gate bias circuit in Fig. 10-60 has a *JFET* with the transfer characteristics in Fig. 10-61. Analyze the circuit to calculate $V_{DS(max)}$ and $V_{DS(min)}$.

10-8 Repeat Problem 10-7 using Eq. 9-1 instead of the transfer characteristics.

10-9 The *JFET* used in a gate bias circuit has the transfer characteristics in Fig. 10-61. If R_D = 2.2 kΩ, V_{DD} = 20 V, and V_G = -2 V, draw the bias line and calculate $V_{DS(max)}$ and $V_{DS(min)}$.

10-10 Repeat Problem 10-9 using Eq. 10-8 instead of the transfer characteristics.

10-11 Analyze the circuit in Fig. 10-62 to determine $V_{DS(max)}$ and $V_{DS(min)}$.

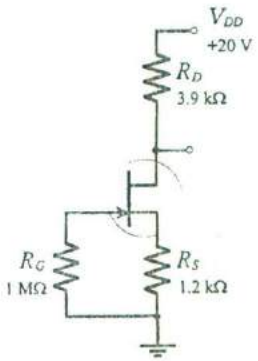


Figure 10-59

Section 10-3

10-12 Determine the maximum and minimum levels of V_{DS} for the *JFET* self bias circuit in Fig. 10-63. Assume that the device has the transfer characteristics in Fig. 10-61.

10-13 A *JFET* self bias circuit (as in Fig. 10-63) has V_{DD} = 30 V, R_D = 4.7 kΩ, R_S = 820 Ω, and R_G = 1 MΩ. If the *FET* is a *2N5457* calculate the minimum level of V_{DS}.

10-14 Recalculate $V_{DS(min)}$ for the circuit in Problem 10-13 when the device is changed to a *2N5458*.

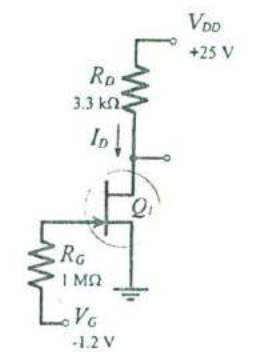


Figure 10-60

Section 10-4

10-15 Assuming that the *JFET* in the voltage divider bias circuit in Fig. 10-64 has the transfer characteristics in Fig. 10-61, determine the maximum and minimum V_{DS} levels.

10-16 A *JFET* voltage divider bias circuit (as in Fig. 10-64) has V_{DD} = 20 V, $R_D = R_S$ = 2.7 kΩ, R_1 = 7.7 MΩ, and R_2 = 1 MΩ. Using

the *JFET* transfer characteristics in Fig. 10-61, determine the maximum and minimum V_{DS} levels.

10-17 A *JFET* with the transfer characteristics in Fig. 10-61 is connected in a voltage divider bias circuit with V_{DD} = 22 V. The circuit components are: $R_D = R_S$ = 3.9 kΩ, R_1 = 7.8 MΩ, and R_2 = 1 MΩ. Calculate $V_{DS(max)}$ and $V_{DS(min)}$.

10-18 A *2N5457 JFET* is used in a voltage divider bias circuit with V_{DD} = 20 V. The circuit components are: R_D = 4.7 kΩ, R_S = 3.9 kΩ, R_1 = 1.2 MΩ, and R_2 = 300 kΩ. Determine $V_{DS(min)}$.

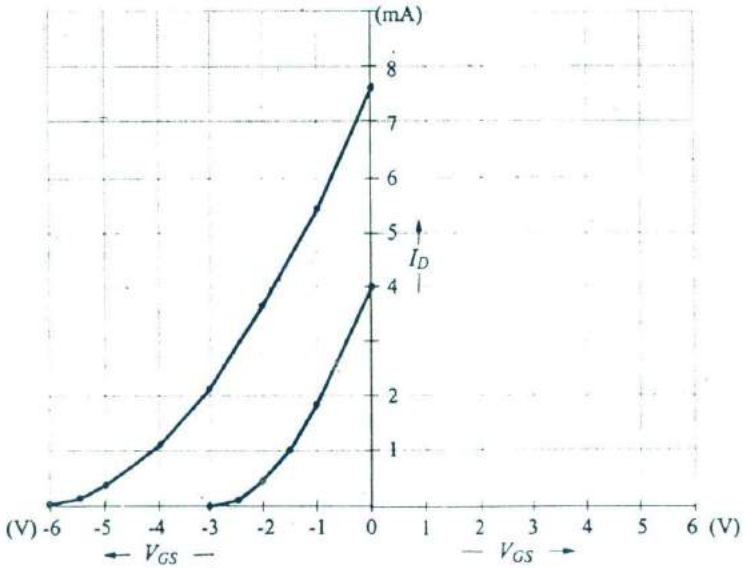


Figure 10-61

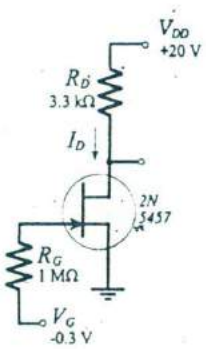


Figure 10-62

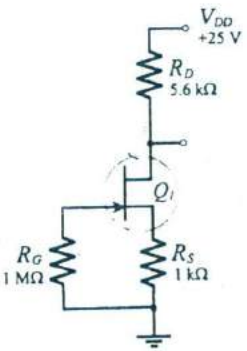


Figure 10-63

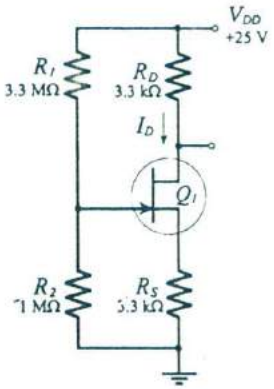


Figure 10-64

Section 10-7

10-19 A *JFET* gate bias circuit is to have $I_{D(max)}$ = 5.5 mA and $V_{DS(min)}$ = 7 V. The supply voltage is 25 V, and the *FET* transfer characteristics are shown in Fig. 10-61. Determine the required bias voltage and suitable resistor values.

10-20 Design a gate bias circuit using a *2N5457 JFET*. The circuit is to have $I_{D(max)}$ = 4.5 mA and $V_{DS(min)}$ = 7.5 V, and the supply voltage is to be 20 V.

10-21 A *JFET* self bias circuit is to have V_{DD} = 25 V, $I_{D(max)}$ = 2.5 mA, and $V_{DS(min)}$ = 7 V. Design the circuit using the *FET* transfer characteristics shown in Fig. 10-61.

10-22 Design a self bias circuit using a *2N5457 JFET* with V_{DD} = 20 V, $I_{D(max)}$ = 2 mA, and $V_{DS(min)}$ = 7.5 V.

10-23 A *JFET* voltage divider bias circuit is to have V_{DD} = 25 V, $I_{D(max)}$ = 2.5 mA, and $V_{DS(min)}$ = 7 V. Design the circuit using the device transfer characteristics shown in Fig. 10-61.

10-24 Design a *JFET* voltage divider bias circuit to have V_{DD} = 20 V, $I_{D(max)}$ = 2 mA, and $V_{DS(min)}$ = 7.5 V. Use a *2N5457 JFET*.

10-25 A *JFET* voltage divider bias circuit is to have V_{DD} = 22 V, $I_{D(max)}$ = 1.5 mA, and $V_{DS(min)}$ = 9 V. Design the circuit using the device transfer characteristics in Fig. 10-61.

10-26 A *JFET* with the device transfer characteristics in Fig. 10-61 is used in a voltage divider bias circuit with V_{DD} = 20 V and R_D = 4.7 kΩ. Determine suitable values for R_1, R_2, and R_S to maintain I_D within the limits of 1 mA to 1.3 mA.

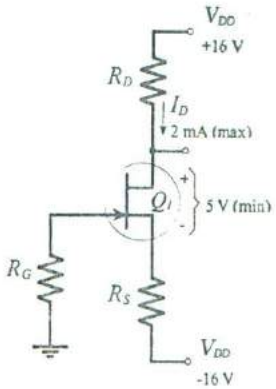


Figure 10-65

Section 10-8

10-27 Design the circuit shown in Fig. 10-65 using the transfer characteristics in Fig. 10-61.

10-28 Analyze the circuit designed for Problem 10-27 to determine the levels of $V_{DS(max)}$ and $V_{DS(min)}$.

10-29 A *JFET* circuit like the one in Fig. 10-65 is to have the following voltage and current levels: V_{DD} = 20 V, V_{SS} = -10 V, $I_{D(max)}$ = 1.5 mA, and $V_{DS(min)}$ = 8 V. Design the circuit to use a *2N5458 JFET*. Select suitable standard-value resistors.

10-30 Analyze the circuit designed for Problem 10-29 to determine $V_{DS(min)}$.

10-31 Design the circuit shown in Fig. 10-66 using the *JFET* transfer characteristics in Fig. 10-37. Select suitable standard-value resistors.

10-32 Analyze the circuit designed for Problem 10-31 to determine $V_{DS(max)}$ and $V_{DS(min)}$.

10-33 A *JFET* circuit like the one in Fig. 10-66 is to have the following voltage and current levels: V_{DD} = 22 V, $I_{D(max)}$ = 1.5 mA, and $V_{DS(min)}$ = 9 V. Design the circuit to use a *JFET* with

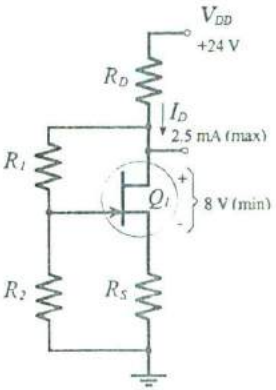


Figure 10-66

the transfer characteristics in Fig. 10-61. Select suitable standard-value resistors.

10-34 Analyze the circuit designed for Problem 10-33 to determine the maximum and minimum levels of V_{DS}.

10-35 Design the *JFET* circuit shown in Fig. 10-67 using the transfer characteristics in Fig. 10-61. Select suitable standard-value resistors.

10-36 Analyze the circuit designed for Problem 10-35 to determine all voltage and current levels.

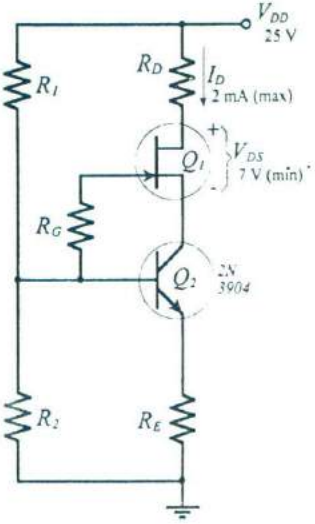


Figure 10-67

Section 10-9

10-37 Use the *FET* universal transfer characteristic in Fig. 10-45 to determine $V_{DS(min)}$ for the gate bias circuit in Fig. 10-62.

10-38 Use the *FET* universal transfer characteristic in Fig. 10-45, to determine $V_{DS(min)}$ for the circuit in Fig. 10-63. The actual device transfer characteristics are shown in Fig. 10-61.

10-39 Assuming that a *2N5458 JFET* is connected in the voltage divider bias circuit in Fig. 10-64, determine $V_{DS(min)}$ using the *FET* universal transfer characteristic in Fig. 10-45.

Section 10-10

10-40 The *MOSFET* in the gate bias circuit in Fig. 10-68 has the transfer characteristics in Fig. 10-69. Draw the bias line and calculate $V_{DS(max)}$ and $V_{DS(min)}$.

10-41 Design the *MOSFET* gate bias circuit shown in Fig. 10-70 using the transfer characteristics in Fig. 10-69. Select suitable standard-value resistors.

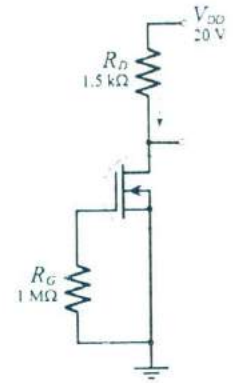


Figure 10-68

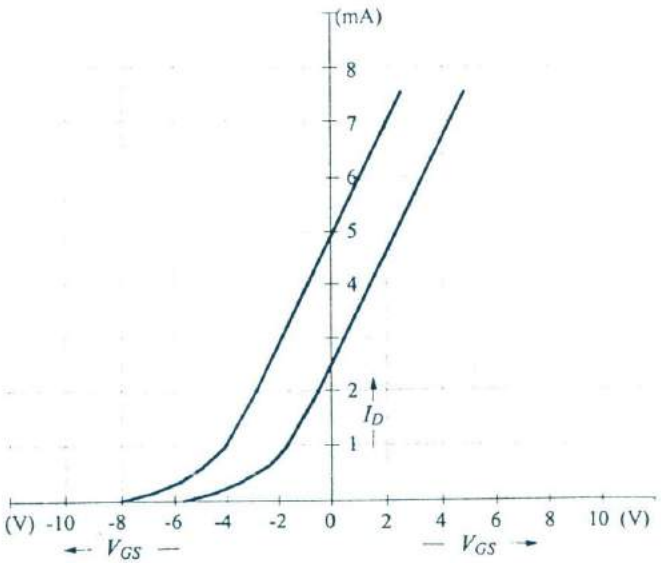


Figure 10-69

10-42 Analyze the circuit designed for Problem 10-41 to determine all voltage and current maximum and minimum levels.

10-43 Design the *MOSFET* voltage divider bias circuit shown in Fig. 10-71 using the transfer characteristics in Fig. 10-69. Select suitable standard-value resistors.

10-44 Analyze the circuit designed for Problem 10-43 to determine all voltage and current maximum and minimum levels.

10-45 Determine suitable resistors for the *MOSFET* drain-to-gate bias circuit in Fig. 10-72 using the transfer characteristics in Fig. 10-52. Calculate the drain-source voltage.

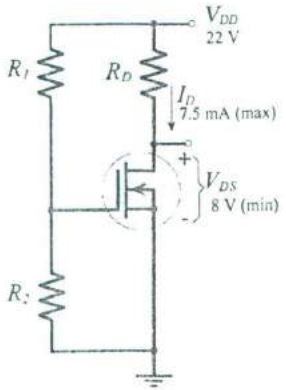


Figure 10-70

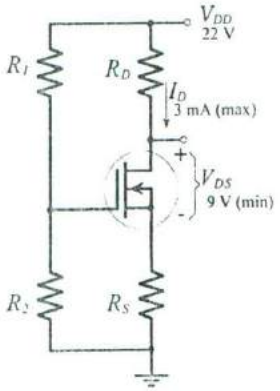


Figure 10-71

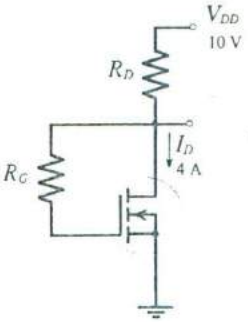


Figure 10-72

Section 10-11

10-46 Calculate V_{DS} levels for the direct-coupled *JFET* switching circuit in Fig. 10-73 when the *FET* is *off*, and when it is *on*. Appendix 1-12 gives the data sheet for the *2N4861*.

10-47 A direct-coupled *JFET* switching circuit (as in Fig. 10-73) is to be designed to use a *2N4861* and V_{DD} = 18 V. V_{DS} is not to exceed 100 mV when the device is *on*. Determine suitable resistor values and a suitable input voltage amplitude.

10-48 The *JFET* switching circuit in Fig. 10-74 is to have $V_{DS} \approx 50$ mV when the device is *on*. Select a *FET* from the *2N4856* through *2N4861* range, calculate appropriate resistor values, and determine a suitable input voltage amplitude.

10-49 The switching circuit in Fig. 10-75 is required to pass 5 A through a 5 Ω resistance. Calculate a suitable $r_{DS(on)}$ value for the device. Also, determine a suitable input voltage amplitude using the transfer characteristic in Fig. 10-52.

10-50 The *MOSFET* in the switching circuit in Fig. 10-76 has the transfer characteristic in Fig. 10-52 and $r_{DS(on)}$ = 0.2 Ω. Calculate the required drain current and suitable values for resistors R_1 and R_2.

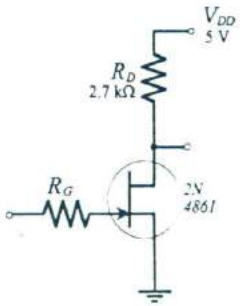


Figure 10-73

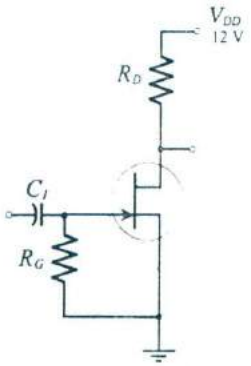


Figure 10-74

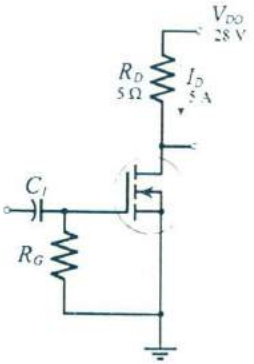


Figure 10-75

Practise Problem Answers

10-1.1 8 V
10-1.2 ±5 V
10-2.1 8.4 V, 17.6
10-2.2 12.7 V
10-3.1 8.8 V, 16.1 V
10-4.1 14 V, 18.7 V
10-7.1 -1.7 V, 1 MΩ, 4.7 kΩ
10-7.2 1 MΩ, 3.9 kΩ, 1.5 kΩ
10-7.3 4.7 MΩ, 1 MΩ, 5.6 kΩ, 5.6 kΩ
10-8.1 1 MΩ, 3.3 kΩ, 8.3 kΩ
10-8.2 1 MΩ, 10 kΩ, 5.6 kΩ
10-8.3 (2.2 MΩ + 220 kΩ), 1 MΩ, 2.7 kΩ, 2.7 kΩ
10-9.1 12.4 V
10-9.2 10 V
10-9.3 14.1 V
10-10.1 9.6 V, 12.3 V
10-10.2 12 Ω
10-11.1 3.3 kΩ, 0.6 V, -5 V
10-11.3 48 V, 8.6 V

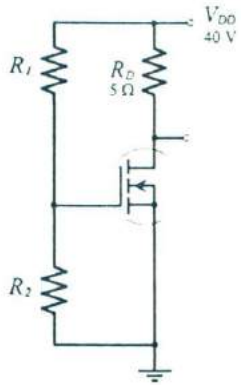
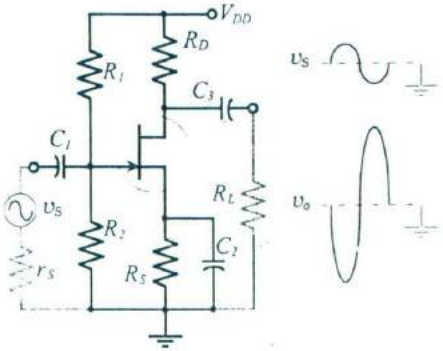


Figure 10-76

Chapter 11

AC Analysis of FET Circuits



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Objectives

You will be able to:

1. *Explain the need for coupling and bypass capacitors in FET circuits, and draw ac equivalent circuits for circuits containing capacitors.*
2. *Draw ac load lines for basic FET circuits.*
3. *Sketch ac equivalent circuits for various FET common-source, common-drain, and common-gate circuits.*
4. *Analyze various CS, CD, and CG FET circuits to determine input resistance, output resistance, and voltage gain.*
5. *Compare the performance of CS, CD, and CG circuits, and compare FET and BJT circuits.*
6. *Calculate the cutoff frequency for FET circuits.*

Introduction

Like *BJT* circuits, *FET* amplifiers have *ac* signals capacitor-coupled to the circuit input, and loads capacitor-coupled to the output terminals. Bypass capacitors are also employed both in *FET* and *BJT* circuits to ensure maximum *ac* voltage gains. Because of the *ac*-coupled load and the *ac* bypassed components, the *ac* load for a given circuit is different from the *dc* load, consequently, the *ac* load line is different from the *dc* load line.

There are three basic *FET* circuit configurations; common-source, common-drain, and common-gate. These are similar to the *BJT* common-emitter, common-collector, and common-base circuits, respectively. The common-source circuit is capable of voltage amplification, and it has a high input impedance. The common-drain circuit is a buffer amplifier, with a voltage gain of approximately one, high input impedance, and low output impedance. The common-gate circuit has voltage gain, low input impedance, and good high-frequency performance.

11-1 Coupling, Bypassing, and AC Load Lines

Coupling Capacitors

This subject is treated for *BJT* circuits in Section 6-1, and the discussion there applies equally to *FET* circuits. As explained, coupling capacitors are required at a circuit input to couple a signal source to the circuit without affecting the bias conditions. Similarly, loads are capacitor-coupled to the circuit output to avoid the change in bias conditions produced by direct coupling. Input and output coupling capacitors (C_1 and C_3) are shown in the *FET* circuit in Fig. 11-1.

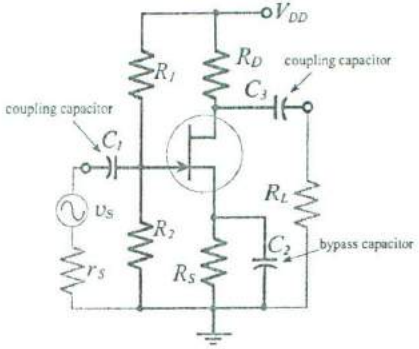


Figure 11-1
FET circuit with coupling and bypass capacitors.

Bypassing Capacitors

Bypass capacitors are also just as necessary in *FET* circuits as in *BJT* circuits. Bypass capacitor C_2 in Fig. 11-1 provides an *ac* short-circuit across resistor R_S. As will be shown, if C_2 is not present R_S substantially reduces the *ac* voltage gain of the circuit.

Figure 11-2 illustrates another situation where a bypassing capacitor is required. The *MOSFET* drain-to-gate bias circuit shown would have its voltage gain reduced by feedback from the drain to the gate via R_G (*ac* degeneration) if capacitor C_2 were not present. Splitting R_G into two equal resistors and *ac* shorting the junction to ground via C_2 eliminates the feedback.

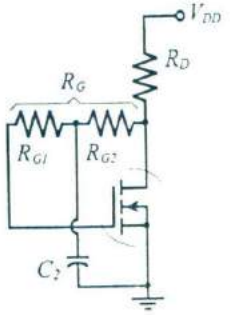


Figure 11-2
MOSFET circuit with bypass capacitor to eliminate ac degeneration.

AC Load Lines

Once again, this is a subject that applies equally to *BJT* and *FET* circuits, (see Section 6-2). The *dc* load for the *FET* circuit in Fig. 11-1 is $(R_D + R_S)$. With R_S *ac* bypassed and R_L absent, the *ac* load is R_D. With the capacitor-coupled load present in Fig. 11-1, the *ac* load is $R_D \| R_L$. The *dc* load line is drawn in the usual way, and the *Q*-point is marked, then the *ac* load line is drawn through the *Q*-point, as shown in Fig. 11-3.

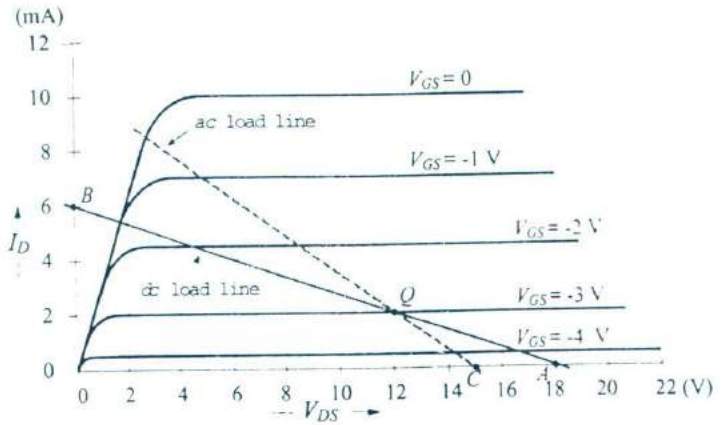


Figure 11-3
FET circuit dc and ac load lines.

Example 11-1

Draw the *dc* and *ac* load lines for the transistor circuit in Fig. 11-4 using the transistor common-emitter characteristics in Fig. 11-3, and identifying the *Q*-point current as $I_D = 2$ mA.

Solution

dc load line,

$$R_{L(dc)} = R_D + R_S = 1.5\ \text{k}\Omega + 1.5\ \text{k}\Omega$$
$$= 3\ \text{k}\Omega$$

The equation for V_{DS} is, $V_{DS} = V_{DD} - I_D (R_D + R_S)$

When $I_D = 0$, $V_{DS} = V_{DD} = 18\ \text{V}$

Plot point A at, $I_D = 0$ *and* $V_{DS} = 18\ \text{V}$

When $V_{DS} = 0$, $I_D = \dfrac{V_{DD}}{R_D + R_S} = \dfrac{18\ \text{V}}{3\ \text{k}\Omega}$

$$= 6\ \text{mA}$$

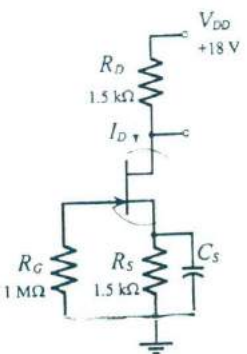


Figure 11-4
Circuit for Ex. 11-1.

Plot point B at, $I_D = 6$ mA and $V_{DS} = 0$
Draw the dc load line through points A and B.
Mark the Q-point on the dc load line at $I_D = 2$ mA.

ac load line,

$$R_{l(ac)} = R_D = 1.5\ \text{k}\Omega \text{ (when } R_S \text{ is bypassed)}$$

When I_D changes by $\Delta I_D = 2$ mA,

$$\Delta V_{DS} = \Delta I_D \times R_D = 2\ \text{mA} \times 1.5\ \text{k}\Omega$$
$$= 3\ \text{V}$$

Plot point C at, $\Delta I_D = 2$ mA and $\Delta V_{DS} = 3$ V from the Q point.
Draw the ac load line through points C and Q.

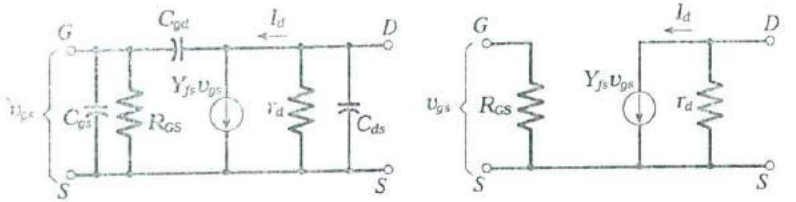
Practise Problems

11-1.1 The circuit in Fig. 11-1 has $R_D = 2.2\ \text{k}\Omega$, $R_S = 1.8\ \text{k}\Omega$, $R_l = 15\ \text{k}\Omega$, and $V_{DD} = 20$ V. Determine the *dc* and ac load resistances, and draw both load lines on the characteristic in Fig. 11-3. Assume that the Q-point drain current is 2.5 mA.

11-2 FET Models and Parameters

FET Equivalent Circuit

The complete equivalent circuit for a field effect transistor is shown in Fig. 11-5(a). It is seen that the source terminal is common to both input and out, so this is a *common-source* equivalent circuit. Resistor R_{GS} between the gate and source terminals is the resistance of the reverse-biased gate-source junction, and C_{gs} is the junction capacitance. So, a signal applied to the input sees R_{GS} in parallel with C_{gs}.



(a) Complete equivalent circuit (b) Low- and medium-frequency equivalent circuit

Figure 11-5
The complete equivalent circuit for a FET includes capacitances between terminals. For low- and medium-frequency operations, the capacitances are omitted.

The output stage of the equivalent circuit is represented as a current source ($Y_{fs}\, v_{gs}$) supplying current to the drain resistance (r_d). Y_{fs} is the forward transfer admittance for the *FET*, and v_{gs} is the *ac* signal voltage developed across the gate-source terminals, so the *ac* drain current is ($Y_{fs}\, v_{gs}$). The drain-source capacitance (C_{ds}) appears in parallel with r_d, and the gate-drain capacitance (C_{gd}) is shown connected between the input and output stages.

For low- and medium-frequency operations the capacitances can be neglected, and the equivalent circuit is then as shown in Fig. 11-5(b). This is the *FET model* (or equivalent circuit) normally used in *ac* circuit analysis.

Equivalent Circuit Parameters

The parameters used in the equivalent circuit are discussed in Section 9-3. As explained, R_{GS} is a junction reverse resistance with a $10^9\ \Omega$ typical value for a *JFET*. Because its resistance is so high, R_{GS} is often regarded as an open circuit. Instead of R_{GS} being listed on a device data sheet, the gate-source reverse current is usually specified, and a value for R_{GS} can be calculated from this quantity.

The forward transfer admittance (Y_{fs} or g_{fs}) varies widely for different types of *FET*. For a small-signal or switching *JFET*, Y_{fs} typically ranges from 1000 μS to 5000 μS. For an *E-MOSFET*, Y_{fs} might be 2.9 S.

The drain resistance (r_d) shown in the equivalent circuit is the *ac* resistance offered between the drain and source terminals of the *FET* when operating in the pinch-off region of the drain characteristics. This quantity is usually defined in terms of an output admittance (Y_{os}) which equals $1/r_d$. Typical values of r_d range from 20 kΩ to 100 kΩ for a *JFET*.

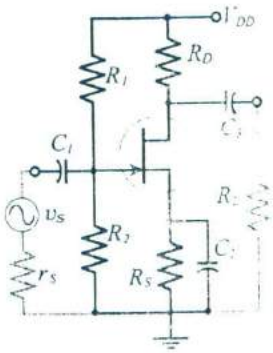


Figure 11-6
FET common-source amplifier circuit.

Section 11-2 Review

11-2.1 Sketch the low- and medium-frequency equivalent circuit for a *FET*. Identify all components, list typical component values, and briefly explain how the equivalent circuit represents the device.

11-3 Common Source Circuit Analysis

Common Source Circuit

The circuit of a *FET* common-source amplifier is shown in Fig. 11-6. With the capacitors treated as *ac* short-circuits, the circuit input terminals are the gate and source, and the output terminals are the drain and the source. So, the source terminal is *common* to both input and output, and the circuit configuration is known as *common-source* (*CS*).

The current and voltage waveforms for the *CS* circuit in Fig. 11-6 are illustrated in Fig. 11-7. The 180° *phase shift* between the input and output waveforms can be understood by considering the effect of a positive-going input signal. An increase in v_s increases the *FET* gate-source voltage (V_{GS}), thus raising the level of I_D, and increasing the voltage drop across R_D. This produces a decrease in the level of the drain voltage (V_D), which is capacitor-coupled to the circuit output as a negative-going *ac* output voltage (v_o). Consequently, as v_s increases in a positive direction, v_o changes in a negative direction, as illustrated. Conversely, when v_s changes in a negative direction, the resultant decrease in V_{GS} reduces I_D and produces a positive-going output.

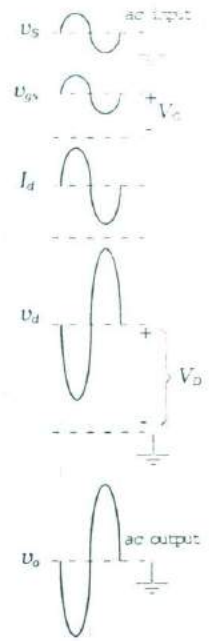


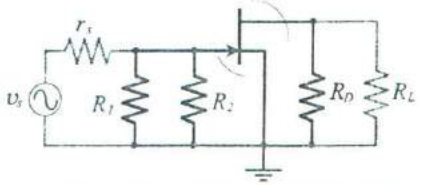
Figure 11-7
Voltage and current waveforms in a common-source circuit.

The circuit in Fig. 11-6 has an *input impedance* (Z_i), an *output impedance* (Z_o), and a *voltage gain* (A_v). Equations for these quantities can be determined by *ac* analysis of the circuit.

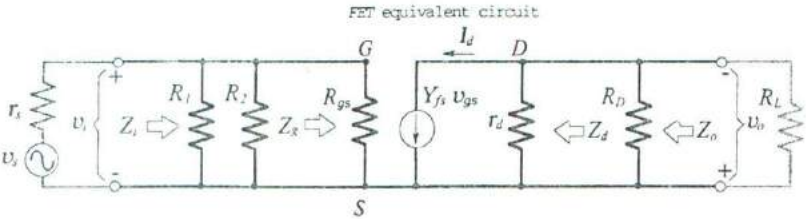
Common Source Equivalent Circuit

The first step in *ac* analysis of a *FET* (or *BJT*) circuit is to draw the *ac* equivalent circuit, by substituting *ac* short-circuits in place of the power supply and capacitors. When this is done for the circuit in Fig. 11-6, the *ac* equivalent circuit shown in Fig. 11-8(a) is created. For *ac* analysis, the *FET* equivalent circuit [from Fig. 11-5(b)] is now substituted in place of the device. This results in the *CS ac* equivalent circuit in Fig. 11-8(b).

The current directions and voltage polarities in Fig. 11-8(b) are those that occur when the instantaneous level of the input voltage is moving in a positive direction.



(a) *ac* equivalent circuit for *FET CS* circuit



(b) Substitution of the *FET* equivalent circuit into the *CS* ac equivalent circuit

Figure 11-8
A common-source ac equivalent circuit is drawn by first replacing the power supply and all capacitors with short-circuits, then the FET model is substituted in place of the device.

Input Impedance

Considering the input section of the equivalent circuit in Fig. 6-8(b) it is seen that the input impedance at the *FET* terminals is,

$$Z_g = R_{gs} \tag{11-1}$$

As already discussed, a typical value of R_{gs} for a low-current *JFET* is $10^9\ \Omega$. At the circuit input terminals, resistors R_1 and R_2 are seen to be in parallel with Z_g. So, the circuit input impedance is,

$$Z_i = R_1 \| R_2 \| Z_g \tag{11-2}$$

Because Z_g is so large, the circuit input impedance is almost always determined by the bias resistors.

$$Z_i \approx R_1 \| R_2 \tag{11-3}$$

So, the input impedance of a *FET* circuit can usually be determined simply by calculating the equivalent resistance of the bias resistors. However, as already discussed, very high input resistance is one of the most important properties of a *FET*. In circumstances where it is necessary to achieve the highest possible input resistance, the signal source might be directly connected in series with the gate terminal, and in this case $Z_i \approx Z_g$.

In the case of the self biased circuit in Fig. 11-4, the circuit input impedance is equal to the gate bias resistor R_G.

Output Impedance

Looking into the output of the *CS* equivalent circuit in Fig. 11-8(b), the output impedance at the *FET* drain terminal is,

$$\mathbf{Z_d = r_d} \qquad \textbf{(11-4)}$$

At the circuit output terminals, resistor R_D is in parallel with Z_d. So, the circuit output impedance is,

$$\mathbf{Z_o = R_D || r_d} \qquad \textbf{(11-5)}$$

Because r_d is typically 100 kΩ, and R_D is usually much lower than 50 kΩ, the circuit output impedance is approximately equal to R_D. Using this information, the output impedance of a *CS* circuit can be discovered simply by reading the resistance of R_D.

$$\mathbf{Z_o \approx R_D} \qquad \textbf{(11-6)}$$

Voltage Gain

Amplifier voltage gain is given by the equation,

$$A_v = \frac{v_o}{v_i}$$

From Fig. 11-8(b), $v_o = I_d\,(r_d || R_D || R_L)$

and $I_d = -Y_{fs}\, v_i$

so, $$A_v = \frac{-Y_{fs}\, v_i\,(r_d || R_D || R_L)}{v_i}$$

or, $$\mathbf{A_v = -Y_{fs}(r_d || R_D || R_L)} \qquad \textbf{(11-7)}$$

The minus sign in Eq. 11-7 indicates that v_o is 180° out of phase with v_i. (When v_i increases, v_o decreases, and vice versa.) It is seen that the voltage gain of a common source amplifier is directly proportional to the Y_{fs} of the *FET*. If the appropriate Y_{fs} value and the resistance of R_D and R_L are known, the voltage gain of a *CS* circuit can be quickly estimated. For Y_{fs} = 5000 μS, R_D = 4.7 kΩ, and with $R_L >> R_D$, and $r_d >> R_D$, the voltage gain is -23.5.

The voltage gain of a *FET* common-source amplifier is typically about one tenth of the gain of a *BJT* common-emitter circuit. Low

voltage gain, caused by the low Y_{fs} value, is the major disadvantage of *JFET* circuits compared to *BJT* circuits. The same is generally true of *MOSFET* circuits, except for *E-MOSFET* devices (*V-MOS* and *T-MOS*), which have much larger Y_{fs} values. However, *E-MOSFETs* use relatively large drain currents, and they are normally unsuitable for small-signal applications.

Summary of Typical CS Circuit Performance

Device input impedance	$Z_g = R_{gs}$
Circuit input impedance	$Z_i = R_1 \| R_2 \| Z_g \approx R_1 \| R_2$
Device output impedance	$Z_d = r_d$
Circuit output impedance	$Z_o = R_D \| r_d \approx R_D$
Circuit voltage gain	$A_v = -Y_{fs}(r_d \| R_D \| R_L)$

The common-source circuit has voltage gain, 180° phase shift, high input impedance, and relatively high output impedance.

Example 11-2

Calculate the input impedance, output impedance, and voltage gain for the common-source circuit in Fig. 11-9 using the *FET* typical parameters.

Solution

From the 2N5457 data sheet

$$r_d = \frac{1}{Y_{os}} = \frac{1}{10\,\mu S}$$
$$= 100\ k\Omega$$

and, $Y_{fs} = 3000\,\mu S$

Eq. 11-3, $Z_i = R_1 \| R_2 = 1\ M\Omega \| 5.6\ M\Omega$
$= 848\ k\Omega$

Eq. 11-5, $Z_o = R_D \| r_d = 2.7\ k\Omega \| 100\ k\Omega$
$= 2.63\ k\Omega$

Eq. 11-7, $A_v = -Y_{fs}(r_d \| R_D \| R_L) = -3000\,\mu S\ (100\ k\Omega \| 2.7\ k\Omega)$
$= -7.9$

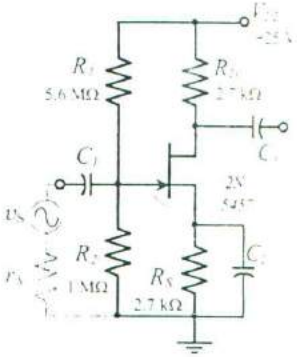


Figure 11-9
Circuit for Ex. 11-2.

Practise Problems

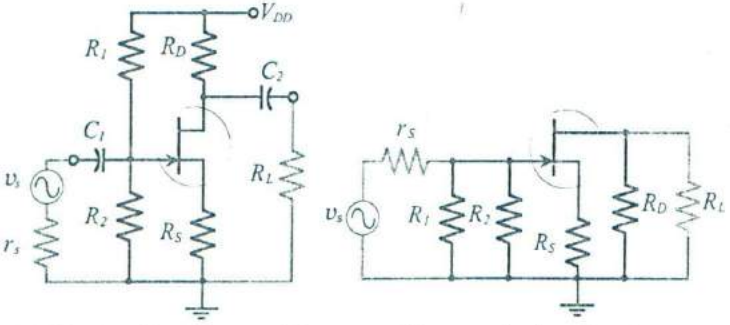
11-3.1 Calculate the typical input impedance, output impedance, and voltage gain for the circuit in Fig. 11-4, if the *FET* is a *2N5458*.

11-3.2 A circuit similar to the one in Fig. 11-4 has $R_G = 470\ k\Omega$, $R_D = 3.9\ k\Omega$, and a *2N5457 FET*. Determine the typical input impedance, output impedance, and voltage gain for the circuit.

11-4 CS Circuit with Unbypassed Source Resistor

Equivalent Circuit

When an unbypassed source resistor (R_S) is present in a *FET* common-source circuit, as shown in Fig.11-10(a), it also appears in the *ac* equivalent circuit, [Fig. 11-10(b)]. In the complete equivalent circuit R_S must be shown connected between the *FET* source terminal and the circuit common input-output terminal, (Fig. 11-11). As with the previous equivalent circuit, the current directions and voltage polarities shown in Fig. 11-11 are those that occur when the instantaneous input voltage is positive-going. The presence of R_S without a bypass capacitor significantly affects the circuit voltage gain.



(a) Circuit with unbypassed R_S (b) *ac* equivalent circuit

Figure 11-10
FET common-source circuit with unbypassed source resistor, and ac equivalent circuit.

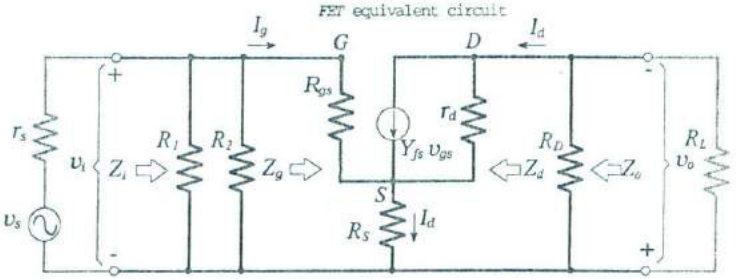


Figure 11-11
An unbypassed source resistor in a FET circuit must be included in the complete ac equivalent circuit.

Input Impedance

An equation for the input impedance at the *FET* gate can be determined from v_i and I_g. From Fig. 11-11,

$$v_i = v_{gs} + I_d R_S = v_{gs} + Y_{fs} v_{gs} R_S$$
$$= v_{gs}(1 + Y_{fs} R_S)$$

and,

$$I_g = \frac{v_{gs}}{R_{gs}}$$

so, $$Z_g = \frac{v_i}{I_g} = \frac{v_{gs}(1 + Y_{fs}R_S)}{v_{gs}/R_{gs}}$$

or, $$\mathbf{Z_g = R_{gs}(1 + Y_{fs}R_S)} \qquad \textbf{(11-8)}$$

Equation 11-8 gives the input impedance at the *FET* gate terminal. The circuit input impedance is again given by Eq. 11-2,

$$Z_i = R_1 \| R_2 \| Z_g$$

In this case, Z_g is much larger than $R_1 \| R_2$, so the circuit input impedance is determined by the gate bias resistors.

Eq. 11-3. $Z_i \approx R_1 \| R_2$

Output Impedance

To calculate the circuit output impedance, the *ac* signal voltage (v_s) is assumed to be zero, and an *ac* voltage (v_o) is applied at the output, (see Fig. 11-12(a). The *ac* output current (I_d) is calculated in terms of v_o, then Z_o is determined as v_o divided by I_d. Figure 11-12(a) shows that when v_s is zero, the *ac* voltage across source resistor R_S is applied as a gate-source voltage.

$$v_{gs} = I_d R_S$$

Actually, $I_d R_S$ is divided across $r_s \| R_G$ and R_{gs}. However, $R_{gs} >> r_s \| R_G$ so that all of $I_d R_S$ is effectively applied as a gate-source voltage. The v_{gs} produced in this way generates an *ac* drain current which opposes the drain current produced by v_o.

$$I = -Y_{fs}v_{gs} = -Y_{fs}(I_d R_S)$$

Converting the current generator $I(Y_{fs}v_{gs})$ in parallel with r_d to a voltage generator $I(Y_{fs}v_{gs}r_d)$ in series with r_d gives the equivalent circuit in Fig. 11-12(b). The equation for the voltage drops around this circuit is,

$$I_d(r_d + R_S) = v_o - (Y_{fs}\, I_d\, R_S\, r_d)$$

giving, $$v_o = I_d(r_d + R_S + Y_{fs}R_S r_d)$$

and, $$Z_d = \frac{v_o}{I_d} = r_d + R_S + Y_{fs}R_S r_d$$

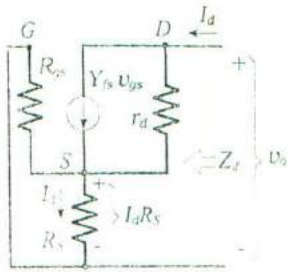
or, $$\mathbf{Z_d = r_d + R_S + Y_{fs}R_S r_d} \qquad \textbf{(11-9)}$$

The circuit output impedance is,

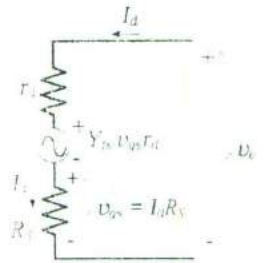
Eq. 11-5. $Z_o = R_D \| Z_d$

Because the output impedance at the *FET* drain terminal is much larger than the drain resistor (R_D), the output impedance of the circuit with the unbypassed source resistor is still,

Eq. 11-6. $Z_o \approx R_D$



(a) Circuit output stage with input shorted



(b) Current source replaced with a voltage source

Figure 11-12
Analysis of the output impedance of a common-source circuit with an unbypassed source resistor.

Voltage Gain

From the derivation of the input impedance equation,

$$v_i = v_{gs}(1 + Y_{fs}R_S)$$

and neglecting r_d,

$$v_o = I_d(R_D \| R_L) = -Y_{fs}v_{gs}(R_D \| R_L)$$

so,
$$A_v = \frac{v_o}{v_i} = \frac{-Y_{fs}v_{gs}(R_D \| R_L)}{v_{gs}(1 + Y_{fs}R_S)}$$

giving,
$$\mathbf{A_v = \frac{-Y_{fs}(R_D \| R_L)}{1 + Y_{fs}R_S}} \qquad \textbf{(11-10)}$$

Usually, $Y_{fs}R_S >> 1$

so,
$$\mathbf{A_v \approx \frac{-(R_D \| R_L)}{R_S}} \qquad \textbf{(11-11)}$$

The voltage gain of a *FET* common-source circuit with an unbypassed source resistor can be quickly estimated using Eq. 11-11. For the circuit in Fig. 11-10(a), with R_D = 4.7 kΩ, R_S = 2.2 kΩ and $R_L >> R_D$, $A_v \approx$ -2.1.

Summary of Performance of CS Circuit with Unbypassed R_S

Device input impedance	$Z_g = R_{gs}(1 + Y_{fs}R_S)$
Circuit input impedance	$Z_i = R_G \| Z_g \approx R_1 \| R_2$
Circuit output impedance	$Z_o \approx R_D$
Circuit voltage gain	$A_v = \frac{-Y_{fs}(R_D \| R_L)}{1 + Y_{fs}R_S}$
Circuit voltage gain	$A_v \approx \frac{-(R_D \| R_L)}{R_S}$

The most significant feature of the performance of a *CS* circuit with an unbypassed source resistor is that its voltage gain is much lower than that for a *CS* circuit with R_S bypassed.

Example 11-3

For the common-source circuit in Fig. 11-13, calculate the gate input impedance, the drain output impedance, the circuit input and output impedances, and the voltage gain. Use the typical parameters for the *FET*.

Solution

From the *2N5458* data sheet,

$$r_d = \frac{1}{Y_{os}} = 100\ \text{k}\Omega$$

$$Y_{fs} = 4000\ \mu\text{S}$$

and,
$$I_G = 1\ \text{nA with } V_{GS} = 15\ \text{V}$$

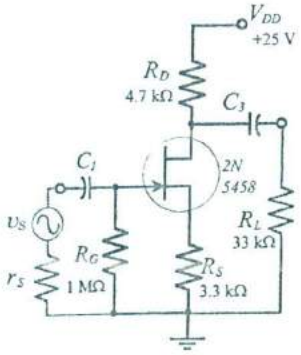


Figure 11-13
Circuit for Example 11-3.

so, $$R_{gs} = \frac{V_{GS}}{I_G} = \frac{15\text{ V}}{1\text{ nA}}$$
$$= 15 \times 10^9\ \Omega$$

Eq. 11-8, $$Z_g = R_{gs}(1 + Y_{fs}R_S) = 15 \times 10^9\ \Omega[1 + (4\text{ mS} \times 3.3\text{ k}\Omega)]$$
$$= 2.13 \times 10^{11}\ \Omega$$

from Eq. 11-3, $$Z_i = R_G = 1\text{ M}\Omega$$

Eq. 11-9, $$Z_d = r_d + R_S + (Y_{fs}R_S r_d)$$
$$= 100\text{ k}\Omega + 3.3\text{ k}\Omega + (4\text{ mS} \times 3.3\text{ k}\Omega \times 100\text{ k}\Omega)$$
$$\approx 1.4\text{ M}\Omega$$

Eq. 11-5, $$Z_o = R_D \| Z_d = 4.7\text{ k}\Omega \| 1.4\text{ M}\Omega$$
$$= 4.68\text{ k}\Omega$$

Eq. 11-10, $$A_v = \frac{-Y_{fs}(R_D \| R_l)}{1 + Y_{fs}R_S} = \frac{-4\text{ mS} \times (4.7\text{ k}\Omega \| 33\text{ k}\Omega}{1 + (4\text{ mS} \times 3.3\text{ k}\Omega)}$$
$$= -1.16$$

or, Eq. 11-11, $$A_v \approx \frac{-(R_D \| R_l)}{R_S} = \frac{4.7\text{ k}\Omega \| 33\text{ k}\Omega}{3.3\text{ k}\Omega}$$
$$= -1.24$$

Practise Problems

11-4.1 Calculate the gate input impedance, drain output impedance, the circuit input and output impedance, and the voltage gain for the circuit in Fig. 11-4, when the source bypass capacitor is removed. Assume that the *FET* is a *2N5458*.

11-4.2 Determine the items listed in Problem 11-4.1 for the circuit in Fig. 11-9 when the source bypass capacitor is removed.

11-5 Common Drain Circuit Analysis

Common Drain Circuit

The *FET* common-drain circuit shown in Fig. 11-14 has the output voltage developed across the source resistor (R_S). The external load (R_L) is capacitor-coupled to the source terminal of the *FET*, and the gate bias voltage (V_G) is derived from V_{DD} by means of voltage divider resistors R_1 and R_2. No resistor is connected in series with the drain terminal, and no source bypass capacitor is employed.

To understand the operation of the circuit in Fig. 11-14 note that the *dc* gate voltage (V_G) is a constant quantity, and the source voltage is,

$$V_S = V_G + V_{GS}$$

When an *ac* signal is applied to the gate via capacitor C_1, the gate

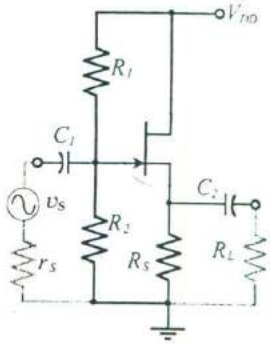


Figure 11-14
Common-drain circuit, also called a source follower. The ac input is applied to the FET gate, and the output is taken from the source terminal.

voltage is increased and decreased as the instantaneous level of the signal voltage rises and falls. Also, V_{GS} remains substantially constant, so the source voltage increases and decreases with the gate voltage. (See the waveforms in Fig. 11-15.) Thus, the *ac* output voltage is closely equal to the *ac* input voltage, and the circuit can be said to have unity gain. AC analysis of the circuit shows that v_o is slightly smaller than v_i. Because the output voltage at the source terminal follows the signal voltage at the gate, the common-drain circuit is also known as a *source follower.*

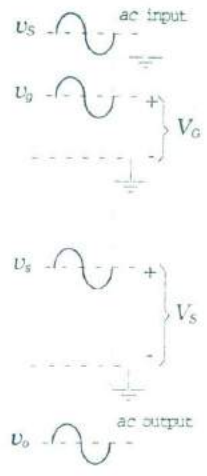
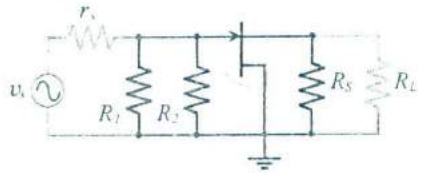


Figure 11-15
Voltage waveforms in a common-drain circuit.

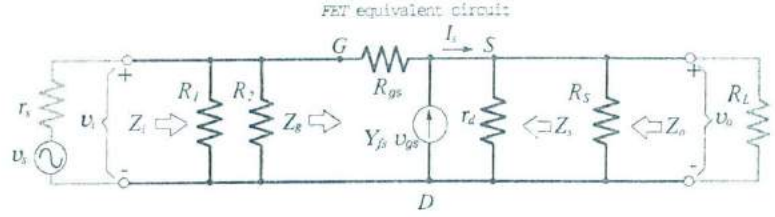
Common Drain Equivalent Circuit

As in the case of other circuits, the supply voltage and coupling capacitors in Fig. 11-14 must be replaced with short-circuits in order to study the circuit *ac* performance. This gives the common-drain *ac* equivalent circuit in Fig. 11-16(a). The input terminals of the *ac* equivalent circuit are seen to be the *FET* gate and drain, and the output terminals are the source and drain. Because the drain terminal is common to both input and output, the circuit configuration is named *common-drain (CD).*

The completer *CD ac* equivalent circuit is drawn by substituting the *FET* model into the *ac* equivalent circuit. [Fig. 11-16(b)]. The indicated current directions and voltage polarities are, once again, those that are produced by a positive-going signal voltage.



(a) *ac* equivalent circuit for *FET CD* circuit



(b) Substitution of the *FET* equivalent circuit into the *CD* ac equivalent circuit

Figure 11-16
A common-drain ac equivalent circuit is drawn by first replacing the power supply and all capacitors with short-circuits, then the FET model is substituted in place of the device.

Input Impedance

Looking into the gate and drain terminals in Fig. 11-16(b), is similar to *looking into* the input of a common-source amplifier with an unbypassed source resistor. Therefore, the common-drain Z_g equation is derived in the same way as Eq. 11-8. One important difference is that the common-drain circuit has the external load resistor (R_L) in parallel with R_S.

$$Z_g = R_{gs}[1 + Y_{fs}(R_S||R_L)] \qquad \textbf{(11-12)}$$

As discussed in Section 11-4, the equation for Z_g gives a very large value. This is important only when the signal source is connected directly in series with the gate terminal. With the signal capacitor-coupled to the input, the circuit input impedance is,

Eq. 11-2. $$Z_i = R_1 \| R_2 \| Z_g$$

which reduces to,

Eq. 11-3. $$Z_i \approx R_1 \| R_2$$

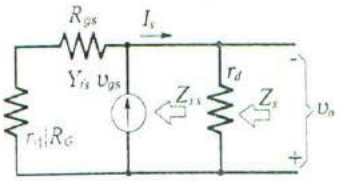


Figure 11-17
Analysis of the output impedance of a common-drain circuit.

Output Impedance

In a common-drain circuit, any variation in the output voltage (v_o) has an effect on the *FET* gate-source voltage. To determine the impedance *looking into* the source terminal, the signal voltage [in Fig. 11-16(b)] is assumed to be zero, and the output current (I_s) is calculated in terms of v_o. The circuit is redrawn in Fig. 11-17 with resistor R_G representing the gate bias resistors, [$R_G = R_1 \| R_2$ in Fig. 11-16(a)]. With $v_s = 0$, v_o is divided across $R_G \| r_s$ and R_{gs}, (see Fig. 11-17). Because $R_{gs} >> (R_G \| r_s)$, effectively all of v_o is applied as an *ac* gate-source voltage. So,

$$I_s = Y_{fs}\, v_o$$

and, $$Z_{ss} = \frac{v_o}{I_s} = \frac{v_o}{Y_{fs}\, v_o} \qquad \text{(see Fig. 11-17)}$$

or, $$Z_{ss} = 1/Y_{fs}$$

also, $$Z_s = Z_{ss} \| r_d$$

so, $$\boldsymbol{Z_s = (1/Y_{fs}) \| r_d} \qquad \textbf{(11-13)}$$

Equation 11-13 gives the device output impedance. The circuit output impedance also involves R_S.

$$\boldsymbol{Z_o = (1/Y_{fs}) \| R_S \| r_d} \qquad \textbf{(11-14)}$$

The drain resistance is usually much larger than R_S, and R_S is usually much larger than $1/Y_{fs}$, so that $Z_o \approx 1/Y_{fs}$. For $Y_{fs} = 5000$ μS, $Z_o = 200\ \Omega$.

Voltage Gain

From Fig. 11-16(b),

$$v_o = I_s(R_S \| R_L) = Y_{fs} v_{gs}(R_S \| R_L)$$

and, $$v_i = v_{gs} + v_o = v_{gs} + Y_{fs} v_{gs}(R_S \| R_L)$$
$$= v_{gs}[1 + Y_{fs}(R_S \| R_L)]$$

so, $$A_v = \frac{v_o}{v_i} = \frac{Y_{fs} v_{gs}(R_S \| R_L)}{v_{gs}[1 + Y_{fs}(R_S \| R_L)]}$$

or, $$\boldsymbol{A_v = \frac{Y_{fs}(R_S \| R_L)}{1 + Y_{fs}(R_S \| R_L)}} \qquad \textbf{(11-15)}$$

As already discussed, the *ac* output voltage from a *CD* circuit is usually closely equal to the input voltage, so the voltage gain is normally taken as,

$$A_v \approx 1 \qquad \textbf{(11-16)}$$

Summary of CD Circuit Performance

Device input impedance	$Z_g = R_{gs}[1 + Y_{fs}(R_S \| R_L)]$
Circuit input impedance	$Z_i \approx R_1 \| R_2$
Device output impedance	$Z_s = (1/Y_{fs}) \| r_d$
Circuit output impedance	$Z_o = (1/Y_{fs}) \| R_S \| r_d \approx (1/Y_{fs}) \| R_S$
Circuit voltage gain	$A_v = \dfrac{Y_{fs}(R_S \| R_L)}{1 + Y_{fs}(R_S \| R_L)}$
Circuit voltage gain	$A_v \approx 1$

A common-drain circuit has a voltage gain approximately equal to 1, no phase shift between input and output, very high input impedance, and low output impedance. Because of its high Z_i, low Z_o, and unity gain, the *CD* circuit is usually used as a *buffer amplifier* between a high impedance signal source and a low impedance load.

Example 11-4

The common-drain circuit in Fig. 11-18 has a *FET* with $Y_{fs} = 3000\ \mu S$, $R_{gs} = 100\ M\Omega$, and $r_d = 50\ k\Omega$. Determine the input and output impedances at the device terminals, and the circuit input and output impedances. Also, calculate the circuit voltage gain.

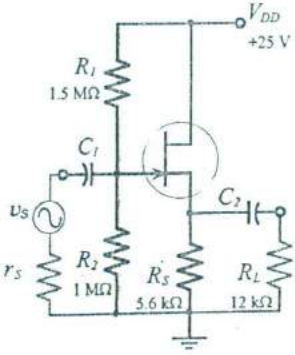


Figure 11-18
Circuit for Example 11-4.

Solution

Eq. 11-12, $$Z_g = R_{gs}[1 + Y_{fs}(R_S \| R_L)]$$
$$= 100\ M\Omega[1 + 3000\ \mu S(5.6\ k\Omega \| 12\ k\Omega)]$$
$$= 1.25 \times 10^9\ \Omega$$

Eq. 11-2, $$Z_i \approx R_1 \| R_2 = 1.5\ M\Omega \| 1\ M\Omega$$
$$= 600\ k\Omega$$

Eq. 11-13, $$Z_s = (1/Y_{fs}) \| r_d = (1/3000\ \mu S) \| 50\ k\Omega$$
$$= 326\ \Omega$$

Eq. 11-14, $$Z_o = (1/Y_{fs}) \| R_S \| r_d = 326\ \Omega \| 5.6\ k\Omega \| 50\ k\Omega$$
$$= 306\ \Omega$$

Eq. 11-15, $$A_v = \frac{Y_{fs}(R_S \| R_L)}{1 + Y_{fs}(R_S \| R_L)} = \frac{3000\ \mu S(5.6\ k\Omega \| 50\ k\Omega)}{1 + [3000\ \mu S(5.6\ k\Omega \| 50\ k\Omega)]}$$
$$= 0.94$$

Practise Problems

11-5.1 Calculate the device and circuit input and output impedances for a common-drain circuit (as in Fig. 11-18) with the following components: $R_1 = 470\ k\Omega$, $R_2 = 330\ k\Omega$, $R_S = 3.3\ k\Omega$, $R_L = 47\ k\Omega$. Assume that the *FET* is a *2N5458*.

11-6 Common-Gate Circuit Analysis

Common-Gate Circuit

The *FET* common-gate (*CG*) circuit shown in Fig. 11-19 uses voltage divider bias. The *ac* output is taken from the drain terminal, and an external load (R_L) is capacitor-coupled to the drain, exactly as in the case of a common-source circuit. Unlike a *CS* circuit, the *ac* input for the *CG* circuit is applied to the *FET* source terminal (via C_3), and a capacitor (C_1) is included to *ac* short-circuit the gate to ground. Because the gate is grounded, all of the *ac* input voltage appears across the gate-source terminals.

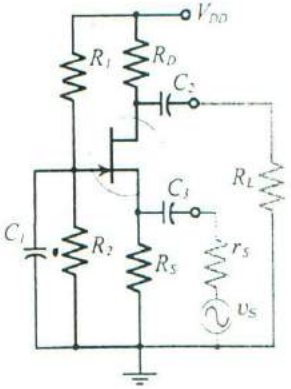


Figure 11-19
In a common-gate circuit the signal is capacitor-coupled to the FET source terminal, and the output is taken from the drain.

The current and voltage waveforms for the *CG* circuit shown in Fig. 11-20 illustrate the circuit operation. When the instantaneous level of the *ac* signal voltage increases, the source voltage increases while the gate voltage remains constant. Consequently, the gate-source voltage decreases, the drain current is reduced, and the output voltage at the drain terminal is increased. Similarly, when v_i decreases, v_{gs} increases, I_d increases, and v_d decreases. Thus, an increase in v_i causes an increase in v_o, and a decrease in v_i produces a decrease in v_o; so, there is no phase shift between the input and the output. (See the voltage and current waveforms in Fig. 11-20.)

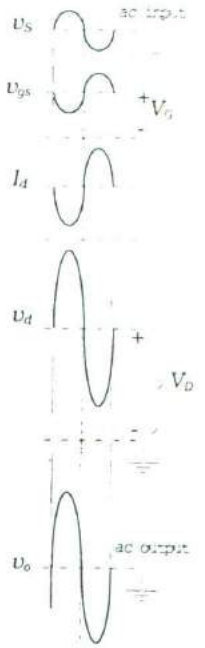


Figure 11-20
Voltage and current waveforms in a common-gate circuit.

Common Gate Equivalent Circuit

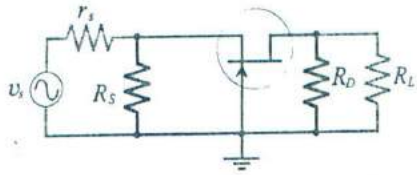
As in the case of other circuits, the supply voltage and capacitors in Fig. 11-19 are replaced with short-circuits in order to study the circuit *ac* performance. This gives the common-gate *ac* equivalent circuit in Fig. 11-21(a). The input terminals of the *ac* equivalent circuit are seen to be the *FET* source and gate, and the output terminals are the drain and gate. The gate terminal is common to both input and output, so the circuit is named *common-gate*.

The completer *CG ac* equivalent circuit is drawn by substituting the *FET* model into the *ac* equivalent circuit, [Fig. 11-21(b)]. As always, the indicated current directions and voltage polarities are those that are produced by a positive-going signal voltage.

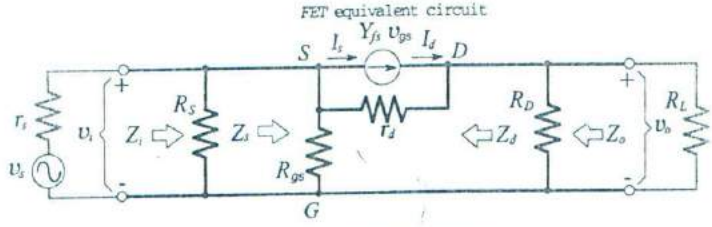
Input Impedance

'Looking into' the source and gate terminals of the *CG* circuit in Fig. 11-21(b), is similar to 'looking into' the output of a common-drain circuit. Therefore, the equation for the common-gate device input impedance (Z_s) is derived in the same way as the equation for Z_s in the common-drain circuit.

$$Z_s = 1/Y_{fs} \qquad (11\text{-}17)$$



(a) *ac* equivalent circuit for *FET CG* circuit



(b) Complete common-gate *ac* equivalent circuit

Figure 11-21
A common-gate ac equivalent circuit is drawn by first replacing the power supply and all capacitors with short-circuits, then the FET model is substituted in place of the device.

The circuit input impedance is R_S in parallel with the device input impedance.

so, $$Z_i = (1/Y_{fs}) || R_S \qquad \textbf{(11-18)}$$

Using a typical Y_{fs} of 5000 μS, the input impedance of a common-gate circuit is around 200 Ω. Low input impedance is the major disadvantage of the common-gate circuit, because the signal voltage is divided across r_s and Z_s, (see Fig. 11-22).

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} \qquad \textbf{(11-19)}$$

Output Impedance

The output of a common-gate circuit is taken from the drain terminal, as in the case of a common-source circuit. So, the common-gate output impedance is the same as the common-drain output impedance. At the drain terminal,

Eq. 11-4, $$Z_d = r_d$$

and the circuit output impedance is,

Eq. 11-5, $$Z_o = R_D || r_d$$

Voltage Gain

From Fig. 11-21(b),

$$v_o = I_d(R_D || R_L) = Y_{fs} v_i (R_D || R_L)$$

and, $$A_v = \frac{v_o}{v_i} = \frac{Y_{fs} v_i (R_D || R_L)}{v_i}$$

or, $$A_v = Y_{fs}(R_D || R_L) \qquad \textbf{(11-20)}$$

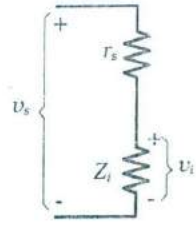


Figure 11-22
Because a common-gate circuit has a low input impedance, some of the signal voltage is lost when it is divided across r_s and Z_i.

Equation 11-20 is similar to Eq. 11-7 for the voltage gain of a common-source circuit, with the exception that there is no minus sign in Eq. 11-20. So, the voltage gain for a common-gate circuit is the same as the voltage gain for a common-source circuit with the same component values. As, already discussed, there is no phase shift between the input and output of a common-gate circuit, hence the absence of the minus sign in Eq. 11-20.

Effect of Unbypassed Gate Resistors

If capacitor C_1 is not present in the *CG* circuit in Fig. 11-19, the *FET* gate is *not ac* short-circuited to ground. So, a resistance ($R_G = R_1 \| R_2$) must be included in the *ac* equivalent circuit (see Fig. 11-23), and in the complete *CG ac* equivalent circuit. The presence of the unbypassed gate resistors affects the circuit input impedance and voltage gain. Analysis of the equivalent circuit shows that,

$$Z_i = (1/Y_{fs})\frac{R_G + R_{gs}}{R_{gs}} \qquad \textbf{(11-21)}$$

and,

$$A_v = Y_{fs}(R_D \| R_L)\frac{R_{gs}}{R_G + R_{gs}} \qquad \textbf{(11-22)}$$

When $R_{gs} >> R_G$ (which is usually the case), Eq. 11-21 gives $Z_i = 1/Y_{fs}$, and Eq. 11-22 gives $A_v = Y_{fs}(R_D \| R_L)$, which are the equations for a *CG* circuit with the gate bypassed to ground. The Z_i and A_v effects occur only in situations where very high value bias resistors are used in a *CG* circuit. Figure 11-24 shows a *CG* circuit that uses self bias. In this case, R_G is omitted because there is no signal applied at the gate input; the gate is directly grounded and no gate bypass capacitor is required.

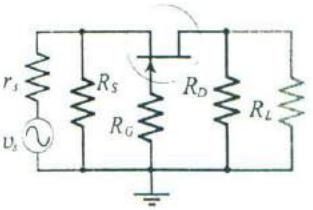


Figure 11-23
When the gate bypass capacitor is omitted in a CG circuit, the equivalent resistance of the gate bias resistors (R_G) must be included for circuit analysis.

Summary of CG Circuit Performance

With the gate bypassed to ground:

Device input impedance	$Z_s = 1/Y_{fs}$
Circuit input impedance	$Z_i = (1/Y_{fs}) \| R_S$
Device output impedance	$Z_d = r_d$
Circuit output impedance	$Z_o = R_D \| r_d$
Circuit voltage gain	$A_v = Y_{fs}(R_D \| R_L)$

With the gate unbypassed:

Circuit input impedance	$Z_i = (1/Y_{fs})\dfrac{R_G + R_{gs}}{R_{gs}}$
Circuit voltage gain	$A_v = Y_{fs}(R_D \| R_L)\dfrac{R_{gs}}{R_G + R_{gs}}$

A common-gate circuit has a voltage gain, no phase shift between input and output, low input impedance, and relatively high output impedance.

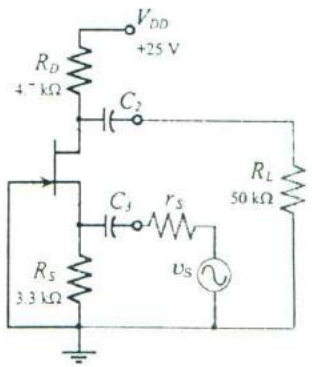


Figure 11-24
A common-gate circuit that uses self bias can have its gate directly grounded.

Example 11-5

The common-gate circuit in Fig. 11-24 has a *FET* with $Y_{fs} = 3000\ \mu S$, and $r_d = 50\ k\Omega$. Determine the device and circuit input and output impedances, and the circuit voltage gain. Also, calculate the overall voltage gain if the signal source impedance is $r_s = 600\ \Omega$.

Solution

Eq. 11-17, $Z_s = 1/Y_{fs} = 1/3000\ \mu S$
$= 333\ \Omega$

Eq. 11-18, $Z_i = (1/Y_{fs})\|R_S = 333\ \Omega \| 3.3\ k\Omega$
$= 302\ \Omega$

Eq. 11-4, $Z_d = r_d = 50\ k\Omega$

Eq. 11-5, $Z_o = R_D\|r_d = 4.7\ k\Omega \| 50\ k\Omega$
$= 4.3\ k\Omega$

Eq. 11-20, $A_v = Y_{fs}(R_D\|R_L) = 3000\ \mu S \times (4.7\ k\Omega \| 50\ k\Omega)$
$= 12.9$

Combining Eq. 11-19 and 11-20, the overall voltage gain is

$$A_v = \frac{Y_{fs}(R_D\|R_L)\, Z_i}{r_s + Z_i} = \frac{12.9 \times 333\ \Omega}{600\ \Omega + 333\ \Omega}$$

$$= 4.6$$

Practise Problems

11-6.1 The common-gate circuit in Fig. 11-19 has the following components: $R_1 = 3.9\ M\Omega$, $R_2 = 2.2\ M\Omega$, $R_D = 3.3\ k\Omega$, $R_S = 1.5\ k\Omega$, and $R_L = 27\ k\Omega$. The *FET* has $Y_{fs} = 3.5\ mS$ and $r_d = 70\ k\Omega$, and the signal source has $r_s = 1\ k\Omega$. Calculate the device and circuit input and output impedances, the circuit voltage gain, and the overall voltage gain.

11-6.2 If the *FET* in Problem 11-6.1 has $R_{gs} = 10\ M\Omega$, determine the circuit input impedance and voltage gain when C_1 is removed.

11-7 Comparison of FET and BJT Circuits

CS, CD, and CG Circuit Comparison

Table 11-1 compares Z_i, Z_o, and A_v for *CS*, *CD*, and *CG* circuits. As already discussed, the *CS* circuit has voltage gain, high input impedance, high output impedance, and a 180° phase shift from input to output. The *CD* circuit has high input impedance, low output impedance, a voltage gain of approximately 1, and no phase shift. The *CG* circuit offers low input impedance, high output impedance, voltage gain, and no phase shift.

Table 11-1 Comparison of common-source, common-drain, and common-gate circuits.

Circuit configuration	Z_i	Z_o	A_v	Phase shift
CS	$\approx R_G$	$\approx R_D$	$-Y_{fs}(R_D\|\|R_L)$	180°
CD	$\approx R_G$	$\approx 1/Y_{fs}$	≈ 1	0
CG	$\approx 1/Y_{fs}$	$\approx R_D$	$Y_{fs}(R_D\|\|R_L)$	0

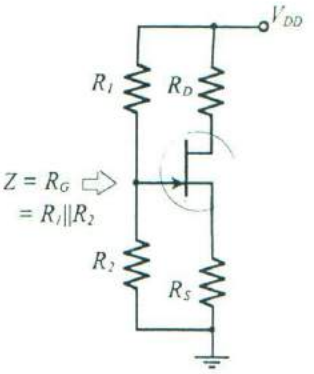


Figure 11-25
FET circuit impedance at the gate terminal.

Impedance at the FET Gate

Consideration of each type of circuit shows that the input or output impedance depends upon which device terminal is involved. In both the *CS* and *CD* circuits, the input signal is applied to the *FET* gate terminal, so Z_i is the impedance *looking into* the gate. Figure 11-25 shows that, for *CS* and *CD* circuits the gate input impedance is,

$$Z_g = R_{gs}$$

and the circuit input impedance is,

$$Z_i = R_G \| R_{gs}$$

where R_G is the equivalent resistance of the bias resistors. Because the reverse-biased gate-source resistance (R_{gs}) is so large, an unbypassed source resistor has no significant effect on Z_i at the gate. The circuit input impedance is largely determined by R_G in both the *CS* and *CD* circuits.

$$Z_i \approx R_G$$
$$= R_1 \| R_2 \text{ (in the case of voltage divider bias)}$$

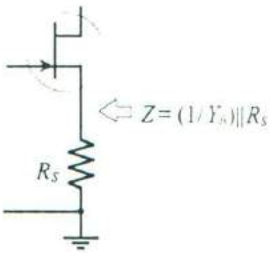


Figure 11-26
FET circuit impedance at the source terminal.

Impedance at the FET Source

The *FET* source is the output terminal for a *CD* circuit and the input terminal for a *CG* circuit. The device impedance in each case is the impedance *looking into* the source, (see Fig. 11-26).

$$Z_s = 1/Y_{fs}$$

The circuit impedance at the source terminal must include the source resistor.

$$Z_i \text{ or } Z_o = (1/Y_{fs}) \| R_S$$

Impedance at the FET Drain

The output for *CS* and *CG* circuits is produced at the *FET* drain terminal. So, the impedance *looking into* the drain is the device output impedance (r_d). As illustrated in Fig. 11-27, the circuit output impedance for any circuit with the output taken from the *FET* drain terminal is,

$$Z_o = R_D \| r_d \approx R_D$$

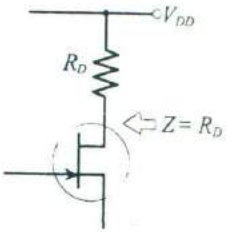


Figure 11-27
FET circuit impedance at the drain terminal.

Voltage gain

In a circuit with an unbypassed source resistor, the *ac* voltage at the source terminal follows the *ac* input at the gate, (see Fig. 11-28). A *CD* circuit (a source follower) has a voltage gain of approximately 1. A *CS* circuit with an unbypassed source resistor has v_i developed across R_S, and so,

$$v_o \approx v_i \times \frac{R_D}{R_S}$$

In a *CG* circuit, and in a *CS* circuit with R_S bypassed, the *ac* input (v_i) is developed across the gate-source terminals, and the *ac* output (v_o) is produced at the drain terminal. Thus, the voltage gain is the same for *CS* and *CG* circuits with similar component values and *FET* parameters. The *CS* voltage gain equation can be used for the *CG* circuit, with the omission of the minus sign that indicates *CS* phase inversion.

Although the voltages gains are equal for similar *CS* and *CG* circuits, the low input impedance of the *CG* circuit can substantially attenuate the signal voltage, and result in a low amplitude output. This is demonstrated in Example 11-6.

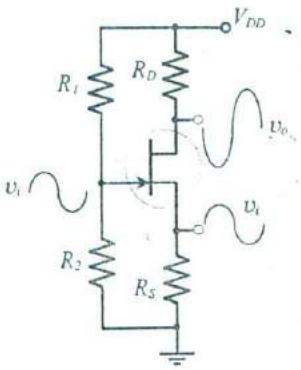


Figure 11-28
In a FET circuit that has an unbypassed R_s, v_i applied to the gate also appears at the source terminal.

Example 11-6

A 50 mV signal with a 600 Ω source resistance is applied to the circuit in Fig. 11-29. Calculate the *ac* output voltage when the conditions are: (a) *CS* circuit operation with the signal coupled to the gate, and R_S bypassed, (b) *CG* circuit operation with the signal applied to the source, and the gate bias resistors bypassed. The *FET* has a forward transfer admittance $Y_{fs} = 6000\ \mu S$.

Solution

(a) *CS circuit*

$$A_v = -Y_{fs}(R_D \| R_L) = -6000\ \mu S\ (2.7\ k\Omega \| 33\ k\Omega)$$
$$\approx -15$$

$$Z_i = R_1 \| R_2 = 100\ k\Omega \| 47\ k\Omega$$
$$= 32\ k\Omega$$

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} = \frac{50\ mV \times 320\ k\Omega}{600\ \Omega + 320\ k\Omega}$$
$$= 49.1\ mV$$

$$v_o = A_v \times v_i = -15 \times 49.1\ mV$$
$$= 736\ mV$$

(b) *CG circuit*

$$A_v = Y_{fs}(R_D \| R_L) = 6000\ \mu S\ (2.7\ k\Omega \| 33\ k\Omega)$$
$$= 15$$

$$Z_i = (1/Y_{fs}) \| R_S = (1/6000\ \mu S) \| 2.7\ k\Omega$$
$$= 157\ \Omega$$

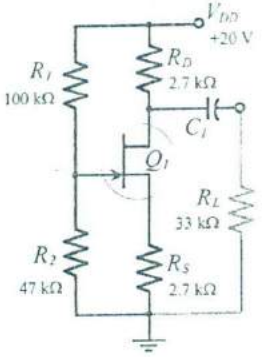


Figure 11-29
Circuit for Ex. 11-6.

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} = \frac{50\text{ mV} \times 157\ \Omega}{600\ \Omega + 157\ \Omega}$$
$$= 10.4\text{ mV}$$

$$v_o = A_v \times v_i = 15 \times 10.6\text{ mV}$$
$$= 156\text{ mV}$$

FET-BJT circuit Comparison

Table 11-2 compares Z_i, Z_o, and A_v for the basic *FET* and *BJT* circuits. The *BJT CE* and *CB* circuits have much higher voltage gains than the corresponding *FET CS* and *CG* circuits, while the *FET CS* and *CD* circuits have much higher input impedances than the *BJT CE* and *CC* circuits. Apart from these differences, *BJTs* and *FETs* can generally perform similar functions. High-frequency, fast-switching, and high-power devices of both types are available. In some switching applications, *FETs* have the advantage of a smaller voltage drop ($V_{DS(on)}$) than that across *BJTs* ($V_{CE(sat)}$). This is discussed in Section 10-11.

Table 11-2 Typical quantities for basic *FET* and *BJT* circuits

FET circuit	A_v	Z_i	Z_o	*BJT* circuit	A_v	Z_i	Z_o
CS	-25	500 kΩ	5 kΩ	*CE*	-250	5 kΩ	5 kΩ
CD	≈ 1	500 kΩ	200 Ω	*CC*	≈ 1	5 kΩ	20 Ω
CG	25	200 Ω	5 kΩ	*CB*	250	20 Ω	5 kΩ

Practise Problems

11-7.1 A *FET* circuit with voltage divider bias has the following component values: $R_1 = 560\text{ k}\Omega$, $R_2 = 390\text{ k}\Omega$, $R_D = 3.9\text{ k}\Omega$, $R_S = 3.3\text{ k}\Omega$, $R_L = 50\text{ k}\Omega$. Assuming that the *FET* is a *2N5457* with typical parameters, calculate the impedances *looking into* the drain, source, and gate terminals.

11-8 Frequency Response of FET Circuits

Low-Frequency Response

The low frequency response of *FET* circuits is determined by exactly the same considerations as for *BJT* circuits. The lower cutoff frequency is normally set by a source bypass capacitor, and it can be affected by coupling capacitors. This is considered in detail in Chapter 12.

High-Frequency Response

Unlike *BJTs*, a device cutoff frequency is not normally specified for

a *FET*. Instead, *FETs* intended for high-frequency operation have the parameters listed as measured at a specified high frequency. The low-frequency parameters are also normally listed. For example, a *2N5484 JFET* has the following parameters:

At f = 1 kHz	min	max
Output conductance (Y_{os})		50 μS
Forward transconductance (Y_{fs})	3000 μS	6000 μS
At f = 100 MHz		
Input admittance (Y_{is})		100 μS
Output conductance (Y_{os})		75 μS
Forward transconductance (Y_{fs})	2500 μS	

The device inter-terminal capacitances (C_{gs}, C_{gd}, and C_{ds}) are important quantities in determining the performance of a *FET* circuit, and these are used in the same way as the *BJT* capacitances. An input capacitance limited cutoff frequency ($f_{2(i)}$), and an output capacitance limited cutoff frequency ($f_{2(o)}$) can be calculated exactly as explained for *BJT* circuits in Section 8-4. The input capacitance is amplified by the Miller effect in the case of a *CS* circuit (an inverting amplifier). Equation 8-9 can be rewritten for the *FET* circuit,

$$C_{in} = C_{gs} + (1 + A_v)\, C_{gd} \qquad \textbf{(11-23)}$$

The *FET* capacitances are specified as the *input capacitance* (C_{iss}), the *reverse transfer capacitance* (C_{rss}), and the *output capacitance* (C_{oss}). The reverse transfer capacitance is another name for the gate-drain capacitance. The input capacitance is the sum of the gate-source capacitance and the gate-drain capacitance. The output capacitance is simply the drain-source capacitance.

$$C_{rss} = C_{gd} \qquad \textbf{(11-24)}$$

$$C_{iss} = C_{gs} + C_{gd} \qquad \textbf{(11-25)}$$

$$C_{oss} = C_{ds} \qquad \textbf{(11-26)}$$

Typical input capacitance values for a *2N5484* high-frequency *JFET* are: C_{rss} = 1 pF, C_{iss} = 5 pF, C_{oss} = 2 pF. Because, these are extremely small, the circuit performance can be easily affected by stray capacitance.

Example 11-7

Calculate the input capacitance limited cutoff frequency for the circuit in Fig. 11-30 when operated as a *CS* circuit with R_S bypassed. Assume that there is no additional stray capacitance at the input terminals.

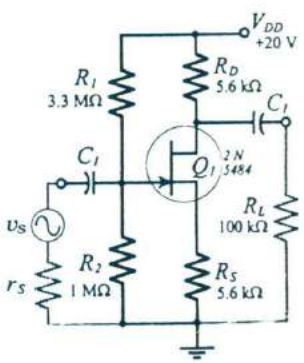


Figure 11-30
Circuit for Ex. 11-7.

Solution

Eq. 11-24, $C_{gd} = C_{rss} = 1$ pF

From Eq. 11-25, $C_{gs} = C_{iss} - C_{rss} = 5\text{ pF} - 1\text{ pF}$
$= 4\text{ pF}$

$|A_v| = Y_{fs}[(1/Y_{os})\|R_D\|R_L]$
$= 2500\,\mu\text{S}\,[(1/75\,\mu\text{S})\|5.6\text{ k}\Omega\|100\text{ k}\Omega]$
$= 9.5$ (note that A_v is a minimum value, because Y_{fs} is the minimum specified value.)

Eq. 11-23, $C_{in} = C_{gs} + (1 + A_v)C_{gd} = 4\text{ pF} + (1 + 9.5)1\text{ pF}$
$= 14.5$ pF (note that C_{in} is a minimum value, because of the minimum A_v.)

Eq. 11-2, $Z_i = R_1\|R_2\|(1/Y_{is}) = 3.3\text{ M}\Omega\|1\text{ M}\Omega\|(1/100\,\mu\text{S})$
$= 9.87\text{ k}\Omega$

From Eq. 8-10, $f_{2(i)} = \dfrac{1}{2\pi C_{in}(r_s\|Z_i)} = \dfrac{1}{2\pi \times 14.5\text{ pF} \times (600\ \Omega\|9.87\text{ k}\Omega)}$
$= 19.4$ MHz

Practise Problems

11-8.1 The *FET* circuit in Fig. 11-30 is reconnected to function as a common-gate circuit with the gate terminal bypassed to ground and no source bypass capacitor. Calculate the input capacitance limited cutoff frequency.

11-8.2 The circuit in Ex. 11-7 has 5 pF of stray capacitance at the output terminal. Calculate the output capacitance limited cutoff frequency.

Chapter-11 Review Questions

Section 11-1

11-1 Sketch a practical common-source amplifier circuit using voltage divider bias. Show a capacitor-coupled signal source and capacitor-coupled load. Explain the need for coupling capacitors, and discuss the correct polarity for connecting the capacitors.

11-2 Explain what is meant by *ac* degeneration in a *FET* circuit. Show how *ac* degeneration is eliminated in voltage divider bias and self bias circuits.

11-3 Discuss the purpose of an *ac* load line for a *FET* circuit. State how *ac* load lines differ from *dc* load lines for circuits with bypassed source resistors, and for circuits with capacitor-coupled loads.

Section 11-2

11-4 Sketch the complete equivalent circuit for a field effect

transistor connected in common-source configuration. Identify each component of the circuit and discuss its origin. Also, sketch a simplified form of the *FET* equivalent circuit for low- and medium-frequency applications.

11-5 Define each parameter in the *FET* low-frequency equivalent circuit, and state typical values.

Section 11-3

11-6 Sketch a practical common-source amplifier circuit using voltage divider bias. Draw *ac* voltage and current waveforms for the circuit, and explain its operation.

11-7 Show what happens to a *CS* circuit when the capacitors and *dc* supply are replaced with *ac* short circuits. Explain.

11-8 Draw the complete *ac* equivalent for a *CS* circuit with voltage divider bias, a bypassed source resistor, a capacitor-coupled signal source, and a capacitor-coupled load.

11-9 Draw the complete *ac* equivalent for a *CS* circuit with self bias, a bypassed source resistor, a capacitor-coupled signal source, and a capacitor-coupled load. Briefly explain.

11-10 Write equations for Z_i, Z_o, and A_v, for the *FET* circuit in Question 11-8.

11-11 Draw the complete *ac* equivalent for a *CS* circuit with gate bias, a bypassed source resistor, a capacitor-coupled signal source, and a capacitor-coupled load. Briefly explain.

11-12 List the performance characteristics for a *CS* circuit, and briefly discuss its usual applications.

Section 11-4

11-13 Draw the complete *ac* equivalent for a *CS* circuit with voltage divider bias, a capacitor-coupled signal source, a capacitor-coupled load, and *no* bypass capacitor across the source resistor. Explain the circuit.

11-14 Write equations for Z_i, Z_o, and A_v for the circuit described in Question 11-12.

11-15 Draw the complete *ac* equivalent for the circuit in Question 11-11 when the source bypass capacitor is removed.

Section 11-5

11-16 Sketch a practical common-drain amplifier circuit using voltage divider bias. Draw *ac* voltage and current waveforms for the circuit, and explain its operation.

11-17 Show what happens to a *CD* circuit when the capacitors and *dc* supply are replaced with *ac* short circuits. Explain.

11-18 Draw the complete *ac* equivalent for a *CD* circuit with voltage divider bias, a capacitor-coupled signal source, and a capacitor-coupled load. Explain the circuit.

11-19 Draw the complete *ac* equivalent for a *CD* circuit with self bias, a capacitor-coupled signal source, and a capacitor-coupled load. Explain.

11-20 Write equations for Z_i, Z_o, and A_v for the *FET* circuits in Questions 11-18 and 11-19.

11-21 List the performance characteristics for a *CD* circuit, and briefly discuss its usual applications.

Section 11-6

11-22 Sketch a practical common-gate amplifier circuit using voltage divider bias. Draw *ac* voltage and current waveforms for the circuit, and explain its operation.

11-23 Show what happens to a *CG* circuit when the capacitors and *dc* supply are replaced with *ac* short circuits. Explain.

11-24 Draw the complete *ac* equivalent for a *CG* circuit with voltage divider bias, a capacitor-coupled signal source, and a capacitor-coupled load. Explain the circuit.

11-25 Sketch a practical common-gate amplifier circuit using self bias. Draw the complete *ac* equivalent for the circuit.

11-26 Write equations for Z_i, Z_o, and A_v for the *FET* circuits in Questions 11-24 and 11-25.

11-27 List the performance characteristics for a *CG* circuit, and briefly discuss its usual applications.

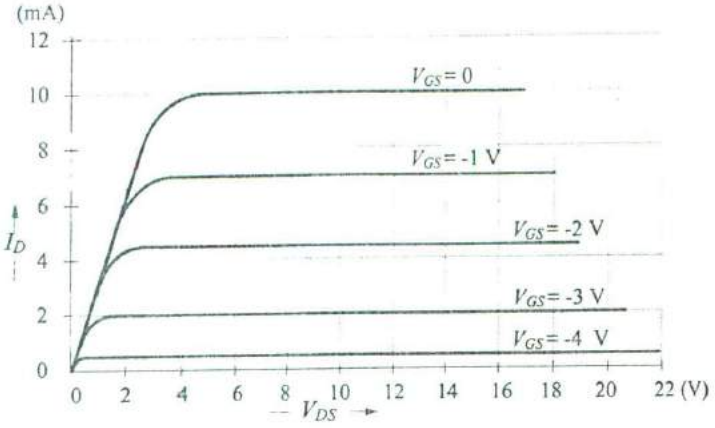


Figure 11-31

Section 11-7

11-28 Compare the performance of *CS*, *CD*, and *CG* circuits, and discuss typical applications of each type of circuit.

11-29 Write equations for the impedances 'seen looking into' the gate, source, and drain terminals of a *FET* in a circuit. Briefly explain each equation.

11-30 Construct a table to compare A_v, Z_i, and Z_o for basic *FET* and *BJT* circuits.

Chapter-11 Problems

Section 11-1

11-1 The drain characteristics for the circuit in Fig. 11-29 are shown in Fig. 11-31. Draw the *dc* and *ac* load lines for the circuit when it is operated in *CS* configuration with R_S bypassed. Assume that the *Q*-point drain current is 1.8 mA.

11-2 Draw the new *ac* load line for the circuit in Problem 11-1 when a 12 kΩ external load resistor (R_l) is capacitor-coupled to the *FET* drain terminal.

11-3 Using the device characteristics in Fig. 11-31, draw the *dc* and *ac* load lines for the *CS* circuit shown in Fig. 11-32. Take the *Q*-point drain current as 2 mA.

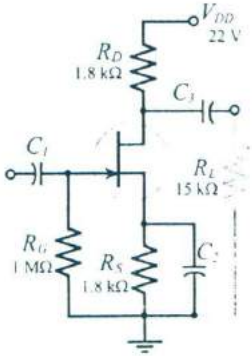


Figure 11-32

Section 11-3

11-4 The *FET* in the *CS* circuit in Fig. 11-33 has Y_{fs} = 6000 μS and r_d = 70 kΩ. Calculate the circuit input impedance, output impedance, and voltage gain.

11-5 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 11-4 when the *FET* is replaced with one having Y_{fs} = 3500 μS, and r_d = 95 kΩ.

11-6 Determine the circuit input impedance, output impedance, and voltage gain for the *CS* circuit in Fig. 11-34.

11-7 Determine the circuit input impedance, output impedance, and voltage gain for the *CS* circuit in Fig. 11-35.

11-8 Determine the new values of input impedance, output impedance, and voltage gain for the *CS* circuit in Fig. 11-35 when a *2N5457 FET* is used and R_L is changed to 18 kΩ.

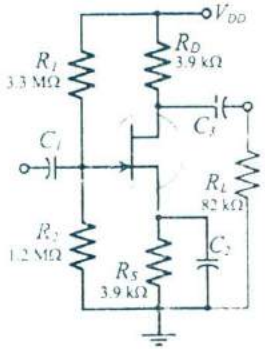


Figure 11-33

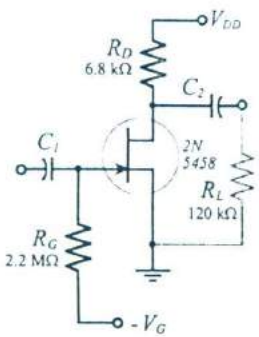


Figure 11-34

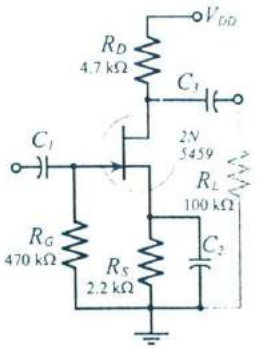


Figure 11-35

11-9 A *CS* amplifier is to have a minimum voltage gain of 12. If R_L = 150 kΩ and a *2N5459 FET* is used, determine a suitable resistance for R_D. Also, calculate the typical gain.

Section 11-4

11-10 Calculate the new values of input impedance, output impedance, and voltage gain for the circuit in Problem 11-4 when the source bypass capacitor is removed.

11-11 Calculate the new values of input impedance, output impedance, and voltage gain for the circuit in Problem 11-7 when the source bypass capacitor is removed.

11-12 The source resistor in the circuit in Problem 11-4 is replaced with two series-connected resistors (R_{S1} and R_{S2}). R_{S2} is bypassed and R_{S1} is left unbypassed. Calculate a suitable resistance for R_{S1} to give a voltage gain of 5.

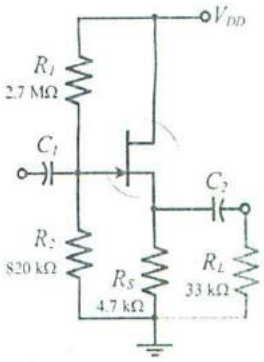


Figure 11-36

Section 11-5

11-13 The *FET* in the *CD* circuit in Fig. 11-36 has Y_{fs} = 6000 μS and r_d = 70 kΩ. Calculate the circuit input impedance, output impedance, and voltage gain.

11-14 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 11-13 when the *FET* has Y_{fs} = 3500 μS and r_d = 95 kΩ.

11-15 Determine the circuit input impedance, output impedance, and voltage gain for the *CD* circuit in Fig. 11-37.

11-16 A *CD* circuit as in Fig. 11-36 has the following components: R_1 = 2.2 MΩ, R_2 = 1 MΩ, R_S = 6.8 kΩ, R_L = 150 kΩ. The *FET* parameters are Y_{fs} = 5000 μS, and r_d = 120 kΩ. Calculate the input impedance, output impedance, and voltage gain.

11-17 Determine the typical input impedance, output impedance, and voltage gain for the *CD* circuit in Problem 11-16 when a *2N5457 FET* is used and R_L is changed to 39 kΩ.

11-18 A *CD* amplifier is to have an output impedance of approximately 200 Ω. Select a suitable *FET* from the data sheet in Appendix 1-11. If R_S = 1 kΩ, calculate the typical, minimum, and maximum values of Z_o. Also, calculate the typical voltage gain for the circuit.

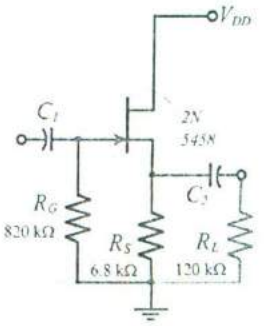


Figure 11-37

Section 11-6

11-19 The *FET* in the *CG* circuit in Fig. 11-38 has Y_{fs} = 6000 μS and r_d = 70 kΩ. Calculate the circuit input impedance, output impedance, and voltage gain.

11-20 A 120 mV *ac* signal with r_s = 300 Ω is applied as input to the *CG* circuit in Problem 11-19. Calculate the circuit *ac* output voltage.

11-21 Recalculate Z_i, Z_o, and A_v for the circuit in Problem 11-19 when the *FET* is replaced with one having Y_{fs} = 3500 μS, and r_d = 95 kΩ.

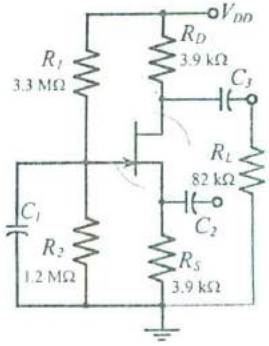


Figure 11-38

11-22 Determine the circuit input impedance, output impedance, and voltage gain for the *CG* circuit in Fig. 11-39.

11-23 Recalculate the values of input impedance, output impedance, and voltage gain for the circuit in Problem 11-22 when a *2N5457 FET* is used and R_L is changed to 18 kΩ.

11-24 Determine the input impedance, output impedance, and voltage gain for a *CG* circuit, as in Fig. 11-39, when a *2N5457 FET* is used and the resistors are: R_S = 2.2 kΩ, R_D = 3.3 kΩ, R_L = 100 kΩ.

11-25 An *ac* signal with r_s = 600 Ω is applied to the source input of the *CG* circuit in Problem 11-23. Calculate the required level of signal voltage if the *ac* output is to be 4 V.

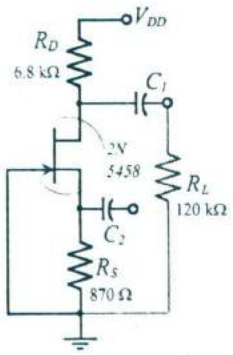


Figure 11-39

Section 11-7

11-26 The circuit in Fig. 11-40 uses a *FET* that has Y_{fs} = 5000 μS and r_d = 100 kΩ. Calculate the circuit impedances *looking into* each terminal.

11-27 A 30 mV ac signal with r_s = 300 Ω is applied to the circuit in Fig. 11-40. Determine the *ac* output voltage when the circuit is operated as: (a) a *CS* circuit with R_S bypassed, (b) a *CG* circuit with the gate bypassed to ground. The *FET* used has Y_{fs} = 7000 μS.

11-28 A *2N5458 FET* is used in a circuit with voltage divider bias and the following components: R_1 = 560 kΩ, R_2 = 390 kΩ, R_D = 3.3 kΩ, R_S = 2.7 kΩ, R_L = 68 kΩ. Calculate the impedances *looking into* the drain, source, and gate terminals. Use the *FET* typical parameters.

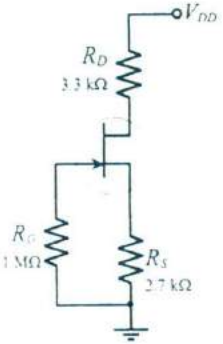


Figure 11-40

Section 11-8

11-29 The circuit in Fig. 11-40 has a *FET* with the following high-frequency parameters: Y_{fs} = 5000 μS, Y_{is} = 67 μS, Y_{os} = 50 μS, C_{iss} = 7 pF, C_{rss} = 3 pF, C_{oss} = 3 pF. Calculate the input capacitance limited cutoff frequency when the circuit is used as a *CS* amplifier with the source terminal bypassed to ground. The signal source has a 1 kΩ resistance.

11-30 Repeat Problem 11-29 for the circuit reconnected as a *CG* amplifier with the gate bypassed to ground.

11-31 The circuit in Problems 11-29 and 11-30 has 8 pF stray capacitance at the device drain terminal. Determine the output capacitance limited cutoff frequency.

11-32 The *CS* amplifier in Fig. 11-9 uses a *2N5484 JFET*. Calculate the input capacitance limited cutoff frequency for the circuit. Assume that r_s = 4.7 kΩ.

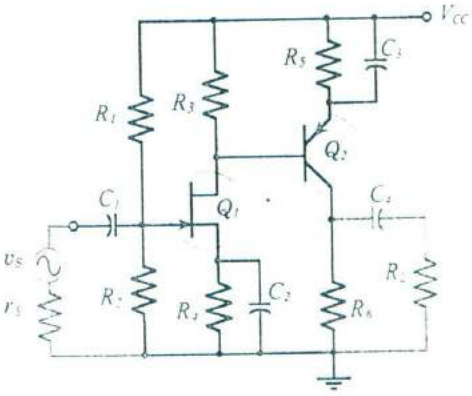
11-33 Recalculate the input capacitance limited cutoff frequency for the circuit in Problem 11-32 when it is connected to function as a *CG* circuit.

Practise Problem Answers

11-1.1 4 kΩ, 1.92 kΩ
11-3.1 1 MΩ, 1.48 kΩ, -5.5
11-3.2 470 kΩ, 3.75 kΩ, -11.25
11-4.1 1 MΩ, 1.5 kΩ, -1.3
11-4.2 848 kΩ, 2.7 kΩ, -0.89
11-5.1 194 kΩ, 232 Ω, 0.93
11-6.1 286 Ω, 240 Ω, 70 kΩ, 3.15 kΩ, 10.3, 2
11-6.2 274 Ω, 9.1
11-7.1 3.75 kΩ, 303 Ω, 230 kΩ
11-8.1 115 MHz, 6 MHz

Chapter 12

Small Signal Amplifiers



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Objectives

You will be able to:

Sketch the following small-signal amplifier circuits, explain the operation of each circuit, design each circuit for a given specification, and analyze each circuit to determine its performance:

1. *Single-stage BJT CE amplifier.*
2. *Single-stage FET CS amplifier.*
3. *Two-stage BJT CE capacitor-coupled amplifier.*
4. *Direct-coupled two-stage BJT amplifier.*
5. *Direct-coupled two-stage BJT amplifier circuits using complementary transistors.*
6. *Direct-coupled two-stage BJT amplifier with emitter-follower output stage.*
7. *DC feedback pair with CE output.*
8. *DC feedback pair with CC output.*
9. *Two-stage capacitor-coupled BIFET circuit.*
10. *Two-stage direct-coupled BIFET circuit.*
11. *Differential amplifier.*
12. *Common-base amplifier.*
13. *Cascode amplifier.*

Introduction

A *small-signal amplifier* accepts low-voltage *ac* inputs and produces amplified outputs. The *ac* outputs are also relatively low amplitude voltages, usually no larger than ±1 V. *BJT* and *FET* bias circuit design and *ac* analysis of single-stage circuits are treated in earlier chapters. So, this chapter covers the design of small-signal amplifier circuits to meet a given specification for voltage gain, load resistance, supply voltage, frequency response, etc.

A single-stage *BJT* circuit may be employed as a small-signal amplifier, but two cascaded stages give much greater amplification. For very high input impedance, a *FET* may be used as an input stage with a *BJT* as the second stage.

Calculation of circuit resistor values merely involves application of Ohm's law, after selecting suitable voltage and current levels throughout the circuit. Each capacitor value is determined in terms of the circuit lower cut-off frequency and the resistance in series with the capacitor.

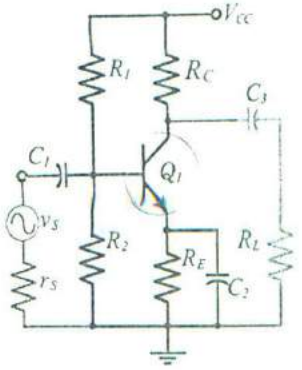


Figure 12-1
Common emitter circuit design commences with a specification for the circuit performance: voltage gain, load impedance, frequency response etc.

12-1 Single-Stage Common-Emitter Amplifier

Specification

Bias circuit design for the *CE* amplifier in Fig. 12-1 is explained in Chapter 5, and *ac* analysis of the circuit is covered in Chapter 6. Design of this circuit (or any other circuit) normally commences with a specification which might list: the supply voltage, minimum voltage gain, frequency response, signal source impedance, and the load impedance.

Selection of I_C, R_C, and R_E

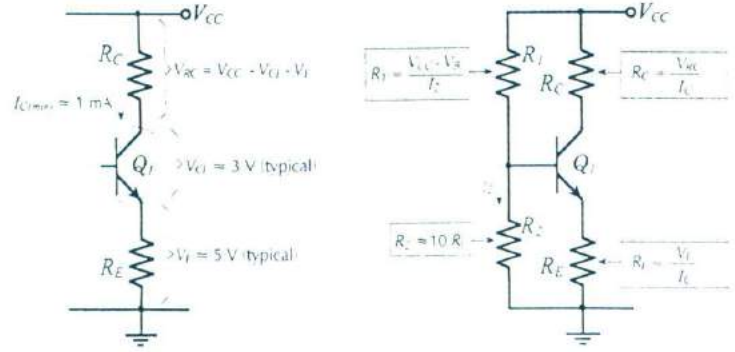
Designing for a particular voltage gain requires the use of *ac negative feedback* to stabilize the gain, (see Chapter 13). The circuit shown in Fig. 12-1 has no provision for negative feedback, consequently, it is designed to achieve the largest possible voltage gain. From Eq. 6-15, the voltage gain of a *CE* circuit is,

$$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie}} \qquad \textbf{(12-1)}$$

Because A_v is directly proportional to $R_C \| R_L$, design for the greatest voltage gain would seem to require selection of the largest possible collector resistance. However, a very large value of R_C might make the collector current too small for satisfactory transistor operation. For most small-signal transistors, I_C should not be less than 500 μA. A good minimum I_C to aim for is 1 mA. Special low-noise transistors operate with much lower collector current levels.

The transistor h_{fe} value is related to I_C, so I_C might be selected high to give the largest h_{fe}, again to achieve the greatest A_v. But, a high I_C level results in a small R_C value for a given voltage drop (V_{RC}). So, a high I_C level might actually result in a low A_v value, although h_{fe} might be relatively large.

For a given level of I_C, the largest possible voltage drop across R_C gives the greatest R_C value, ($R_C = V_{RC}/I_C$). To make V_{RC} as large as possible, V_{CE} and V_E should be held to a minimum, [see Fig. 12-2(a)]. The collector-emitter voltage should typically be around 3 V. This is large enough to ensure that the transistor operates linearly, and it also allows for a collector voltage swing of ±1 V which is usually adequate for a small-signal amplifier. Another consideration in selecting R_C is that there is nothing to be gained by making R_C larger than R_L. In fact, R_C should normally be very much smaller than R_L, so that R_L has little effect on the circuit voltage gain.



(a) Voltage and current selection (b) Resistor determinations

Figure 12-2
Voltage and current selection and resistor determination for a CE amplifier circuit.

For good bias stability, the emitter resistor voltage drop (V_E) should be much larger than the base-emitter voltage (V_{BE}), (see Section 5-7). This is because $V_E = V_B - V_{BE}$, and when $V_E >> V_{BE}$, V_E will be only slightly affected by any variation in V_{BE} (due to temperature change or other effects). Consequently, I_E and I_C remain fairly stable at $I_C \approx I_E = V_E/R_E$. A minimum V_E of 5 V gives good bias stability in most circumstances. [see Fig. 12-2 (a)]. With supply voltages less than 10 V, V_E might have to be reduced to 3 V to allow for reasonable levels of V_{CE} and V_{RC}. Normally, an emitter resistor voltage drop less than 3 V is likely to produce poor bias stability.

Once V_E, V_{CE}, and I_C are selected, V_{RC} is determined as,

$$V_{RC} = V_{CC} - V_{CE} - V_E$$

Then, R_C and R_E are calculated,

$$R_C = \frac{V_{RC}}{I_C}, \text{ and } R_E = \frac{V_E}{I_C} \text{ [see Fig. 12-2(b)]}$$

Bias Resistors

As discussed in Section 5-7, selection of the voltage divider current (I_2) as $I_C/10$ gives good bias stability and reasonably high input resistance. Where the input resistance is not important, I_2 may be made equal to I_C for excellent bias stability. The bias resistors are

calculated as,

$$R_2 = \frac{V_B}{I_2}, \text{ and } R_1 \approx \frac{V_{CC} - V_B}{I_2}$$

Selecting $R_2 = 10\ R_E$ gives $I_2 \approx I_C/10$, [Fig. 12-2(b)]. The precise level of I_2 can be calculated as $I_2 = V_B/R_2$, and this can be used in the equation for R_1.

Bypass Capacitor

All capacitors should be selected to have the smallest possible capacitance value, both to minimize the physical size of the circuit and for economy (large capacitors are the most expensive). Because each capacitor has its highest impedance at the lowest operating frequency, the capacitor values are calculated at the lowest signal frequency that the circuit is required to amplify. This frequency is the circuit *lower cutoff frequency*, or *low 3 dB frequency* (f_1), (see Fig. 12-3 reproduced from Fig. 8-5).

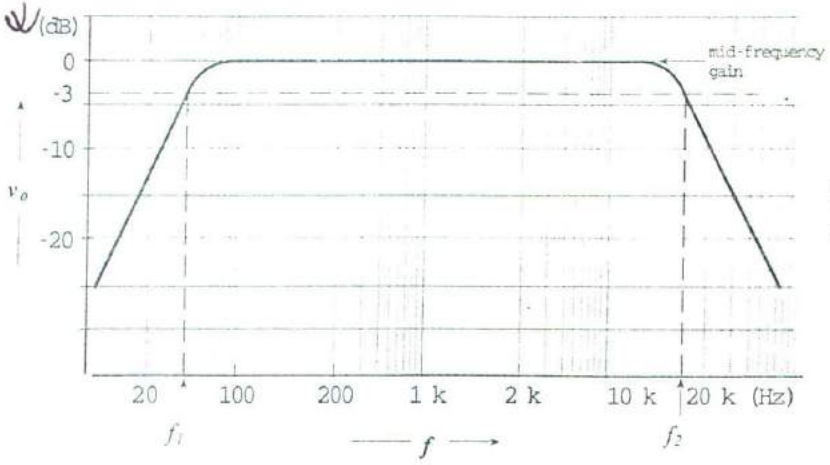


Figure 12-3
Typical frequency response for a transistor amplifier.

Bypass capacitor C_2 in Fig. 12-1 is normally the largest capacitor in the circuit, so C_2 is selected to set f_1 at the desired frequency. Equation 6-21 (for voltage gain) was developed for a *CE* circuit with an unbypassed emitter resistor (R_E). Rewriting the equation to include X_{C2} in parallel with R_E gives

$$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + (1 + h_{fe})(R_E \| X_{C2})}$$

Normally $R_E >> X_{C2}$, so R_E can be omitted. Also, X_{C2} is capacitive,

so,
$$A_v = \frac{-h_{fe}(R_C \| R_L)}{\sqrt{[h_{ie}^2 + [(1 + h_{fe})(X_{C2})]^2}}$$

When $h_{ie} = (1 + h_{fe})\, X_{C2}$,

$$|A_v| = \frac{-h_{fe}(R_C \| R_L)}{h_{ie}\sqrt{(1^2 + 1^2)}} = \frac{\text{mid-frequency gain}}{\sqrt{2}}$$

$$= (\text{mid-frequency gain}) - 3\ \text{dB}$$

Therefore, at f_1,

$$h_{ie} = (1 + h_{fe})\, X_{C2}$$

or,
$$\mathbf{X_{C2} = \frac{h_{ie}}{1 + h_{fe}}\ \text{at}\ f_1} \qquad \textbf{(12-2)}$$

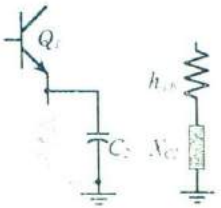


Figure 12-4
In a CE amplifier circuit, the signal voltage can be divided across the emitter bypass capacitor and the emitter resistance (h_{ie}).

From Table 6-1 (in Section 6-3),

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}} = (\text{impedance 'looking into' the emitter})$$

So,
$$\mathbf{X_{C2} = h_{ib}\ \text{at}\ f_1} \qquad \textbf{(12-3)}$$

At f_1, X_{C2} = (impedance 'looking into' the emitter)
= (impedance in *series* with X_{C2}). (see Fig. 12-4)

Equations 12-2 and 12-3 give the smallest value for the bypass capacitor. When selecting a standard value for the capacitor, the next larger value should be chosen. This will give a cutoff frequency slightly lower than the f_1 value used in the calculations.

It is important to note that the emitter bypass capacitor is calculated in terms of the resistance 'seen looking into' the transistor emitter terminal (the resistance in series with C_2). The capacitor value is *not* determined in relation to the value of the emitter resistor (R_E). Example 12-1 demonstrates the results of correct and incorrect bypass capacitor selection.

Example 12-1

The circuit shown in Fig. 12-5 uses a transistor with $h_{fe} = 50$, $h_{ie} = 1\ \text{k}\Omega$, and $h_{ib} = 20\ \Omega$. The circuit lower cutoff frequency (f_1) is to be 100 Hz. Calculate the following quantities:

(a) The required capacitance for C_2.
(b) A_v with the emitter terminal completely bypassed to ground.
(c) A_v at $f = 100$ Hz, using the selected C_2 value.
(d) A_v at $f = 100$ Hz when C_2 is (incorrectly) selected as $X_{C2} = R_E/10$.

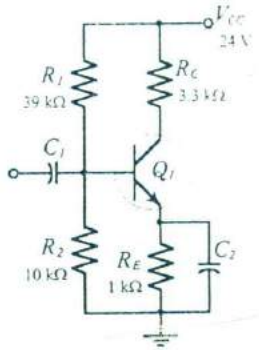


Figure 12-5
Common-emitter circuit for Example 12-1.

Solution

(a) C_2 determination:

Eq. 12-3, $X_{C2} = h_{ib} = 20\ \Omega$

$$C_2 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2 \times 100\ \text{Hz} \times 20\ \Omega}$$

$$= 79.6\ \mu\text{F}\ \ (\text{use } 80\ \mu\text{F standard value})$$

(b) Voltage gain:

Eq. 6-15, $$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie}} = \frac{-50 \times 3.3\ \text{k}\Omega}{1\ \text{k}\Omega}$$

$$= -165$$

(c) A_v at 100 Hz:

at $f = 100$ Hz, $X_{C2} = 20\ \Omega$

Eq. 12-1, $$A_{v(1)} = \frac{-h_{fe}(R_C \| R_L)}{\sqrt{\{h_{ie}^2 + [(1 + h_{fe})X_{C2}]^2\}}}$$

$$= \frac{-50 \times 3.3\ \text{k}\Omega}{\sqrt{\{(1\ \text{k}\Omega)^2 + [(1 + 50) \times 20\ \Omega]^2\}}}$$

$$= -116 = A_v/\sqrt{2}$$

(d) A_v at 100 Hz when $X_{C2} = R_E/10$:

from Eq. 12-1, $$A_{v(x)} = \frac{-h_{fe}(R_C \| R_L)}{\sqrt{\{h_{ie}^2 + [(1 + h_{fe})(R_E/10)]^2\}}}$$

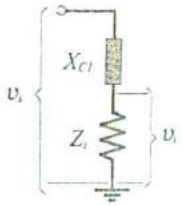
$$= \frac{-50 \times 3.3\ \text{k}\Omega}{\sqrt{\{(1\ \text{k}\Omega)^2 + [(1 + 50) \times (1\ \text{k}\Omega/10)]^2\}}}$$

$$= -31.7$$

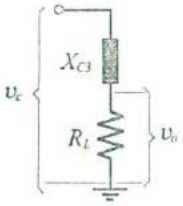
In Ex. 12-1 the circuit voltage gain is -165 when the emitter terminal is completely bypassed to ground. This is the mid-frequency gain (A_v) for the amplifier. With a correctly selected bypass capacitor, the voltage gain ($A_{v(1)}$) at a signal frequency of 100 Hz is -116. This is $1/\sqrt{2}$ times the mid-frequency gain, or 3 dB below the mid-frequency gain, which is to be expected because the bypass capacitor is selected to give a 3 dB gain reduction at 100 Hz. When the impedance of the bypass capacitor is *incorrectly* selected as $R_E/10$, the voltage gain ($A_{v(x)}$) at 100 Hz is much smaller than the required $A_v/\sqrt{2}$.

Coupling Capacitors

The coupling capacitors (C_1 and C_3 in Fig. 12-1) should have a negligible effect on the frequency response of the circuit. Figure 12-6(a) illustrates the fact that X_{C1} and Z_i constitute a voltage divider. If X_{C1} is too large, the circuit *ac* input voltage (v_i) will be significantly smaller than the signal voltage (v_s). Similarly, X_{C3} and R_L attenuate the *ac* voltage at the transistor collector, so that the *ac* output voltage (v_o) can be smaller than the *ac* collector voltage (v_c). [Fig. 12-6(b)]. To minimize the effects of C_1 and C_3, the reactance of each coupling capacitor is selected to be approximately equal to one-tenth of the impedance in series with it at the lowest operating frequency for the circuit (f_l).



(a) The signal voltage is divided across X_{C1} and Z_i



(b) The collector *ac* voltage is divided across X_{C3} and R_L

Figure 12-6
Input and output voltages can be divided across coupling capacitors and input or load resistances.

$$X_{C1} = \frac{Z_i + r_s}{10} \text{ at } f_1 \qquad (12\text{-}4)$$

$$X_{C3} = \frac{Z_o + R_L}{10} \text{ at } f_1 \qquad (12\text{-}5)$$

Usually, $R_L >> Z_o$, and often $Z_i >> r_s$, so that Z_o and r_s can be omitted in Equations 12-4 and 12-5. Once again, the equations give minimum capacitance values, so that the next larger standard values should always be selected for C_1 and C_3.

Equations 12-4 and 12-5 give an impression that approximately 10% of the signal and output voltages are lost across C_1 and C_3. This would be true if the quantities were resistive. However, X_{C1} and X_{C3} are capacitive while Z_i and R_L are usually resistive. So, when the actual loss is calculated, it is found to be only around 0.5% for each capacitor.

Another approach to the selection of coupling capacitors is to make $X_{C1} = Z_i$ at two octaves below f_1.

$$X_{C1} = Z_i \text{ at } f_1/4 \qquad (12\text{-}6)$$

The output coupling capacitor is then determined by making impedance of C_3 equal to R_L at two octaves below $f_1/4$.

$$X_{C3} = R_L \text{ at } f_1/16 \qquad (12\text{-}7)$$

When Equations 12-6 and 12-7 are used to determine the values of the coupling capacitors, it can be shown that the capacitor attenuation effects are less than 5% of A_v.

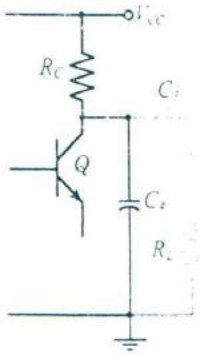


Figure 12-7
A shunting capacitor can be used at the output of a common-emitter circuit to select the upper 3 dB frequency.

Shunting Capacitor

Sometimes an amplifier is required to have a particular *upper cutoff frequency*, (f_2 in Fig. 12-3). The transistor must be selected to have a much higher cutoff frequency than f_2, (see Section 8-3). The upper cutoff frequency for the circuit can then be set by connecting a small capacitor from the transistor collector terminal to ground, (C_4 in Fig. 12-7). The effect of shunt capacitance at the transistor collector is discussed in Section 8-4.

Design Calculations

Example 12-2

Calculate suitable resistor values for the CE amplifier in Fig. 12-8.

Solution

$$R_C << R_l$$

select $$R_C = \frac{R_l}{10} = \frac{120\ \text{k}\Omega}{10}$$

$$= 12\ \text{k}\Omega \text{ (standard value)}$$

select $V_E = 5$ V, and $V_{CE} = 3$ V

$$V_{RC} = V_{CC} - V_{CE} - V_E = 24\text{ V} - 3\text{ V} - 5\text{ V}$$
$$= 16\text{ V}$$

$$I_C = \frac{V_{RC}}{R_C} = \frac{16\text{ V}}{12\text{ k}\Omega}$$
$$= 1.3\text{ mA}$$

$$R_E = \frac{V_E}{I_C} = \frac{5\text{ V}}{1.3\text{ MA}}$$
$$= 3.75\text{ k}\Omega$$ (Use a 3.9 kΩ standard value to make I_C a little less than the design level, thus ensuring that V_{CE} is not less than 3 V.)

$$R_2 = 10\,R_E = 10 \times 3.9\text{ k}\Omega$$
$$= 39\text{ k}\Omega \text{ (standard value)}$$

$$I_2 = \frac{V_E + V_{BE}}{R_2} = \frac{5\text{ V} + 0.7\text{ V}}{39\text{ k}\Omega}$$
$$\approx 146\,\mu\text{A}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{24\text{ V} - 5.7\text{ V}}{146\,\mu\text{A}}$$
$$\approx 125\text{ k}\Omega$$ (use 120 kΩ standard value)

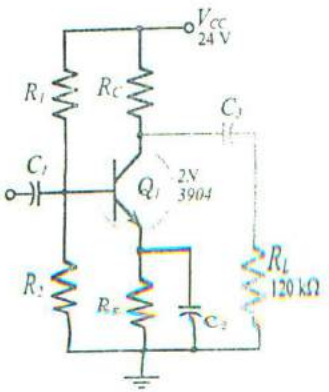


Figure 12-8
Common-emitter amplifier for Example 12-2.

Example 12-3

Determine suitable capacitor values for the *CE* amplifier in Ex. 12-2. The signal source resistance is 600 Ω, and the lower cutoff frequency is to be 100 Hz.

Solution

From Appendix 1-5, for the *2N3904:*

$h_{fe} = 100$, and $h_{ie} = 1$ kΩ

Eq. 12-2, $$X_{C2} = \frac{h_{ie}}{1 + h_{fe}} = \frac{1\text{ k}\Omega}{1 + 100}$$
$$\approx 10\,\Omega$$

$$C_2 = \frac{1}{2\,\pi\,f_1\,X_{C2}} = \frac{1}{2\,\pi \times 100\text{ Hz} \times 10\,\Omega}$$
$$= 159\,\mu\text{F}$$ (use 180 μF standard value)

$$Z_i = R_1 \| R_2 \| h_{ie} = 120\text{ k}\Omega \| 39\text{ k}\Omega \| 1\text{ k}\Omega$$
$$= 967\,\Omega$$

from Eq. 12-4, $$C_1 = \frac{1}{2\,\pi\,f_1\,(Z_i + r_s)/10}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times (967\ \Omega + 600\ \Omega)/10}$$

$$= 10.1\ \mu\text{F} \quad \text{(use 10 } \mu\text{F standard value)}$$

from Eq. 12-5, $$C_3 = \frac{1}{2\pi f_1 (R_C + R_L)/10}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times (12\ \text{k}\Omega + 120\ \text{k}\Omega)/10}$$

$$= 0.12\ \mu\text{F} \quad \text{(standard value)}$$

The complete Common-source circuit designed in Examples 12-2 and 12-3 is shown in Fig. 12-9.

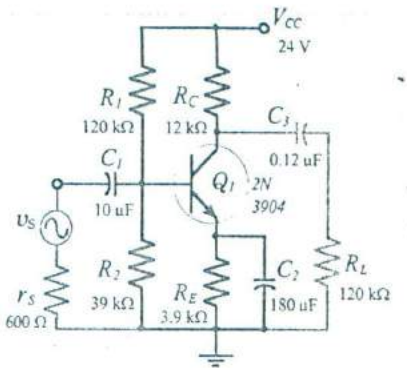


Figure 12-9
CE amplifier circuit designed in Examples 12-2 and 12-3.

Practise Problems

12-1.1 Determine suitable resistor values for a CE amplifier (see Fig. 12-9) that uses a 20 V supply and has a 68 kΩ capacitor-coupled load.

12-1.2 Determine suitable capacitor values for the circuit in Problem 12-1.1 to have a 40 Hz lower cutoff frequency and to use a 2N3903 transistor. Assume that $r_s = 500\ \Omega$.

12-2 Single-Stage Common-Source Amplifier

Specification

Bias circuit design for the common-source amplifier in Fig. 12-10 is treated in Chapter 10, and *ac* analysis of *FET* circuits is covered in Chapter 11. As with the common-emitter *BJT* circuit in Section 12-1, design commences with specification of the supply voltage, amplification, frequency response, load impedance, etc.

Selection of I_D, R_D, and R_S

The circuit shown in Fig. 12-10 has no provision for negative feedback, so, it should be designed to achieve the largest possible gain. From Eq. 11-7, the voltage gain of a CS circuit is,

$$A_v = -Y_{fs}(R_D \| R_L)$$

Because A_v is directly proportional to $R_D \| R_L$, design for the greatest voltage gain normally requires selection of the largest possible drain resistance. However, a very large value of R_D might make the drain current too small for satisfactory *FET* operation. Also, low I_D levels give small Y_{fs} values, which result in lower *ac* voltage gain. Furthermore, R_D should normally be much smaller than R_L, so that R_L has little effect on the circuit voltage gain.

For a given level of I_D, the largest possible voltage drop across R_D gives the greatest R_D value, ($R_D = V_{RD}/I_D$). To make V_{RD} as large as possible, V_{DS} and V_S should be held to a minimum, [see Fig. 12-

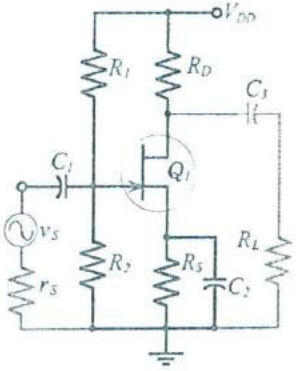


Figure 12-10
Common source circuit design commences with a specification for the circuit performance.

11(a)]. The drain-source voltage should typically be $V_{DS(min)} = (V_{p(max)} + 1\ V)$. This is large enough to ensure that the *FET* operates in the pinch-off region of its characteristics. It also allows for a drain voltage swing of ±1 V, which is usually adequate for a small-signal amplifier. If the gate-source bias voltage (V_{GS}) is other than zero, then, as illustrated in Fig. 12-11(a), the minimum V_{DS} should be calculated as,

$$V_{DS(min)} = V_{p(max)} + 1\ V - V_{GS} \qquad (12\text{-}8)$$

Recall from Chapter 10 that for good bias stability, the source resistor voltage drop (V_S) should be as large as possible. Where the supply voltage is small, V_S may be reduced to a minimum to allow for the minimum level of V_{DS}. A reasonable approach for most *FET* circuits is to calculate the the sum of V_S and V_{RD} from,

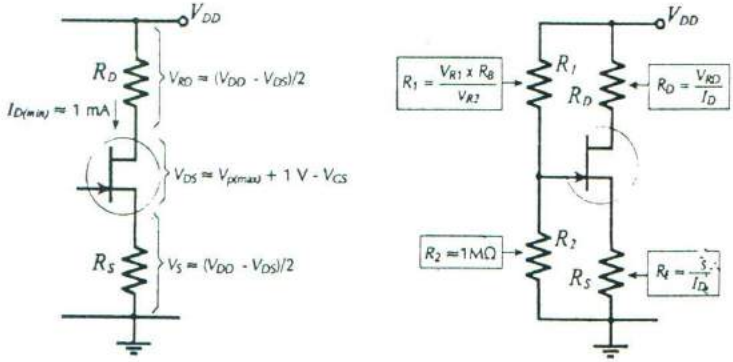
$$V_S + V_{RD} = V_{DD} - V_{DS(min)}$$

and then make,

$$V_S = V_{RD} = \frac{V_{DD} - V_{DS(min)}}{2} \qquad (12\text{-}9)$$

Once V_S, V_{RD}, and I_D are selected, R_D and R_S are calculated,

$$R_D = \frac{V_{RD}}{I_D}, \text{ and } R_S = \frac{V_S}{I_D} \text{ [see Fig. 12-11(b)]}$$



(a) Voltage and current selection (b) Resistor determination

Figure 12-11
Voltage and current selection and resistor determination for a CS amplifier circuit.

As already discussed in Section 10-4, a bias line should be drawn upon the *FET* transfer characteristics to determine a suitable gate bias voltage (V_G). The selected maximum drain current ($I_{D(max)}$) is plotted on the maximum transfer characteristics for the *FET* used. The bias line is then drawn through this point with a slope of $1/R_S$. The gate bias voltage is read from the intersection of the bias line and the V_G scale. As an alternative to drawing the bias line, V_{GS} can be read from the transfer characteristic when $I_{D(max)}$ is plotted. Then,

$$V_G = V_S - V_{GS}$$

Instead of using the *FET* transfer characteristics, $V_{P(max)}$ and $I_{DSS(max)}$ can be substituted into Eq. 10-8 to calculate the V_{GS} level.

Bias Resistors

With a voltage divider bias circuit [as in Fig. 12-11(b)], R_2 is usually selected as 1 MΩ or less. Smaller resistance values may be used where a lower input impedance is acceptable. Larger resistance values may also be used, however, as discussed in Section 10-7, there are distinct disadvantages to using resistances higher than 1 MΩ. With R_2 determined, R_1 is calculated using R_2 and the ratio of V_{R1} to V_{R2}.

$$R_1 = \frac{V_{R1} \times R_2}{V_{R2}} \qquad \textbf{(12-10)}$$

Capacitors

As for a *BJT* capacitor-coupled circuit, coupling and bypass capacitors should be selected to have the smallest possible capacitance values. The largest capacitor in the circuit (source bypass capacitor C_2 in Fig 12-10) sets the circuit low 3 dB frequency (f_1). Equation 11-10 was developed for the voltage gain of a common-source circuit with an unbypassed source resistor (R_S). Rewriting the equation to include X_{C2} in parallel with R_S gives

$$A_v = \frac{-Y_{fs}(R_D \| R_L)}{1 + Y_{fs}(R_S \| X_{C2})}$$

Normally $R_S >> X_{C2}$, so R_S can be omitted. Also, X_{C2} is capacitive,

so, $$A_v = \frac{-Y_{fs}(R_D \| R_L)}{\sqrt{[1^2 + (Y_{fs} X_{C2})^2]}} \qquad \textbf{(12-11)}$$

When $Y_{fs} X_{C2} = 1$,

so, $$|A_v| = \frac{-Y_{fs}(R_D \| R_L)}{\sqrt{(1^2 + 1^2)}} = \frac{\text{mid-frequency gain}}{\sqrt{2}}$$

$$= \text{(mid-frequency gain) - 3 dB}$$

Therefore, at f_1,

$$Y_{fs} X_{C2} = 1$$

or, $$X_{C2} = \frac{1}{Y_{fs}} \text{ at } f_1 \qquad \textbf{(12-12)}$$

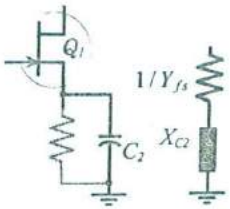


Figure 12-12
In a CS amplifier circuit, the signal voltage can be divided across the source bypass capacitor and the source resistance ($1/Y_{fs}$).

From Section 11-7,

$$Z_S = \frac{1}{Y_{fs}} = \text{(impedance 'looking into' the } \textit{FET} \text{ source)}$$

So, at f_1, X_{C2} = (impedance 'looking into' the source terminal)
= (impedance in *series* with X_{C2}), (see Fig. 12-12)

Equations 12-12 gives the smallest value for the source bypass capacitor. When selecting a standard value, the next larger capacitance value should be chosen. This will give a cutoff frequency slightly lower than the f_l value used in the calculations.

As explained in Section 12-1, it is important to note that the bypass capacitor is calculated in terms of the resistance *seen looking into* the device terminal (the resistance in series with C_2). *The capacitance value is* **not** *determined in terms of the parallel resistor* (R_S).

The input and output coupling capacitors should have almost zero effect on the circuit frequency response. In Section 12-1 it is explained that X_{C1} in series with Z_i and X_{C3} in series with R_L constitute voltage dividers that can attenuate the ac input and output voltages. To minimize the attenuation, the reactance of each coupling capacitor is selected to be approximately one-tenth of the impedance in series with it at the lowest operating frequency for the circuit (f_l). Equations 12-4 and 12-5 apply once again for the calculation of the minimum C_1 and C_2 values.

Eq. 12-4. $$X_{C1} = \frac{Z_i + r_s}{10} \text{ at } f_l$$

Eq. 12-5. $$X_{C2} = \frac{Z_o + R_L}{10} \text{ at } f_l$$

As in *BJT* circuits, R_L is usually much larger than Z_o, and Z_i is often much larger than r_s, so Z_o and r_s can be omitted in Equations 12-4 and 12-5. As always, the equations give minimum capacitance values, so that the next larger standard values should always be selected for C_1 and C_3.

Alternatively, as discussed in Section 12-1, Equations 12-6 and 12-7 may be used for determining coupling capacitor values.

Design Calculations

Example 12-4

Calculate suitable resistor values for the common-source circuit in Fig. 12-13.

Solution

Refer to the *2N5459* transfer characteristics in Fig. 9-19. A reasonable level of $I_{D(max)}$ might be 1.5 mA. Y_{fs} becomes smaller at lower I_D levels.

Eq. 10-8, $$V_{GS} = V_P[1 - \sqrt{(I_D/I_{DSS})}]$$

Using $V_{P(max)}$ and $I_{DSS(max)}$ from Appendix 1-11, (and from Fig. 9-19)

$$V_{GS} = 8\text{ V}\,[1 - \sqrt{(1.5\text{ mA}/16\text{ mA})}]$$
$$= 5.6\text{ V}$$

Eq. 12-8, $$V_{DS(min)} = V_{P(max)} + 1\text{ V} - V_{GS} = 8\text{ V} + 1\text{ V} - 5.6\text{ V}$$
$$= 3.4\text{ V}$$

Eq. 12-9, $$V_S = V_{RD} = \frac{V_{DD} - V_{DS(min)}}{2} = \frac{24\text{ V} - 3.4\text{ V}}{2}$$

$$= 10.3\text{ V}$$

$$R_S = R_D = \frac{V_{RD}}{I_D} = \frac{10.3\text{ V}}{1.5\text{ mA}}$$

$$= 6.87\text{ k}\Omega \text{ (use 6.8 k}\Omega\text{ standard value)}$$

R_D should be $<< R_L$

6.8 kΩ << 120 kΩ

$$V_{R2} = V_G = V_S - V_{GS} = 10.3\text{ V} - 5.5\text{ V}$$
$$= 4.8\text{ V}$$

$$V_{R1} = V_{DD} - V_G = 24\text{ V} - 4.8\text{ V}$$
$$= 19.2\text{ V}$$

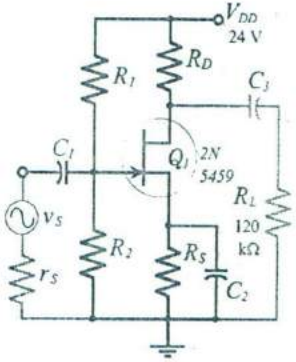


Figure 12-13
Common source amplifier circuit for Ex. 12-4.

select $R_2 = 1\text{ M}\Omega$

Eq. 12-10, $$R_1 = \frac{V_{R1} \times R_2}{V_{R2}} = \frac{19.2\text{ V} \times 1\text{ M}\Omega}{4.8\text{ V}}$$

$= 4\text{ M}\Omega$ (Use 4.7 MΩ standard value to ensure that V_G is slightly lower than the design level. This will give a lower level of I_D and a higher V_{DS} than the minimum design level.)

Example 12-5

Determine suitable capacitor values for the common-source amplifier in Ex. 12-4. The signal source resistance is 600 Ω, and the lower cutoff frequency is to be 100 Hz.

Solution

From Appendix 1-11, for the *2N5459:*

$$Y_{fs(max)} = 6000\,\mu\text{S}$$

Eq. 12-12, $$X_{C2} = \frac{1}{Y_{fs}} = \frac{1}{6000\,\mu\text{S}}$$

$$\approx 167\,\Omega$$

$$C_2 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2\pi \times 100\text{ Hz} \times 167\,\Omega}$$

$= 9.5\,\mu\text{F}$ (use 10 μF standard value)

$$Z_i = R_1 \| R_2 = 4.7\text{ M}\Omega \| 1\text{ M}\Omega$$
$$= 825\text{ k}\Omega$$

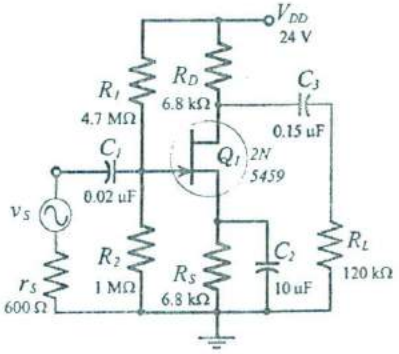


Figure 12-14
Common source circuit designed in Examples 12-4 and 12-5.

from Eq. 12-4, $$C_1 = \frac{1}{2\pi f_1 (Z_i + r_s)/10}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times (825\ \text{k}\Omega + 600\ \Omega)/10}$$

$$= 0.019\ \mu\text{F} \qquad \text{(use 0.02 } \mu\text{F standard value)}$$

from Eq. 12-5, $$C_3 = \frac{1}{2\pi f_1 (R_D + R_L)/10}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times (6.8\ \text{k}\Omega + 120\ \text{k}\Omega)/10}$$

$$= 0.13\ \mu\text{F} \qquad \text{(use 0.15 } \mu\text{F standard value)}$$

Practise Problems

12-2.1 A common-source amplifier (see Fig. 12-13) is to use a *2N5458 FET* and a 25 V supply. The external load is 100 kΩ. Determine suitable resistor values for the circuit.

12-2.2 Determine suitable capacitor values for the circuit in Problem 12-2.1 to give a 30 Hz lower cutoff frequency.

12-3 Capacitor-Coupled Two-Stage CE Amplifier

Circuit

A capacitor-coupled two-stage amplifier circuit is shown in Fig. 12-15. Each stage is similar to the single-stage circuit in Fig. 12-9. *Stage-1* is capacitor-coupled (via C_3) to the input of *Stage-2*. The signal is applied to the input of *Stage-1*, and the load is coupled to the output of *Stage-2*. The signal is amplified by *Stage-1*, and the output of *Stage-1* is amplified by *Stage-2*, so that the overall voltage gain is much greater than the gain of a single stage. As illustrated by the circuit waveforms in Fig. 12-16, the signal voltage is phase-shifted through 180° by *Stage-1*, and through a further 180° by *Stage-2*. Consequently, the overall phase shift from input to output is zero (or 360°).

Circuit Design

The simplest approach to design of this circuit is to make each stage identical. Then, when *Stage-2* has been designed, the components for *Stage-1* are selected as: $R_1 = R_5$, $R_2 = R_6$, $R_3 = R_7$, $R_4 = R_8$, $C_1 = C_3$, and $C_2 = C_4$. Note that C_3 is calculated in terms of the input resistance to *Stage-2*, which should be identical to that for *Stage-1* if the stages are otherwise identical. C_5 is calculated in the usual way for an output coupling capacitor.

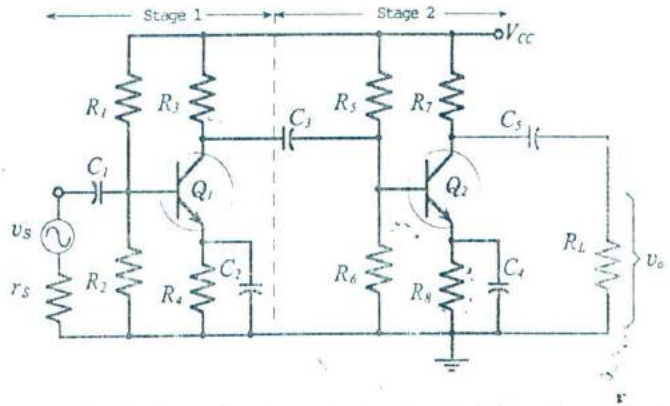


Figure 12-15
A two-stage capacitor-coupled CE amplifier consists of two similar CE circuits with capacitor-coupling between stages.

One way the design of a two-stage circuit differs from that of a single-stage circuit is in determination of emitter bypass capacitors C_2 and C_4. Consider Eq. 12-2, which was derived to calculate a bypass capacitor value to make the voltage gain of a single-stage circuit 3 dB down from the mid-frequency gain at the selected lower cutoff frequency (f_1).

$$X_C = \frac{h_{ie}}{1 + h_{fe}} \text{ at } f_1$$

If this equation is used to calculate the capacitance of C_2 and C_4 in the two-stage circuit, it is found that the gain of *Stage 1* is down by 3 dB at f_1, and the gain of *Stage 2* is also down by 3 dB at f_1, (see Fig. 12-17). This means that the overall gain of the circuit is down by a total of 6 dB at frequency f_1. For a 3 dB decrease in overall voltage gain at f_1, the bypass capacitors must be calculated to give a 1.5 dB reduction in the gain of each stage. A 1.5 dB reduction in stage gain at f_1, is achieved by making the reactance of the emitter bypass capacitor equal to 0.65 times the impedance in series with the capacitor. Thus, the equation for the bypass capacitor impedance now becomes,

$$\mathbf{X_{C2} = X_{C4} = \frac{0.65\ h_{ie}}{1 + h_{fe}} \text{ at } f_1} \qquad \textbf{(12-13)}$$

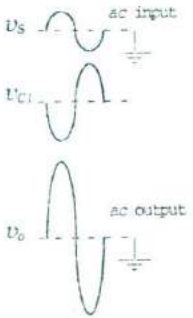


Figure 12-16
Voltage waveforms for a two stage CE circuit.

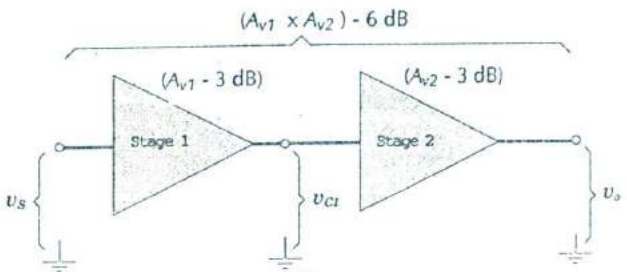


Figure 12-17
If the voltage gain of each stage o a two-stage circuit is down by 3 dB at f_1 the overall voltage gain i down by 6 dB.

Example 12-6

Design a two-stage capacitor-coupled amplifier, as shown in Fig. 12-15, to fulfil the specification used for Examples 12-2 and 12-3: *2N3904* transistors, $V_{CC} = 24$ V, $R_L = 120$ kΩ, $f_1 = 100$ Hz.

Solution

Except for the emitter bypass capacitors, each stage is designed exactly as in Examples 12-2 and 12-3. Therefore, $R_3 = R_7 = 12$ kΩ, $R_4 = R_8 = 3.9$ kΩ, $R_1 = R_5 = 120$ kΩ, $R_2 = R_6 = 39$ kΩ, $C_1 = C_3 = 10\ \mu$F, $C_5 = 0.12\ \mu$F.

From Appendix 1-5, for the *2N3904*: $h_{fe} = 100$, and $h_{ie} = 1$ kΩ

Eq. 12-13,
$$X_{C4} = \frac{0.65\, h_{ie}}{1 + h_{fe}} = \frac{0.65 \times 1\ \text{k}\Omega}{1 + 100}$$

$$\approx 6.4\ \Omega$$

$$C_2 = C_4 = \frac{1}{2\pi f_1 X_{C4}} = \frac{1}{2\pi \times 100\ \text{Hz} \times 6.4\ \Omega}$$

$$= 249\ \mu\text{F} \qquad \text{(use 250 } \mu\text{F standard value)}$$

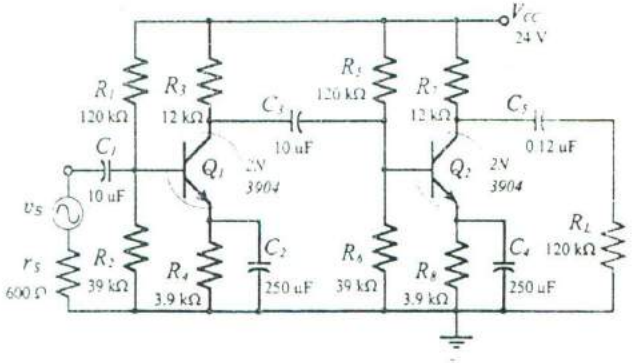


Figure 12-18
Two-stage capacitor-coupled CE circuit designed in Example 12-6.

Circuit Analysis

Ac analysis of a two-stage, capacitor-coupled circuit is similar to analysis of single-stage circuits, as covered in Chapter 6. The *h*-parameter equivalent circuit for the amplifier circuit in Fig. 12-15 is drawn in Fig. 12-19. Once again, this equivalent circuit is produced by replacing the supply voltage and all capacitors with short circuits, and substituting device h-parameter models for each transistor. The resultant equivalent circuit simply consists of two single-stage *h*-parameter equivalent circuits. As always, voltage polarities and current directions are indicated for an instantaneous positive-going signal voltage. The voltage polarities show a 180° phase shift between v_i and v_{c1}, and a further 180° phase shift between v_{C1} and v_o.

The performance equations for the two-stage circuit are readily derived from the equations for a single-stage circuit. Input and output impedance are exactly the same as for the single-stage circuit:

$$Z_i = R_1 \| R_2 \| h_{ie} \qquad \textbf{(12-14)}$$

$$Z_o \approx R_7 \qquad \textbf{(12-15)}$$

The voltage gain equation for the second stage is exactly the same as the single-stage gain equation. The capacitor-coupled load at the collector terminal of the first stage is the input impedance of the second stage. So the voltage gain equations are,

$$A_{v1} = \frac{-h_{fe1}\,(R_3 \| Z_{i2})}{h_{ie1}} \qquad \textbf{(12-16)}$$

and,

$$A_{v2} = \frac{-h_{fe2}\,(R_7 \| R_L)}{h_{ie2}} \qquad \textbf{(12-17)}$$

The overall voltage gain is found by multiplying the two individual stage gains:

$$A_v = A_{v1} \times A_{v2} \qquad \textbf{(12-18)}$$

Equations for current gain and power gain can also be derived from the single-stage equations, but these quantities are normally not important.

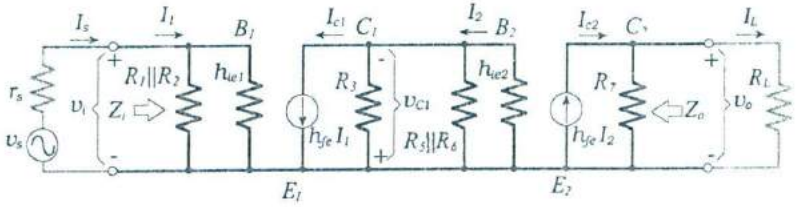


Figure 12-19
The h-parameter equivalent circuit for a two-stage CE amplifier is drawn by cascading the equivalent circuits for each stage.

Example 12-7

Analyze the two-stage amplifier circuit designed in Example 12-6 to determine its input impedance, output impedance, and minimum overall voltage gain.

Solution

Eq. 12-14, $Z_i = R_1 \| R_2 \| h_{ie} = 120\ \text{k}\Omega \| 39\ \text{k}\Omega \| 1\ \text{k}\Omega$
$= 967\ \Omega$

Eq. 12-15, $Z_o \approx R_7 = 12\ \text{k}\Omega$

From Eq. 12-14, $Z_{i2} = R_5 \| R_6 \| h_{ie2} = 120\ \text{k}\Omega \| 39\ \text{k}\Omega \| 1\ \text{k}\Omega$
$= 967\ \Omega$

Eq. 12-16. $$A_{v1} = \frac{-h_{fe1}(R_3 \| Z_{i2})}{h_{ie1}} = \frac{-100 \times (12\ \text{k}\Omega \| 967\ \Omega)}{1\ \text{k}\Omega}$$

$$\approx -89$$

Eq. 12-17. $$A_{v2} = \frac{-h_{fe2}(R_4 \| R_L)}{h_{ie2}} = \frac{-100 \times (12\ \text{k}\Omega \| 120\ \text{k}\Omega)}{1\ \text{k}\Omega}$$

$$= -1090$$

Eq. 12-18. $$A_v = A_{v1} \times A_{v2} = (-89) \times (-1090)$$

$$= 97\,000$$

Practise Problems

12-3.1 Determine suitable resistor values for a capacitor-coupled two-stage CE amplifier with a 15 V supply and a 82 kΩ external load.

12-3.2 Determine suitable capacitor values for the circuit in Problem 12-3.1. The circuit uses 2N3903 BJTs, the lower cutoff frequency is 50 Hz, and the signal source resistance is 1 kΩ.

12-3.3 Calculate the overall voltage gain for the circuit in Problems 12-3.1 and 12-3.2.

12-4 Direct-Coupled Two-Stage Circuits

Direct-Coupled Circuit

For economy, the number of components used in any circuit should be kept to a minimum. The use of direct coupling between stages is one way of eliminating components. Figure 12-20 shows a circuit that has the base of transistor Q_2 directly coupled to the collector of Q_1. Comparing this to the capacitor-coupled circuit in Fig. 12-15, it is seen that the two bias resistors for *Stage 2* and the interstage coupling capacitor have been eliminated. This is a saving of only three components, however, the total savings can be considerable when many similar circuits are to be manufactured.

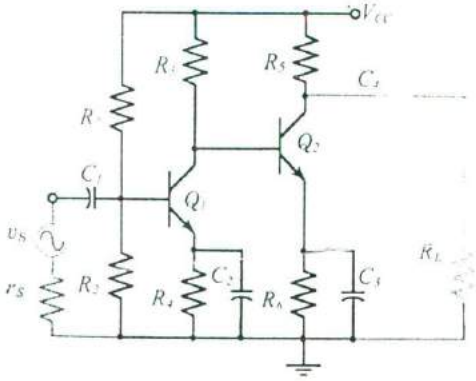


Figure 12-20
Two-stage direct-coupled CE amplifier. Because Q_2 base is directly coupled to Q_1 collector, the inter-stage coupling capacitor and the bias resistors for Q_2 are eliminated.

Circuit Design

The first step in the design of the circuit in Fig. 12-20 involves determining a suitable level of base bias voltage for Q_2. This is done by estimating satisfactory levels of V_{E1} and V_{CE1} for transistor Q_1. Then,

$$V_{B2} = V_{C1} = V_{E1} + V_{CE1}$$

$$V_{E2} = V_{B2} - V_{BE}$$

and,

$$V_{R5} = V_{CC} - V_{E2} - V_{CE2}$$

As discussed in Section 12-1, appropriate *dc* voltage levels for small-signal amplifiers are V_{CE} = 3 V and V_E = 5 V, except in the case of a very low supply voltage.

As for all amplifier circuits, the resistor at the collector of the output transistor (R_5 in Fig. 12-20) should be much smaller than the external load resistor. Once R_5 is selected, I_{C2} can be calculated using the voltage V_{R5} already determined. If I_{C2} looks too small for satisfactory operation of the transistor, a suitable current level should be selected and a new value of R_5 calculated. The collector current of Q_1 is determined by making I_{C1} very much greater than the base current for Q_2. This is done to ensure that I_{B2} has a negligible effect on the bias conditions of Q_1. Normally, just making I_{C1} equal to I_{C2} is the simplest way to achieve the desired effect.

Example 12-8

Calculate suitable resistor values for a two-stage, direct-coupled amplifier, as in Fig. 12-20. The circuit is to use 2N3903 transistors, 14 V supply, 40 kΩ load resistance, and a signal source with a 600 Ω resistance.

Solution

Select, $V_{E1} = 5\text{ V}, V_{CE1} = V_{CE2} = 3\text{ V}$

$$V_{B2} = V_{C1} = V_{E1} + V_{CE1} = 5\text{ V} + 3\text{ V}$$
$$= 8\text{ V}$$

$$V_{E2} = V_{B2} - V_{BE} = 8\text{ V} - 0.7\text{ V}$$
$$= 7.3\text{ V}$$

$$V_{R5} = V_{CC} - V_{E2} - V_{CE2} = 14\text{ V} - 7.3\text{ V} - 3\text{ V}$$
$$= 3.7\text{ V}$$

Select, $$R_5 = \frac{R_L}{10} = \frac{40\text{ k}\Omega}{10}$$
$$= 4\text{ k}\Omega \text{ (use } 3.9\text{ k}\Omega \text{ standard value)}$$

$$I_{C2} = \frac{V_{R5}}{R_5} = \frac{3.7\text{ V}}{3.9\text{ k}\Omega}$$
$$= 949\,\mu\text{A}$$

$$R_6 = \frac{V_{E2}}{I_{C2}} = \frac{7.3\text{ V}}{949\,\mu\text{A}}$$

$= 7.7\text{ k}\Omega$ (use 8.2 kΩ and recalculate I_{C2})

$$I_{C2} = \frac{V_{E2}}{R_6} = \frac{7.3\text{ V}}{8.2\text{ k}\Omega}$$

$= 890\,\mu\text{A}$

$I_{C1} >> I_{B2}$, Select $I_{C1} = 1$ mA

$V_{R3} = V_{CC} - V_{C1} = 14\text{ V} - 8\text{ V}$

$= 6\text{ V}$

$$R_3 = \frac{V_{R3}}{I_{C1}} = \frac{6\text{ V}}{1\text{ mA}}$$

$= 6\text{ k}\Omega$ (use 5.6 kΩ and recalculate I_{C1} in order to keep $V_{B2} = 8\text{ V}$)

$$I_{C1} = \frac{V_{R3}}{R_3} = \frac{6\text{ V}}{5.6\text{ k}\Omega}$$

$= 1.07$ mA

$$R_4 = \frac{V_{E1}}{I_{C1}} = \frac{5\text{ V}}{1.07\text{ mA}}$$

$\approx 4.7\text{ k}\Omega$ (standard value)

$V_{R2} = V_{B1} = V_{E1} + V_{BE} = 5\text{ V} + 0.7\text{ V}$

$= 5.7\text{ V}$

$V_{R1} = V_{CC} - V_{B1} = 14\text{ V} - 5.7\text{ V}$

$= 8.3\text{ V}$

$R_2 = 10\,R_4 = 10 \times 4.7\text{ k}\Omega$

$= 47\text{ k}\Omega$

$$I_2 = \frac{V_{B1}}{R_2} = \frac{5.7\text{ V}}{47\text{ k}\Omega}$$

$= 121\,\mu\text{A}$

Eq. 10-11,
$$R_1 = \frac{V_{R1} \times R_2}{V_{R2}} = \frac{8.3\text{ V} \times 47\text{ k}\Omega}{5.7\text{ V}}$$

$= 68.4\text{ k}\Omega$ (use 68 kΩ standard value)

Example 12-9

Determine suitable capacitor values for the two-stage direct-coupled amplifier in Ex. 12-8. The lower cutoff frequency is to be 75 Hz.

Solution

From Appendix 1-5, for the *2N3903*: $h_{fe(min)} = 50$, and $h_{ie(min)} = 1\text{ k}\Omega$

$$Z_i = R_1 \| R_2 \| h_{ie} = 68\ \text{k}\Omega \| 47\ \text{k}\Omega \| 1\ \text{k}\Omega$$
$$= 965\ \Omega$$

Eq. 12-4,
$$X_{C1} = \frac{Z_i + r_s}{10} = \frac{965\ \Omega + 600\ \Omega}{10}$$
$$= 157\ \Omega$$

$$C_1 = \frac{1}{2\pi f_1 X_{C1}} = \frac{1}{2\pi \times 75\ \text{Hz} \times 157\ \Omega}$$
$$= 13.5\ \mu\text{F}\ \text{(use 15 } \mu\text{F standard value)}$$

Eq. 12-13,
$$X_{C2} = X_{C3} = \frac{0.65\, h_{ie}}{1 + h_{fe}} = \frac{0.65 \times 1\ \text{k}\Omega}{1 + 50}$$
$$\approx 12.7\ \Omega$$

$$C_2 = C_3 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2\pi \times 75\ \text{Hz} \times 12.7\ \Omega}$$
$$= 167\ \mu\text{F} \qquad \text{(use 180 } \mu\text{F standard value)}$$

from Eq. 12-5,
$$X_{C4} = \frac{R_5 + R_L}{10} = \frac{3.9\ \text{k}\Omega + 40\ \text{k}\Omega}{10}$$
$$= 4.39\ \text{k}\Omega$$

$$C_4 = \frac{1}{2\pi f_1 X_{C4}} = \frac{1}{2\pi \times 75\ \text{Hz} \times 4.39\ \text{k}\Omega}$$
$$= 0.48\ \mu\text{F} \qquad \text{(use 0.47 } \mu\text{F standard value)}$$

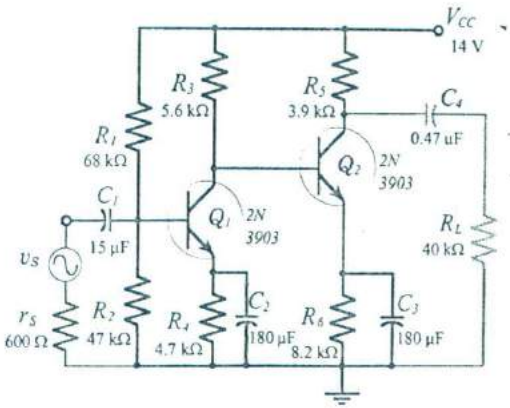


Figure 12-21
Two-stage direct-coupled CE amplifier designed in Examples 12-8 and 12-9.

Circuit Analysis

Analysis procedure for a two-stage direct-coupled circuit is similar to that for analysis of a two-stage capacitor-coupled circuit. The *h*-parameter equivalent for the circuit of Fig. 12-20 is exactly like Fig. 12-19, except that the bias resistors for the second stage are omitted. The voltage gain and impedance equations are as determined for the capacitor-coupled circuit. Because the component numbers differ slightly for the two circuits, care must be taken in substituting components into the equations. For example, from Eq. 12-17, the voltage gain of the second stage of the circuit in Fig. 12-20 is,

$$A_{v2} = \frac{-h_{fe2}(R_5 \| R_L)}{h_{ie2}}$$

Example 12-10

Calculate the minimum overall voltage gain for the circuit in Fig. 12-21.

Solution

Eq. 12-16.
$$A_{v1} = \frac{-h_{fe1}(R_3 \| Z_{i2})}{h_{ie1}} = \frac{-h_{fe1}(R_3 \| h_{ie2})}{h_{ie1}}$$
$$= \frac{-50 \times (5.6\ \text{k}\Omega \| 1\ \text{k}\Omega)}{1\ \text{k}\Omega}$$
$$\approx -42.4$$

Eq. 12-17.
$$A_{v2} = \frac{-h_{fe2}(R_5 \| R_L)}{h_{ie2}} = \frac{-50 \times (3.9\ \text{k}\Omega \| 40\ \text{k}\Omega)}{1\ \text{k}\Omega}$$
$$= -177.7$$

Eq. 12-18.
$$A_v = A_{v1} \times A_{v2} = (-42.4) \times (-177.7)$$
$$= 7533$$

Use of Complementary Transistors

The direct-coupled, two-stage circuit illustrated in Fig. 12-22 is similar to that in Fig. 12-20, except that transistor Q_2 is a *pnp* device. The transistors are selected to have similar characteristics and parameters although one is *npn* and the other is *pnp*. This means that they are *complementary transistors*. Examination of Appendices 1-5 and 1-6 reveals that the *2N3903* and the *2N3905* are complementary, as are the *2N3904* and the *2N3906*.

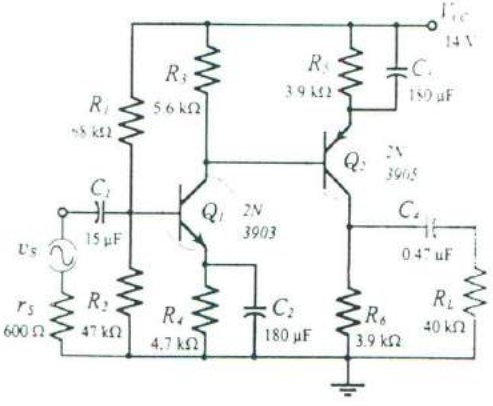


Figure 12-22
Direct-coupled two-stage CE amplifier using complementary transistors. Q_1 and Q_2 have similar parameters, although one is an npn transistor and the other is a pnp device.

Suppose the circuit in Fig. 12-22 is to be designed to use a 14 V supply, as in Example 12-8. Allowing $V_{E1} = 5$ V and $V_{CE1} = 3$ V, the base voltage for Q_2 (measured from $+V_{CC}$) is,

$$V_{B2} = V_{R3} = 6\ \text{V}$$

and
$$V_{R5} = V_{B2} - V_{BE} = 6\ \text{V} - 0.7\ \text{V}$$
$$= 5.3\ \text{V}$$

so,
$$V_{R6} = V_{CC} - V_{E2} - V_{CE2} = 14\ \text{V} - 5.3\ \text{V} - 3\ \text{V}$$
$$= 5.7\ \text{V}$$

The use of complementary transistors in Fig. 12-22 reduces the voltage drop across the emitter resistor of Q_2, compared to the situation in Fig. 12-20. This makes more voltage available for dropping across the Q_2 collector resistor.

The design procedure for the circuit using complementary transistors is very similar to the procedure for designing the non-complementary circuit in Fig. 12-20.

Practise Problems

12-4.1 A direct-coupled two-stage CE amplifier using complementary transistors (see Fig. 12-22) is to be designed to operate from a 25 V supply and to use a *2N3904* and a *2N3906* transistor. The capacitor-coupled load is 56 kΩ. Determine suitable resistor values.

12-4.2 Determine suitable capacitor values for the circuit in Problem 12-4.1 to give a 30 Hz lower cutoff frequency. Assume that $r_s = 300\ \Omega$.

12-4.3 Calculate the minimum overall voltage gain for the circuit in Practise Problems 12-4.1 and 12-4.2.

12-5 Two-Stage Circuit with Emitter Follower Output

Circuit

Figure 12-23 shows another direct-coupled circuit. This time the second stage is a common collector circuit, or emitter follower. *Stage 2* gives the circuit a very low output impedance, but has unity voltage gain. *Stage 1* still has substantial voltage gain.

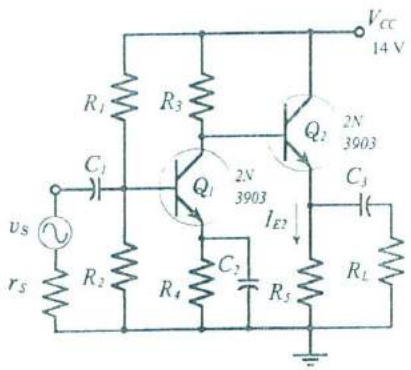


Figure 12-23
Two-stage direct-coupled CE amplifier consisting of a CE input stage and a CC (emitter follower) output stage for low output impedance.

The design procedure for this circuit is similar to the procedures already discussed. As with the circuit in Fig. 12-20, the Q_2 base bias voltage is the collector voltage of Q_1. A suitable level of emitter current I_{E2} is selected, and R_E is calculated to be $(V_{B2} - V_{BE})/I_{E2}$. Coupling capacitor C_1 is once again calculated from $X_{C1} = Z_i/10$.

The load resistor (R_l) may be relatively small, which means that coupling capacitor C_3 must be large. Therefore, both C_2 and C_3 are used to determine the low 3 dB frequency of the circuit by using the 0.65 factor employed in Eq. 12-14.

It is important to realize that the emitter follower in Fig. 12-23 is a small-signal circuit. In fact, this type of circuit functions best when the amplitude of the *ac* output voltage is much smaller than the *dc* base-emitter voltage of the output transistor (V_{BE}). With *ac* output voltages that approach or exceed V_{B2}, the base-emitter junction of Q_2 might become reverse biased when the output voltage moves rapidly in a negative direction. In this case, the circuit will not function correctly. Where large output voltages and low output impedance are required, a complementary emitter follower is used, (see Section 18-4).

With the second stage operating as a small-signal emitter follower, resistor R_5 in Fig. 12-23 does *not* have to be very much smaller than external load R_L. However, for satisfactory operation, Q_2 emitter current (I_{E2}) should be greater than the peak *ac* load current (i_p). The peak output current is calculated by dividing the desired peak output voltage v_p, by the load resistance: $i_p = v_p/R_L$.

Example 12-11

Determine suitable resistor values for the two-stage, amplifier circuit in Fig. 12-23. The circuit is to use 2N3903 transistors, the supply voltage is 20 V, the load resistance is 100 Ω, and the output voltage is to be ±100 mV.

Solution

$$i_p = \frac{v_p}{R_L} = \frac{100\text{ mV}}{100\ \Omega}$$
$$= 1\text{ mA}$$

$I_{E2} > i_p$ Select $I_{E2} = 2$ mA

Select, $V_{E1} = 5$ V and $V_{CE1} = 3$ V

$$V_{B2} = V_{C1} = V_{E1} + V_{CE1} = 5\text{ V} + 3\text{ V}$$
$$= 8\text{ V}$$

$$V_{E2} = V_{B2} - V_{BE} = 8\text{ V} - 0.7\text{ V}$$
$$= 7.3\text{ V}$$

$$R_5 = \frac{V_{E2}}{I_{E2}} = \frac{7.3\text{ V}}{2\text{ mA}}$$
$$= 3.65\text{ k}\Omega\text{ (use 3.3 k}\Omega\text{ standard value)}$$

$I_{C1} >> I_{B2}$, select $I_{C1} = 1$ mA

$$V_{R3} = V_{CC} - V_{B2} = 20\text{ V} - 8\text{ V}$$
$$= 12\text{ V}$$

$$R_3 = \frac{V_{R3}}{I_{C1}} = \frac{12\text{ V}}{1\text{ mA}}$$
$$= 12\text{ k}\Omega \text{ (standard value)}$$

$$R_4 = \frac{V_{E1}}{I_{C1}} = \frac{5\text{ V}}{2\text{ mA}}$$
$$= 5\text{ k}\Omega \text{ (use 4.7 k}\Omega\text{ standard value)}$$

$$V_{B1} = (I_{C1} \times R_4) + V_{BE} = (1\text{ mA} \times 4.7\text{ k}\Omega) + 0.7\text{ V}$$
$$= 5.4\text{ V}$$

Select, $R_2 = 10\,R_4 = 10 \times 4.7\text{ k}\Omega$
$= 47\text{ k}\Omega$

Eq 12-11, $$R_1 = \frac{V_{R1} \times R_2}{V_{R2}} = \frac{(20\text{ V} - 5.4\text{ V}) \times 47\text{ k}\Omega}{5.4\text{ V}}$$
$= 127\text{ k}\Omega$ (use 120 kΩ standard value)

Example 12-12

Calculate suitable capacitor values for the circuit designed in Example 12-11. The signal source resistance is 600 Ω, and the low 3-dB frequency is 150 Hz.

Solution

From Appendix 1-5, for the 2N3903: $h_{fe(min)} = 50$, and $h_{ie(min)} = 1\text{ k}\Omega$

$$Z_i = R_1 \| R_2 \| h_{ie} = 120\text{ k}\Omega \| 47\text{ k}\Omega \| 1\text{ k}\Omega$$
$$= 971\ \Omega$$

$$X_{C1} = \frac{Z_i + r_s}{10} = \frac{971\ \Omega + 600\ \Omega}{10}$$
$$= 157\ \Omega$$

$$C_1 = \frac{1}{2\pi f_1 X_{C1}} = \frac{1}{2\pi \times 150\text{ Hz} \times 157\ \Omega}$$
$$= 6.8\ \mu\text{F} \quad \text{(standard value)}$$

Eq. 12-14, $$X_{C2} = \frac{0.65\,h_{ie}}{1 + h_{fe}} = \frac{0.65 \times 1\text{ k}\Omega}{1 + 50}$$
$$\approx 12.7\ \Omega$$

$$C_2 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2\pi \times 150\text{ Hz} \times 12.7\ \Omega}$$
$$= 83.6\ \mu\text{F} \quad \text{(use 82 } \mu\text{F standard value)}$$

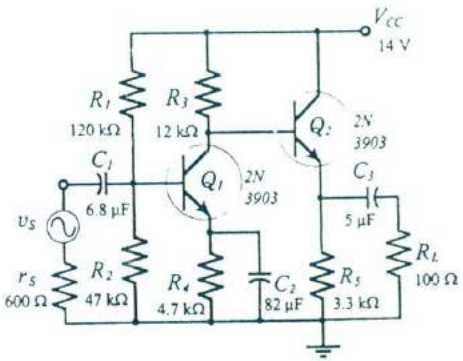


Figure 12-24
Two-stage direct-coupled CE amplifier designed in Examples 12-11 and 12-12.

From Eqns. 6-24 and 6-25,

$$Z_o = \left[\frac{h_{ic} + R_3}{h_{fc}}\right] \| R_5 = \left[\frac{1\text{ k}\Omega + 12\text{ k}\Omega}{51}\right] \| 3.3\text{ k}\Omega$$

$$= 237\ \Omega$$

$$X_{C3} \approx 0.65\,(R_L + Z_o) = 0.65\,(100\ \Omega + 237\ \Omega)$$
$$= 219\ \Omega$$

$$C_3 = \frac{1}{2\pi f_1 X_{C3}} = \frac{1}{2\pi \times 150\ \text{Hz} \times 219\ \Omega}$$

$$= 4.8\ \mu\text{F} \qquad \text{(use 5 } \mu\text{F standard value)}$$

Example 12-13

Analyze the two-stage transistor amplifier circuit in Fig. 12-24 to determine the minimum overall voltage gain.

Solution

From Eqn. 6-23 $Z_{i2} = h_{ic2} + h_{fc2}(R_5 \| R_L) = 1\ \text{k}\Omega + 51(3.3\ \text{k}\Omega \| 100\ \Omega)$
$= 5.95\ \text{k}\Omega$

Eq. 12-16, $A_{v1} = \dfrac{-h_{fe1}\,(R_3 \| Z_{i2})}{h_{ie1}} = \dfrac{-50 \times (12\ \text{k}\Omega \| 5.95\ \text{k}\Omega)}{1\ \text{k}\Omega}$
$= -199$

From Eq. 6-27, $A_{v2} \approx 1$

From Eq. 12-18, $A_v = A_{v1} \times A_{v2} = -199 \times 1$
$= -199$

Practise Problems

12-5.1 A two-stage direct-coupled *BJT* amplifier with an emitter-follower output is to be designed to operate from a 15 V supply. The capacitor-coupled load is 60 Ω. Using 2N3906 (*pnp*) transistors, determine suitable resistor values for the circuit.

12-5.2 Determine suitable capacitor values for the circuit in Problem 12-5.1 to give a 50 Hz lower cutoff frequency. Also, calculate the circuit minimum overall voltage gain. Assume that $r_s = 350\ \Omega$.

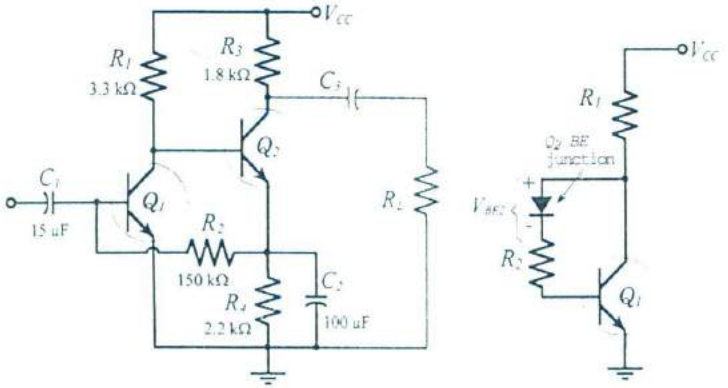
12-6 DC Feedback Pair

DC Feedback Pair With Two Amplification Stages

The two-stage amplifier circuit shown in Fig. 12-25(a) is known as a *dc feedback pair*. The base of transistor Q_2 is directly connected to the collector of Q_1, and the base of Q_1 is biased from the emitter of Q_2 via resistor R_2. Comparing this circuit to the capacitor-coupled circuit of Fig. 12-15 and the direct-coupled circuit of Fig. 12-20, it is seen that a further saving in components has been effected: R_1, R_2, R_4, and C_2 in Fig. 12-20 are now replaced

with the single resistor R_2 in Fig. 12-25.

To understand the bias arrangement for the *dc* feedback pair, note that there is only a *pn* junction voltage drop V_{BE2} between the Q_1 collector and the Q_2 emitter. This is illustrated in Fig. 12-25(b), where it is seen that the first stage of the circuit is essentially a collector-to-base bias circuit. *Stage 2* bias arrangement is similar to voltage divider bias, with resistor R_4 stabilizing the transistor emitter current. The base voltage for Q_2 is derived from the collector of Q_1; consequently, the bias stability of the second stage is no better than that of the first stage.



(a) Circuit of *dc* feedback pair (b) Equivalent circuit for Q_1

Figure 12-25
In a dc feedback pair the base of Q_2 is directly connected to the collector of Q_1, and the base of Q_1 is biased via R_2 from the emitter of Q_2. This arrangement uses fewer components than a capacitor-coupled two-stage circuit.

Because collector-to-base bias is not as stable as voltage divider bias, the bias conditions in this circuit are not as stable as in the circuit of Fig. 12-20. However, the stability is adequate for most purposes, and the component savings can be a major advantage.

The *dc* feedback pair derives its name from the direct coupling between stages and from the feedback from the collector of Q_1 to its base. As explained for collector-to-base bias in Section 5-3, a change in the level of Q_1 collector voltage (V_{C1}), produces a change in base current (I_{B1}). The I_{B1} change in turn alters I_{C1}, and the voltage drop $I_{C1}R_1$ tends to push V_{C1} back towards its original level.

As well as stabilizing the circuit *dc* conditions, the feedback can produce *ac* degeneration, (see Section 6-1). Capacitor C_2 shorts the *ac* feedback to ground, to eliminate *ac* degeneration from *Stage 1*. As the emitter bypass capacitor, C_2 also eliminates *ac* degeneration from *Stage 2*.

The design approach to the *dc* feedback pair is similar to those already discussed. The output stage is designed exactly like the output stage for the direct-coupled circuit in Fig. 12-20. The input stage is designed as a collector-to-base bias circuit to have a collector voltage (V_{C1}) equal to the desired level of the *Stage 2* base voltage (V_{B2}).

The input impedance of the circuit is

$$Z_i = R_2 \| h_{ie} \qquad \textbf{(12-19)}$$

So, (From Eq. 12-4) the impedance of C_1 at f_1 is,

$$X_{C1} = \frac{(R_2 \| h_{ie}) + r_s}{10}$$

C_2 is by far the largest capacitor in the circuit, so it determines the circuit low 3 dB frequency:

Eq. 12-2, $$X_{C2} = \frac{h_{ie}}{1 + h_{fe}} \text{ at } f_1$$

C_3 is once again calculated from Eq. 12-5,

$$X_{C3} = \frac{Z_o + R_L}{10}$$

DC Feedback pair with Emitter Follower Output

Figure 12-26 shows a *dc* feedback pair that has an emitter follower output stage. In this case, a bypass capacitor cannot be used at the emitter of Q_2, otherwise the output would be *ac* shorted to ground. However, C_2 in Fig. 12-25 also serves the purpose of eliminating *ac* feedback from the collector of Q_1 to its base (via Q_2). So, now another method of removing this *ac* feedback must be employed. In Fig. 12-26, the base bias resistor for Q_1 is split into two resistors, and the junction of these two is *ac* grounded via capacitor C_2.

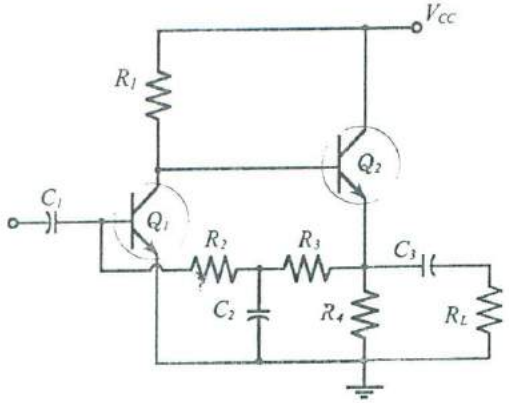


Figure 12-26
DC feedback pair with an emitter follower output stage. In this case, two series-connected feedback resistors (R_2 and R_3) are used, and the junction of the two is grounded via C_2 to eliminate ac degeneration.

The design of this circuit differs from other designs only in calculation of the capacitor values. In this case, X_{C2} should be very much smaller than R_3 at f_1. This is because the *ac* output voltage at the emitter of Q_2 is divided across R_3 and X_{C2} before being fed back to the Q_1 base. Capacitor values normally depend on the resistance in series with them, and in Fig. 12-26 R_3 is in series

with C_2 for *ac* feedback. Because this capacitor is in the feedback path from output to input, it is calculated at f_1 from

$$X_{C2} = \frac{R_3}{100} \qquad \textbf{(12-20)}$$

The reasons for using a factor of 100, instead of the usual factor of 10, will be understood when negative feedback is studied, (see Chapter 13).

Normally, the largest capacitor in any circuit is employed to determine the circuit low 3 dB frequency (f_1). Where two capacitors are likely to be equally large, they are both used to set f_1. The largest capacitor is always the one in series with the lowest resistance. In the circuit in Fig. 12-26, the external load resistance is likely to be the smallest resistance in series with a capacitor. Consequently, C_3 is calculated from,

$$X_{C3} = (Z_o + R_L) \text{ at } f_1 \qquad \textbf{(12-21)}$$

Example 12-14

Design a *dc* feedback pair with an emitter follower output, as shown in Fig. 12-26. The circuit is to use *2N3904* transistors with a 12 V supply. The load resistance is 50 Ω, the lower cutoff frequency is 150 Hz, and the output voltage is to be ±50 mV. Assume that $r_s << Z_{in}$.

Solution

$$i_p = \frac{v_p}{R_L} = \frac{50 \text{ mV}}{50 \Omega}$$
$$= 1 \text{ mA}$$

$I_{E2} > i_p$ Select $I_{E2} = 2$ mA

Select, $V_{E2} = 5$ V

$$R_4 = \frac{V_{E2}}{I_{E2}} = \frac{5 \text{ V}}{2 \text{ mA}}$$
$$= 2.5 \text{ k}\Omega \text{ (use 2.2 k}\Omega \text{ standard value)}$$

$I_{C1} >> I_{B2}$, select $I_{C1} = 1$ mA

$$V_{R1} = V_{CC} - (V_{BE2} + V_{E2}) = 12 \text{ V} - (0.7 \text{ V} + 5 \text{ V})$$
$$= 6.3 \text{ V}$$

$$R_1 = \frac{V_{R1}}{I_{C1}} = \frac{6.3 \text{ V}}{1 \text{ mA}}$$
$$= 6.3 \text{ k}\Omega \text{ (use 5.6 k}\Omega \text{ and recalculate } I_{C1})$$

$$I_{C1} = \frac{6.3 \text{ V}}{5.6 \text{ k}\Omega} = 1.13 \text{ mA}$$

From Appendix 1-5, for the *2N3904*: $h_{FE(min)} = 70$, $h_{fe} = 100$, and $h_{ie} = 1\ k\Omega$

so, $$I_{B1} = \frac{I_{C1}}{h_{fE}} = \frac{1.13\ mA}{70}$$
$$= 16.1\ \mu A$$

$$R_2 + R_3 = \frac{V_{E2} - V_{BE}}{I_{B1}} = \frac{5\ V - 0.7\ V}{16.1\ \mu A}$$
$$= 267\ k\Omega$$

select, $R_2 = 120\ k\Omega$, and $R_3 = 150\ k\Omega$

Eq. 12-19, $$Z_i = R_2 \| h_{ie} = 120\ k\Omega \| 1\ k\Omega$$
$$= 992\ \Omega$$

$$X_{C1} = \frac{Z_i + r_s}{10} = \frac{992\ \Omega}{10}$$
$$= 99.2\ \Omega$$

$$C_1 = \frac{1}{2\pi f_1 X_{C1}} = \frac{1}{2\pi \times 150\ Hz \times 99.2\ \Omega}$$
$$= 10.7\ \mu F \quad \text{(use 15 } \mu F \text{ standard value)}$$

Eq. 12-20, $$X_{C2} = \frac{R_3}{100} = \frac{150\ k\Omega}{100}$$
$$= 1.5\ k\Omega$$

$$C_2 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2\pi \times 150\ Hz \times 1.5\ k\Omega}$$
$$= 0.71\ \mu F \quad \text{(use 0.82 } \mu F \text{ standard value)}$$

$$Z_o = \left[\frac{h_{ie2} + R_1}{h_{fe}}\right] \| R_4 = \left[\frac{1\ k\Omega + 5.6\ k\Omega}{100}\right] \| 2.2\ k\Omega$$
$$= 64\ \Omega$$

Eq. 12-21, $$X_{C3} = R_L + Z_o = 50\ \Omega + 64\ \Omega$$
$$= 114\ \Omega$$

$$C_3 = \frac{1}{2\pi f_1 X_{C3}} = \frac{1}{2\pi \times 150\ Hz \times 114\ \Omega}$$
$$= 9.3\ \mu F \quad \text{(use 10 } \mu F \text{ standard value)}$$

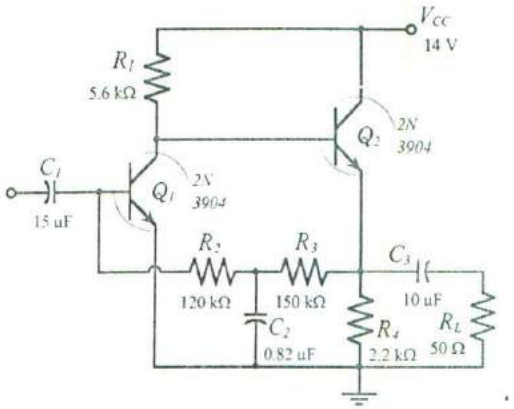


Figure 12-27
Two-stage dc feedback pair designed in Example 12-14.

Practice Problems

12-6.1 A *dc* feedback pair as in Fig. 12-25 is to use $V_{CC} = 15$ V, $R_L = 47$ kΩ, and *2N3903* transistors. Determine suitable resistor values.

12-6.2 The circuit in Problem 12-6.1 to have $f_1 = 75$ Hz. Determine suitable capacitor values, and calculate the circuit minimum overall voltage gain. Assume that $r_s = 350\ \Omega$.

12-7 BIFET Circuits

BJT-FET Considerations

Two-stage *BJT* circuits usually have relatively low input impedances. To increase Z_i, a field effect transistor may be used as the first stage. Circuits which are composed of *BJTs* and *FETs* are termed *BIFET* circuits. Since a *FET* circuit normally has much lower voltage gain than a *BJT* circuit, a *BIFET* circuit can be expected to have lower overall voltage gain than a two-stage *BJT* circuit. Two-stage *FET* circuits can be designed and constructed. However, the voltage gain of a two-stage *FET* circuit is substantially lower than that of a *BIFET* circuit, and there are no advantages to offset the lower voltage gain.

Capacitor-Coupled BIFET Amplifier

A two-stage, capacitor-coupled *BIFET* amplifier circuit is shown in Fig. 12-28. The input stage provides a very high input resistance and a voltage gain usually ranging from 5 to 15. *Stage* 2 has the typical bipolar voltage gain of 200 to 500, depending upon transistor parameters and resistor values. Each stage is designed independently, as discussed in Sections 12-1 and 12-2. The two stages of the circuit shown in Fig. 12-28 are those designed in Examples 12-2 through 12-5. In this case, C_3 in Fig. 12-14 is omitted, and C_3 in Fig. 12-28 is the interstage coupling capacitor.

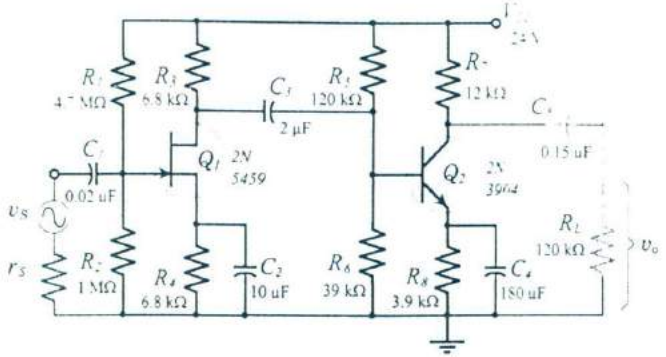
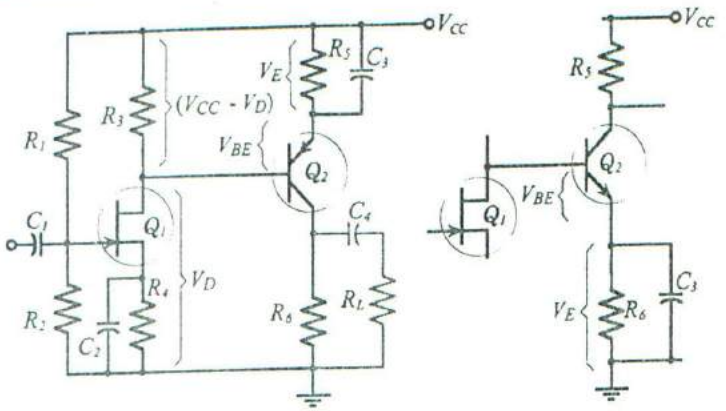


Figure 12-28
Capacitor-coupled two-stage BIFET amplifier. The FET input stage provides a high input impedance, and the BJT produces substantial voltage gain.

Direct-Coupled BIFET Amplifier

In the direct-coupled *BIFET* circuit in Fig. 12-29(a), transistor Q_1 is an *n*-channel *JFET* and Q_2 is a *pnp* bipolar transistor. An *npn BJT* could be used in the circuit, as illustrated in Fig. 12-29(b); however, this arrangement uses a large voltage drop across Q_2 emitter resistor (R_6), leaving a smaller voltage drop across the collector resistor (R_5). Q_2 can also be driven into saturation if the drain current of Q_1 is lower than the design level. For the circuit in Fig. 12-29(a), V_{CE2} is increased when I_{D1} is less than the $I_{D(max)}$ design level.



(a) using a *pnp* output transistor (b) using an *npn* output transistor

Figure 12-29
Direct-coupled two-stage BIFET amplifier. When Q_1 is an n-channel FET, it is preferable that Q_2 be a pnp BJT.

Design Calculations

Example 12-15

Determine suitable resistors for the BIFET amplifier in Fig. 12-29(a). The circuit is to use a *2N3906 BJT* and a *2N5486 FET*. The supply voltage is 20 V, the external load resistance is 80 kΩ, the circuit input impedance is to be approximately 500 kΩ, and the low 3 dB frequency is to be 150 Hz.

Solution

The *2N5486* has:

$$V_{p(max)} = -6\text{ V},\ I_{DSS(max)} = 20\text{ mA, and } Y_{fs} = 6000\ \mu\text{S (typically)}$$

Select, $I_{D(max)} \approx 2\text{ mA}$

Eq. 10-8, $$V_{GS} = V_P[1 - \sqrt{(I_D/I_{DSS})}] = -6\text{ V}\,[1 - \sqrt{(2\text{ mA}/20\text{ mA})}]$$
$$\approx -4.1\text{ V}$$

Eq. 12-8, $$V_{DS(min)} = V_{P(max)} + 1\text{ V} - V_{GS} = 6\text{ V} + 1\text{ V} - 4.1\text{ V}$$
$$= 2.9\text{ V}$$

$$V_{R3} + V_{R4} = V_{CC} - V_{DS} = 20\text{ V} - 2.9\text{ V}$$
$$= 17.1\text{ V}$$

$$V_{R3} = V_{R4} = \frac{17.1\text{ V}}{2}$$
$$\approx 8.5\text{ V}$$

$$R_3 = R_4 = \frac{V_{R4}}{I_D} = \frac{8.5\text{ V}}{2\text{ mA}}$$
$$= 4.25\text{ k}\Omega \qquad \text{(use 3.9 k}\Omega\text{ standard value, and recalculate } V_{R3} \text{ and } V_{R4})$$

$$V_{R3} = V_{R4} = I_D \times R_4 = 2 \text{ mA} \times 3.9 \text{ k}\Omega$$
$$= 7.8 \text{ V}$$

$$V_{R2} = V_G = V_{R4} - V_{GS} = 7.8 \text{ V} - 4.1 \text{ V}$$
$$= 3.7 \text{ V}$$

$$V_{R1} = V_{CC} - V_{R3} = 20 \text{ V} - 3.7 \text{ V}$$
$$= 16.3 \text{ V}$$

For $Z_i \approx 500 \text{ k}\Omega$, select $R_2 = 560 \text{ k}\Omega$

Eq. 12-10, $$R_1 = \frac{V_{R1} \times R_2}{V_{R2}} = \frac{16 \text{ V} \times 560 \text{ k}\Omega}{3.7 \text{ V}}$$
$$\approx 2.5 \text{ M}\Omega \text{ (use 2.7 M}\Omega \text{ standard value)}$$

Select, $$R_6 \approx \frac{R_L}{10} = \frac{80 \text{ k}\Omega}{10}$$
$$= 8 \text{ k}\Omega \text{ (use 8.2 k}\Omega \text{ standard value)}$$

$$V_{R5} = V_{R3} - V_{BE2} = 7.8 \text{ V} - 0.7 \text{ V}$$
$$= 7.1 \text{ V}$$

$$V_{R6} = V_{CC} - V_{R5} - V_{CE \text{ min}} = 20 \text{ V} - 7.1 \text{ V} - 3 \text{ V}$$
$$= 9.9 \text{ V}$$

$$I_{C2} = \frac{V_{R6}}{R_6} = \frac{9.9 \text{ V}}{8.2 \text{ k}\Omega}$$
$$= 1.2 \text{ mA}$$

$$R_5 \approx \frac{V_{R5}}{I_{C2}} = \frac{7.1 \text{ V}}{1.2 \text{ mA}}$$
$$= 5.9 \text{ k}\Omega \text{ (use 6.8 k}\Omega \text{ standard value)}$$

Example 12-16

Determine suitable capacitor values for the BIFET direct-coupled amplifier in Example 12-15.

Solution

$$Z_i = R_1 \| R_2 = 2.7 \text{ M}\Omega \| 560 \text{ k}\Omega$$
$$= 464 \text{ k}\Omega$$

Eq. 12-4, $$X_{C1} = \frac{Z_i}{10} = \frac{464 \text{ k}\Omega}{10}$$
$$= 46.4 \text{ k}\Omega$$

$$C_1 = \frac{1}{2\pi f_1 X_{C1}} = \frac{1}{2\pi \times 150\ \text{Hz} \times 46.4\ \text{k}\Omega}$$

$$= 0.02\ \mu\text{F} \quad \text{(standard value)}$$

From Eq. 12-12,

$$X_{C2} = \frac{0.65}{Y_{fs}} = \frac{0.65}{6000\ \mu\text{S}}$$

$$= 108\ \Omega$$

$$C_2 = \frac{1}{2\pi f_1 X_{C2}} = \frac{1}{2\pi \times 150\ \text{Hz} \times 108\ \Omega}$$

$$= 9.8\ \mu\text{F} \quad \text{(use 10 } \mu\text{F standard value)}$$

Eq. 12-13, $$X_{C3} = \frac{0.65\, h_{ie2}}{1 + h_{fe2}} = \frac{0.65 \times 2\ \text{k}\Omega}{1 + 100}$$

$$\approx 13\ \Omega$$

$$C_3 = \frac{1}{2\pi f_1 X_{C3}} = \frac{1}{2\pi \times 150\ \text{Hz} \times 13\ \Omega}$$

$$= 81.6\ \mu\text{F} \quad \text{(use 82 } \mu\text{F standard value)}$$

From Eq. 12-5, $$X_{C4} = \frac{R_6 + R_L}{10} = \frac{8.2\ \text{k}\Omega + 80\ \text{k}\Omega}{10}$$

$$= 8.8\ \text{k}\Omega$$

$$C_4 = \frac{1}{2\pi f_1 X_{C4}} = \frac{1}{2\pi \times 150\ \text{Hz} \times 8.8\ \text{k}\Omega}$$

$$= 0.12\ \mu\text{F} \quad \text{(standard value)}$$

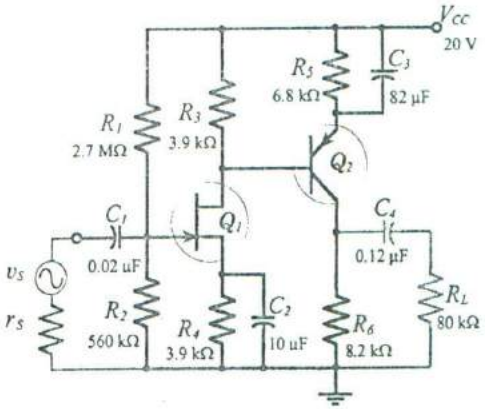


Figure 12-30
BIFET amplifier designed in Examples 12-15 and 12-16.

Example 12-17

Analyze the amplifier circuit in Fig. 12-30 to determine its minimum overall voltage gain.

Solution

For the 2N3906, $Z_{i2} = h_{ie} = 2\ \text{k}\Omega$

Eq. 11-7, $$A_{v1} = -Y_{fs}\,(R_3 \| Z_{i2}) = -6000\ \mu\text{S} \times (3.9\ \text{k}\Omega \| 2\ \text{k}\Omega)$$

$$= -7.9$$

From Eq. 12-17, $$A_{v2} = \frac{-h_{fe2}\,(R_6 \| R_L)}{h_{ie2}} = \frac{-100 \times (8.2\ \text{k}\Omega \| 80\ \text{k}\Omega)}{2\ \text{k}\Omega}$$

$$= -372$$

From Eq. 12-18, $$A_v = A_{v1} \times A_{v2} = (-7.9) \times (-372)$$

$$= 2939$$

Practise Problems

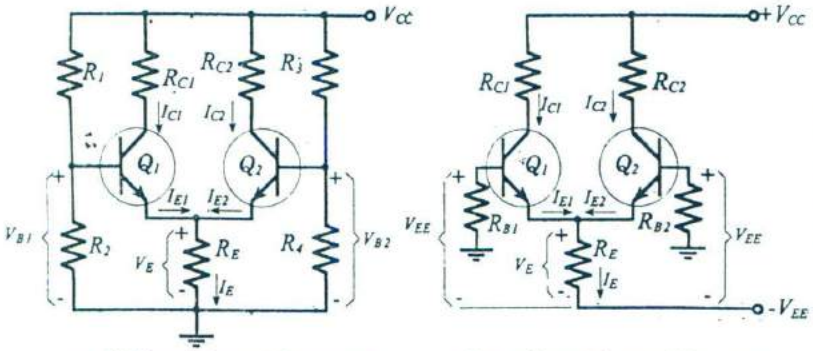
12-7.1 A *BIFET* circuit, as in Fig. 12-28, is to use the circuits designed in Examples 12-2 through 12-5. Make the necessary design modifications to give a 100 Hz lower cutoff frequency.

12-7.2 Calculate the minimum voltage gain for the circuit in Problem 12-7.1.

12-8 Differential Amplifier

Differential Amplifier Circuit

The *differential amplifier* is widely applied in integrated circuitry, because it has both good bias stability and good voltage gain without the use of large bypass capacitors. Its use in integrated circuits is further studied in Chapter 14. Differential amplifiers can also be constructed as discrete component circuits.



(a) Differential amplifier using single-polarity supply

(b) Differential amplifier using plus-minus supply

Figure 12-31
A differential amplifier has two emitter-coupled transistors with a single emitter resistor. The emitter current tends to split evenly between Q_1 and Q_2.

Figure 12-31(a) shows that a basic differential amplifier circuit consists of two voltage divider bias circuits with a single emitter resistor. The circuit is also known as an *emitter-coupled amplifier*, because the transistors are coupled at the emitter terminals. If transistors Q_1 and Q_2 are assumed to be identical in all respects, and if $V_{B1} = V_{B2}$, then the emitter currents are equal, and the total emitter current is,

$$I_E = I_{E1} + I_{E2} \qquad \textbf{(12-22)}$$

also, $$V_E = V_B - V_{BE}$$

so, $$I_E = \frac{V_B - V_{BE}}{R_E}$$

and, $$I_{E1} = I_{E2} = \frac{I_E}{2}$$

Like the emitter current in a single-transistor voltage divider bias circuit, I_E in the differential amplifier remains virtually constant regardless of the transistor h_{FE} value. This results in, I_{E1}, I_{E2}, I_{C1}, and I_{C2} all remaining substantially constant, and the constant collector current levels keep V_{C1} and V_{C2} stable. So, the differential amplifier has the same excellent bias stability as a single-transistor voltage divider bias circuit.

The circuit of a differential amplifier using a plus-minus supply is shown in Fig. 12-31(b). In this case, the voltage across the emitter resistor is $(V_{EE} - V_{BE})$, as illustrated,

and,
$$I_{E1} = I_{E2} = \frac{V_{EE} - V_{BE}}{2\,R_E} \qquad \textbf{(12-23)}$$

The base resistors (R_{B1} and R_{B2}) are included to bias the transistor bases to ground while offering an acceptable input resistance to a signal applied to one of the bases. (See the emitter current bias circuit discussion in Section 5-8.) The transistor emitter currents (I_{E1} and I_{E2}) are exactly equal only if the devices are perfectly matched. To allow for some differences in transistor parameters, a small-value potentiometer (R_{EE}) is sometimes included between the emitters, (see Fig. 12-32). Adjustment of R_{EE} increases the resistance in series with the emitter of one transistor, and reduces the emitter resistance for the other transistor. This reduces the I_E for one transistor and increases it for the other, while the total emitter current remains constant.

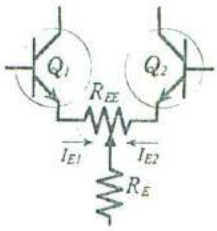


Figure 12-32
A potentiometer connected between the emitters of Q_1 and Q_2 allows I_{E1} and I_{E2} to be equalized.

AC Operation

Consider what happens when the *ac* input voltage (v_i) at the base of Q_1 is positive-going, as illustrated in Fig. 12-33. Q_1 emitter current (I_{E1}) increases. Also, I_{E2} decreases, because the total emitter current ($I_{E1} + I_{E2}$) remains constant. This means that I_{C1} increases and I_{C2} decreases, and consequently, V_{C1} falls and V_{C2} rises, as shown. So, the *ac* output voltage at Q_1 collector is in antiphase to v_i at Q_1 base, and the output at Q_2 collector is in phase with v_i.

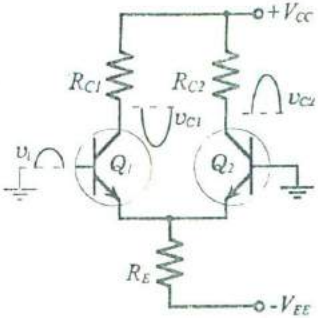


Figure 12-33
An positive-going ac input applied to the base of Q_1 produces a negative-going output at Q_{1C} and a positive-going output at Q_{2C}.

Voltage Gain

The voltage gain of a single-stage amplifier with an unbypassed emitter resistor and no external load is given by Eq. 6-21,

$$A_v = \frac{-h_{fe}\,R_C}{h_{ie} + (1 + h_{fe})R_E}$$

Refering to Fig. 12-34, it is seen that the resistance *looking into* the emitter of Q_2 is h_{ib}, so $h_{ib} \| R_E$ behaves like an unbypassed resistor in series with the emitter of Q_1. Neglecting R_E because it is very much larger than h_{ib}, the voltage gain from the base of Q_1 to its collector is,

$$A_v = \frac{-h_{fe}\,R_C}{h_{ie} + (1 + h_{fe})h_{ib}}$$

this reduces to, $$A_v = \frac{-h_{fe} R_C}{2 h_{ie}} \qquad (12\text{-}24)$$

Equation 12-24 gives the voltage gain from one input terminal to one output of a differential amplifier. It is seen to be half the voltage gain of a similar single-transistor *CE* amplifier with R_E bypassed; but note that *the differential amplifier requires no bypass capacitor.* This is an important advantage, because bypass capacitors are usually large and expensive.

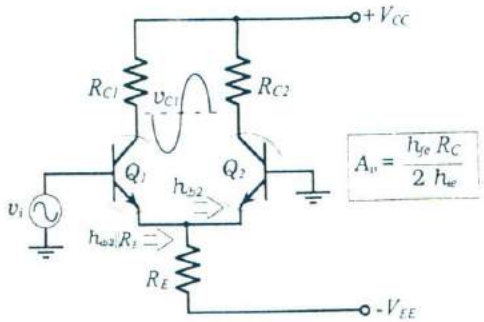


Figure 12-34
The voltage gain of a differential amplifier is half the gain of a common-emitter circuit using similar components. Note the absence of an emitter bypass capacitor.

Another way to contemplate the operation of the differential amplifier circuit is to think of the input voltage being equally divided between Q_1 base-emitter and Q_2 base-emitter. This is illustrated in Fig. 12-35 where it is seen that (for a positive-going input) $v_i/2$ is applied *positive on the base* of Q_1, while the other half of v_i appears *positive on the emitter* of Q_2. Thus, for v_i at Q_{1B}, transistor Q_1 behaves as a common-emitter circuit, and because Q_2 receives the input at its emitter, Q_2 behaves as a common-base circuit. Consequently,

$$v_{C1} = \frac{v_i}{2} \times \frac{-h_{fe} R_C}{h_{ie}}$$

and,

$$v_{C2} = \frac{v_i}{2} \times \frac{h_{fe} R_C}{h_{ie}}$$

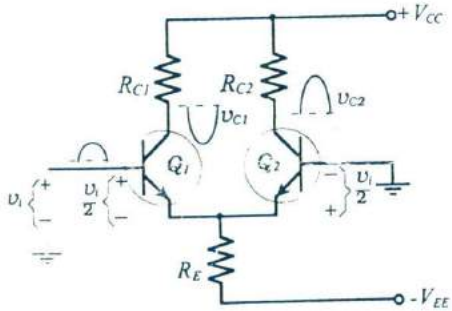


Figure 12-35
A signal at the base of Q_1 is divided equally between the BE junctions of Q_1 and Q_2. Half of v_i appears at Q_1 base-emitter as a common-emitter circuit, and the other half is applied to Q_2 base-emitter as a common-base circuit.

Input and Output Impedances

From Eq. 6-20, the input impedance at the base of a *CE* circuit with an unbypassed emitter resistor is,

$$Z_b = h_{ie} + (1 + h_{fe})R_E$$

Referring to Fig. 12-34, the differential amplifier has $h_{ib} \| R_E$ as an unbypassed resistor in series with the emitter of Q_1. Neglecting R_E (because $R_E >> h_{ib}$), the input resistance at Q_{1B} is,

$$Z_b = h_{ie} + (1 + h_{fe})h_{ib}$$

This reduces to,

$$\mathbf{Z_b = 2\, h_{ie}} \qquad \textbf{(12-25)}$$

or, $Z_b = 2$ (Z_b for a single-stage *CE* circuit)

Note that there are usually bias resistors in parallel with Z_b, so that (from Eq. 6-12) the circuit input impedance is,

$$Z_i = R_B \| Z_b$$

As in the case of *CE* and *CB* circuits, the output impedance at the transistor collector terminals is given by Eq. 6-14:

$$Z_o = R_C \| (1/h_{oe})$$

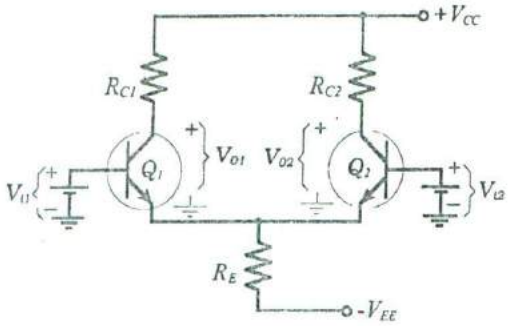


Figure 12-36
When dc voltages are applied to the two inputs of a differential amplifier, the outputs at the transistor collectors are proportional to the differences between the input voltages.

DC Amplification

When one transistor base is grounded in a differential amplifier, and an input is applied to the other one, as already discussed, v_i is amplified to produce the outputs at the collector terminals. In this case v_i is the *voltage difference* between the two base terminals. Figure 12-36 shows a differential amplifier with *dc* input voltages V_{i1} and V_{i2} applied to the transistor bases. If the voltage gain from the base to the collector is A_v, the *dc* voltage changes at the collectors are:

$$\Delta V_{o1} = A_v(V_{i2} - V_{i1})$$

and,

$$\Delta V_{o2} = A_v(V_{i1} - V_{i2})$$

It is seen that the differential amplifier can be employed as a *direct-coupled amplifier*, or *dc amplifier*. The term *difference amplifier* is also used for this circuit.

Design Calculations

Design procedures for a differential amplifier are similar to those for voltage divider bias circuits. Because there is no bypass capacitor in a differential amplifier, one of the coupling capacitors determines the circuit lower cutoff frequency (f_l). The capacitor with the smallest resistance in series with it is normally the largest capacitor, and in the case of a differential amplifier this is usually the input coupling capacitor. So, the input coupling capacitor determines the circuit lower cut-off frequency.

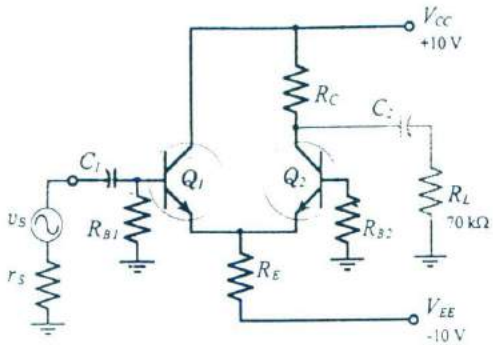


Figure 12-37
Differential amplifier circuit with capacitor-coupled signal and load.

Consider the capacitor-coupled differential amplifier in Fig. 12-37. The circuit uses a plus-minus supply, and a single collector resistor (R_C). No output is taken from Q_1 collector, so there is no need for a collector resistor. R_C is selected in the usual way for a small-signal amplifier; $R_C << R_L$. The collector-emitter voltage should be a minimum of 3 V, as always. Then, I_C is calculated from R_C and the selected voltage drop across R_C.

The total emitter current is determined as,

$$I_E \approx I_{C1} + I_{C2} \approx 2\, I_C$$

and,

$$\boldsymbol{R_E = \frac{V_{EE} - V_{BE}}{I_E}} \qquad \textbf{(12-26)}$$

The base bias resistors are determined from Eq. 5-17,

$$R_B = \frac{V_{BE}}{10\, I_{B(max)}}$$

As discussed, capacitor C_1 sets the lower cutoff frequency. So,

$$\boldsymbol{X_{C1} = Z_i \text{ at } f_1} \qquad \textbf{(12-27)}$$

and C_2 is determined from Eq. 12-5,

$$X_{C2} = R_L/10 \text{ at } f_1$$

Example 12-18

Determine suitable resistor values for the differential amplifier circuit in Fig. 12-37. The transistor parameters are $h_{FE} = 60$, $h_{fe} = 60$, and $h_{ie} = 1.4\ k\Omega$.

Solution

$$R_{C2} << R_L$$

select $$R_{C2} \approx \frac{R_L}{10} \approx \frac{70\ k\Omega}{10}$$

$$= 7\ k\Omega \text{ (use } 6.8\ k\Omega \text{ standard value)}$$

select $$V_{CE(min)} = 3\ V$$

$$V_{RC2} = V_{CC} + V_{BE} - V_{CE(min)} = 10\ V + 0.7\ V - 3\ V$$
$$= 7.7\ V$$

$$I_C = \frac{V_{RC2}}{R_C} = \frac{7.7\ V}{6.8\ k\Omega}$$
$$= 1.13\ mA$$

Eq. 12-26, $$R_E = \frac{V_{EE} - V_{BE}}{I_E} \approx \frac{10\ V - 0.7\ V}{2 \times 1.13\ mA}$$
$$= 4.1\ k\Omega \text{ (use } 4.7\ k\Omega \text{ standard value)}$$

From Eq. 5-17, $$R_B = \frac{V_{BE}}{10\, I_{B(max)}} = \frac{V_{BE}}{10\,(I_C/h_{FE})} = \frac{0.7\ V}{10 \times (1.1\ mA/60)}$$
$$= 3.8\ k\Omega \text{ (use } 3.9\ k\Omega \text{ standard value)}$$

$$R_{B1} = R_{B2} = 3.9\ k\Omega$$

Example 12-19

Determine suitable capacitor values for the amplifier in Ex. 12-18 to give $f_1 =$ 60 Hz. Also, calculate the circuit voltage gain. Assume that $r_s << Z_i$.

Solution

Eq. 12-25, $$Z_b = 2\, h_{ie} = 2 \times 1.4\ k\Omega$$
$$= 2.8\ k\Omega$$

$$Z_i = R_B \| Z_b = 3.9\ k\Omega \| 2.8\ k\Omega$$
$$= 1.6\ k\Omega$$

from Eq. 12-27, $$C_1 = \frac{1}{2\,\pi\, f_1\, Z_i} = \frac{1}{2\,\pi \times 60\ Hz \times 1.6\ k\Omega}$$
$$= 1.66\ \mu F \text{ (use } 1.8\ \mu F \text{ standard value)}$$

from Eq. 12-5, $$C_3 = \frac{1}{2\,\pi\, f_1\, (R_L/10)} = \frac{1}{2\,\pi \times 60\ Hz \times (70\ k\Omega/10)}$$
$$= 0.38\ \mu F \text{ (use } 0.39\ \mu F \text{ standard value)}$$

from Eq. 12-24, $A_v = \dfrac{h_{fe}\,(R_{C2} \| R_L)}{2\,h_{ie}} = \dfrac{60 \times (6.8\ \text{k}\Omega \| 70\ \text{k}\Omega)}{2 \times 1.4\ \text{k}\Omega}$

$= 133$

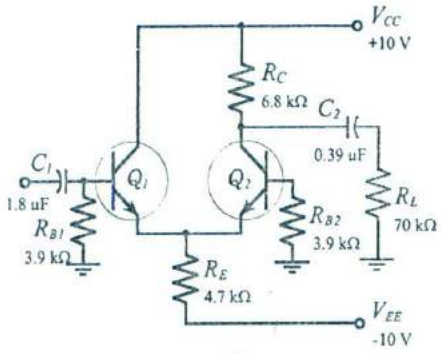


Figure 12-38
Capacitor-coupled differential amplifier circuit designed in Examples 12-18 and 12-19.

Practise Problems

12-8.1 The differential amplifier in Fig. 12-31(a) is to use a 2N3904 transistor, a 20 V supply, and to have a 100 kΩ load capacitor-coupled to Q_2 collector. Determine suitable resistor values.

12-8.2 Determine suitable coupling capacitor values for the circuit in Problem 12-9.1 to give a 75 Hz lower cutoff frequency. Also, calculate the overall voltage gain. Assurme that $r_s = 200\ \Omega$.

12-9 Small-Signal High-Frequency Amplifiers

Common Base Amplifier

A practical *CB* amplifier (using a plus/minus supply) is shown in Fig. 12-39. [Note the polarity of the input coupling capacitor (C_1).] The *CB* circuit is analysed in Section 6-7, where it is found to have a very low input impedance, as well as a voltage gain and output impedance similar to a *CE* circuit. Because the *CB* circuit has no phase inversion between the input and output terminals, there is no Miller-effect amplification of the collector-base capacitance, (see Sections 8-3 and 8-4). Consequently, a *CB* circuit is capable of operating at much higher frequencies than a *CE* circuit.

Design procedure for a *CB* circuit is exactly the same as that for a *CE* circuit, (see Section 12-1). Resistor calculation is performed just as if a *CE* circuit were being designed. The output coupling capacitor (C_2 in Fig. 12-39) is determined in the usual way. Because of the very low input impedance of a *CB* circuit, the input coupling capacitor (C_1) is the largest capacitor in the circuit. So, C_1 determines the circuit low cutoff frequency, and its capacitance is calculated like an emitter bypass capacitor in a *CE* circuit.

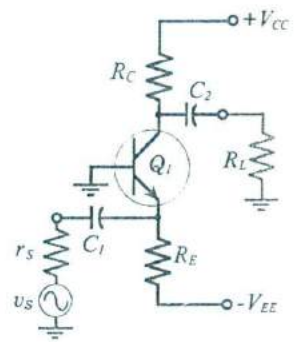


Figure 12-39
A capacitor-coupled CB circuit can be designed in exactly the same way as a CE circuit.

Cascode Amplifier

The very low input impedance of a *CB* circuit (typically 25 Ω) is a major disadvantage. To increase the circuit input impedance while retaining its high frequency performance, the *cascode* amplifier (Fig. 12-40) uses a *CE* input stage driving a *CB* output stage. Transistor Q_1 and its associated components in Fig. 12-40 operates as a *CE* input stage, while the circuit of Q_2 functions as a *CB* output stage.

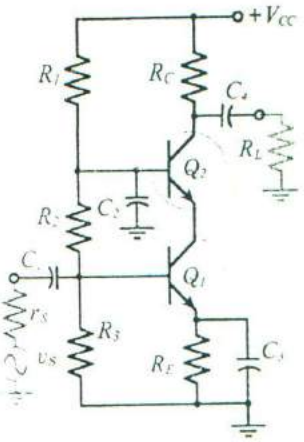


Figure 12-40
A cascode amplifier is like a CB circuit with an additional input transistor (Q_1) that behaves like a CE stage with a gain of one.

The circuit *dc* voltage and current levels are illustrated in Fig. 12-41. It is seen that I_{E1} is set by V_{B1} and R_E. Collector current I_{C1} approximately equals I_{E1}, and I_{E2} is the same current as I_{C1}. So, I_{C2} approximately equals I_{E1}. The current levels remain constant so long as V_{CE1} and V_{CE2} are large enough for transistor operation.

A positive-going *ac* signal at the base of Q_1 produces an increase in I_{E1}, and this results in an I_{C2} increase. Thus, the voltage drop across R_C is increased, producing a decrease in the output voltage. So, there is an *ac* phase inversion between the input and output.

The input impedance at the emitter of Q_2 constitutes the load for the collector of Q_1. Therefore, from Eq. 6-15, the voltage gain from the circuit input to Q_1 collector is,

$$A_{v1} = \frac{-h_{fe} \times (Z_i \text{ to } Q_2)}{h_{ie}} = \frac{-h_{fe} \times [h_{ie}/(1 + h_{fe})]}{h_{ie}}$$

$$\approx -1$$

With an input stage gain of -1, there is no significant Miller effect at the circuit input.

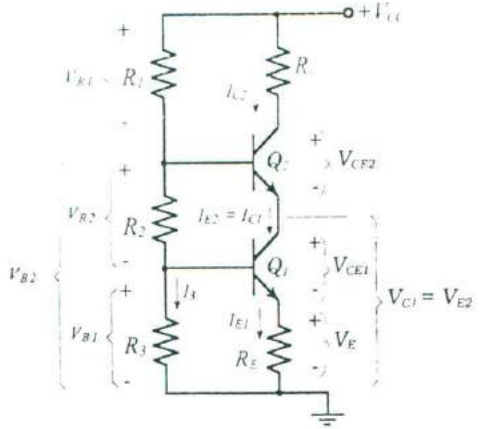


Figure 12-41
DC Voltage levels in a cascode circuit.

From Eq. 6-32, the voltage gain produced by the Q_2 *CB* circuit is,

$$A_{v2} = \frac{h_{fb} \times (R_C \| R_L)}{h_{ib}}$$

Converting to *CE* parameters, the overall voltage gain for the cascode amplifier is the same as that for a *CE* circuit;

$$A_v \approx \frac{-h_{fe} \times (R_C \| R_L)}{h_{ie}}$$

Design Calculations

The design procedure for a cascode amplifier is easily derived from the *CE* design process. The voltage across R_E should typically be 5 V, and the V_{CE} for each transistor should be a minimum of 3 V. The emitter voltage for Q_2 is,

$$V_{E2} = (V_{E1} + V_{CE1})$$

The transistor base voltages are,

$$V_{B1} = (V_{E1} + V_{BE})$$

and,

$$V_{B2} = (V_{E2} + V_{BE})$$

When the voltage and current levels are selected, the resistor values are easily calculated.

The base bypass capacitor (C_2) in Fig. 12-40 should have an impedance equal to one tenth of the h_{ie} of Q_2. This ensures that the impedance looking into Q_2 emitter terminal is not significantly affected by R_1 and R_2. Also, that no portion of the input signal (at Q_2 base) is developed at Q_1 base.

Example 12-20

Determine suitable resistor values the cascode amplifier circuit in Figs. 12-40 and 12-41 if V_{CC} = 20 V and R_L = 90 kΩ. The transistor parameters are h_{fe} = 50, h_{ie} = 1.2 kΩ, and h_{ib} = 24 Ω.

Solution

select

$$R_C \approx \frac{R_L}{10} \approx \frac{90\ \text{k}\Omega}{10}$$

$$= 9\ \text{k}\Omega\ (\text{use } 8.2\ \text{k}\Omega \text{ standard value})$$

select

$$V_{CE1(min)} = V_{CE2(min)} = 3\ \text{V}$$

and,

$$V_E = 5\ \text{V}$$

$$V_{RC} = V_{CC} - V_{CE1} - V_{CE2} - V_E = 20\ \text{V} - 3\ \text{V} - 3\ \text{V} - 5\ \text{V}$$

$$= 9\ \text{V}$$

$$I_C = \frac{V_{RC}}{R_C} = \frac{9\ \text{V}}{8.2\ \text{k}\Omega}$$

$$= 1.1\ \text{mA}$$

Eq. 12-27,

$$R_E \approx \frac{V_E}{I_C} = \frac{5\ \text{V}}{1.1\ \text{mA}}$$

$$= 4.5\ \text{k}\Omega\ (\text{use } 4.7\ \text{k}\Omega \text{ standard value})$$

select $R_3 = 10\,R_E = 10 \times 4.7\ \text{k}\Omega$

$= 47\ \text{k}\Omega$

$V_{B1} = V_E + V_{BE} = 5\ \text{V} + 0.7\ \text{V}$

$= 5.7\ \text{V}$

$$I_3 = \frac{V_{B1}}{R_3} = \frac{5.7\ \text{V}}{47\ \text{k}\Omega}$$

$= 121\ \mu\text{A}$

$V_{B2} = V_E + V_{CE1} + V_{BE2} = 5\ \text{V} + 3\ \text{V} + 0.7\ \text{V}$

$= 8.7\ \text{V}$

$V_{R2} = V_{B2} - V_{B1} = 8.7\ \text{V} - 5.7\ \text{V}$

$= 3\ \text{V}$

$$R_2 = \frac{V_{R2}}{I_3} = \frac{3\ \text{V}}{121\ \mu\text{A}}$$

$= 24.8\ \text{k}\Omega$ (use $22\ \text{k}\Omega + 2.7\ \text{k}\Omega$)

$$R_1 = \frac{V_{CC} - V_{B2}}{I_3} = \frac{20\ \text{V} - 8.7\ \text{V}}{121\ \mu\text{A}}$$

$= 93.4\ \text{k}\Omega$ (use $47\ \text{k}\Omega + 47\ \text{k}\Omega$)

Example 12-21

Determine suitable capacitor values for the cascode circuit in Example 12-20 to give a 25 Hz low cutoff frequency. Assume that $r_s << Z_i$.

Solution

$Z_i = h_{ie1} \| R_3 \| R_2 = 1.2\ \text{k}\Omega \| 47\ \text{k}\Omega \| 24.7\ \text{k}\Omega$

$= 1.1\ \text{k}\Omega$

from Eq. 12-4, $$C_1 = \frac{1}{2\pi f_1 (Z_i/10)} = \frac{1}{2\pi \times 25\ \text{Hz} \times (1.1\ \text{k}\Omega/10)}$$

$= 57.9\ \mu\text{F}$ (use 56 μF standard value)

$$C_2 = \frac{1}{2\pi f_1 (h_{ie2}/10)} = \frac{1}{2\pi \times 25\ \text{Hz} \times (1.2\ \text{k}\Omega/10)}$$

$= 53\ \mu\text{F}$ (use 56 μF standard value)

from Eq. 12-2, $$C_3 = \frac{1}{2\pi f_1 h_{ib}} = \frac{1}{2\pi \times 25\ \text{Hz} \times 24\ \Omega}$$

$= 265\ \mu\text{F}$ (use 270 μF standard value)

from Eq. 12-5, $$C_4 = \frac{1}{2\pi f_1 (R_C + R_L)/10} = \frac{1}{2\pi \times 25\ \text{Hz} \times (99\ \text{k}\Omega/10)}$$

$= 0.64\ \mu\text{F}$ (use 0.68 μF standard value)

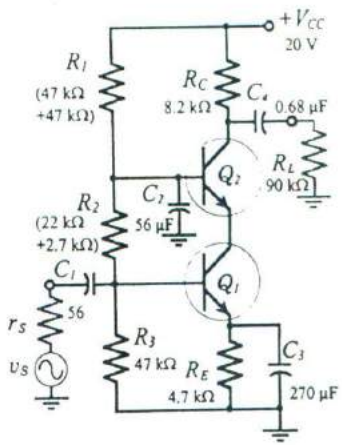


Figure 12-42
Cascode amplifier designed in Examples 12-20 and 12-21.

Differential Amplifier as a High-Frequency Amplifier

The differential amplifier discussed in Section 12-8 can have the same high-frequency performance as a *CB* circuit. The differential amplifier circuit shown in Fig. 12-43, has zero voltage gain from Q_1 base to Q_1 collector, because there is no collector resistor. Consequently, there is no Miller effect on the input capacitance. Also, the amplifier input is applied (via Q_1) to the emitter of Q_2, as in the case of a *CB* circuit. So, there is no Miller effect associated with Q_2. The input impedance (at the base of Q_1) is reasonably high, like a *CE* circuit and unlike the case of a *CB* amplifier.

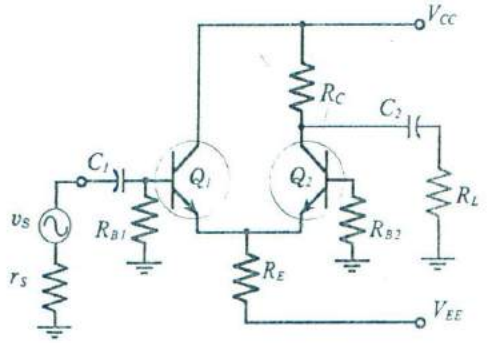


Figure 12-43
A differential amplifier can have a good high frequency response when the input stage has a voltage gain of one, because of the absence of a collector resistor.

Practise Problems

12-9.1 A cascode amplifier circuit as in Fig. 12-40 is to use *2N3904 BJTs* and a 16 V supply. The external load resistor is 33 kΩ. Determine suitable resistor values for the circuit.

12-9.2 Assuming that $r_s << Z_i$, determine suitable capacitor values for the circuit in Problem 12-9.1 to give a 100 Hz lower cutoff frequency. Also, calculate the circuit minimum voltage gain.

12-10 Amplifier Testing

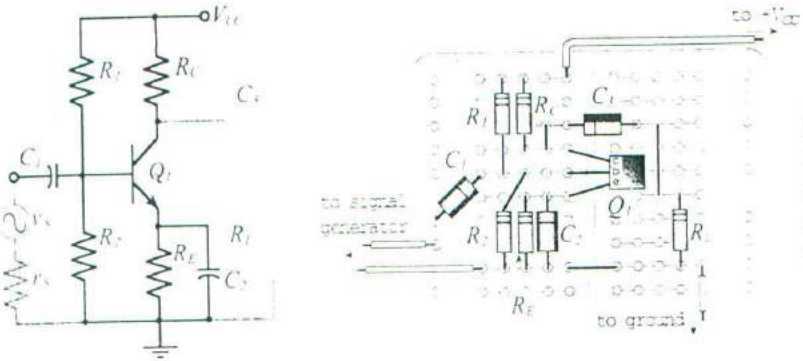
Preparation

Transistor amplifiers and other circuits should be tested in a methodical fashion; otherwise the results obtained may be useless. The circuit should first be carefully constructed in bread-board form, placing the components to resemble the circuit diagram as closely as possible. This makes testing and troubleshooting much easier than when the layout is untidy. Figure 12-24(a) shows a *CE* circuit, and Fig. 12-24(b) illustrates a suitable circuit layout on a plug-in type breadboard.

Instability

After the circuit has been constructed, the power supply should be set to the appropriate voltage and then connected and switched on. An oscilloscope should be connected to monitor the output of

the amplifier to check that the circuit is not oscillating. If the circuit is oscillating, the oscillations must be stopped before proceeding further. For example, *dc* voltage measurements made on an oscillating circuit have absolutely no value.



(a) Amplifier circuit diagram

(b) Breadboarded circuit

Figure 12-44
When constructing a circuit for laboratory testing, the layout of the breadboard should resemble the circuit diagram as closely as possible.

Amplifier instability can be the result of incorrect design or poor circuit layout. It can also be caused by feedback along the conductors from the power supply to the circuit. To stabilize an unstable amplifier, commence by connecting a 0.01 μF (or 0.1 μF, if necessary) decoupling capacitor from the positive supply line to ground, (Fig. 12-45). Where a plus-minus supply is used, connect capacitors from each supply line to ground. *The capacitors must be installed right on the breadboard.* It is useless to place them at power supply terminals.

If the circuit is still unstable, small shunt capacitors should be connected from the transistor collector terminals to ground, or between collector and base, (Fig. 12-45). Start with 50 pF capacitors for this purpose, and increase the capacitance in steps to about 300 pF, as necessary. Normally, these capacitors should not be part of the final circuit. They are usually installed temporarily (if they are required) only until the source of the circuit instability is located.

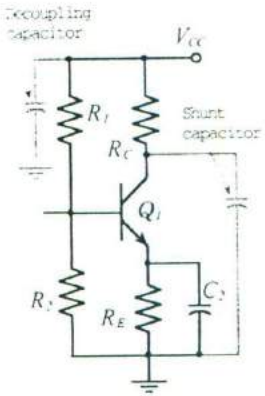


Figure 12-45
Oscillations may be eliminated in an unstable circuit by using power supply decoupling capacitors and/or by employing small shunt capacitors from the transistor collector to ground.

DC Voltage Measurements

Once it is established that the circuit is stable, the next step is to measure the *dc* voltage levels at all transistor terminals. An electronic voltmeter should be used, and every *dc* voltage level should be measured with respect to ground. Some electronic voltmeters have their common terminal capacitor-coupled to ground. So, it is best to keep the voltmeter common terminal grounded at all times. If the *dc* voltages are not satisfactory, they must be corrected before proceeding further. Even when the voltage levels are not exactly as designed, it might be possible to proceed.

The measured *dc* voltage levels should at least show that every *BJT* base-emitter junction is forward biased by the appropriate amount (approximately 0.7 V for silicon transistors and 0.3 V for

germanium devices). The measurements should also show a minimum of 2 V for each collector-emitter voltage drop. *BJT* and *FET* bias circuit trouble-shooting procedures are discussed in Sections 5-6 and 10-6, respectively.

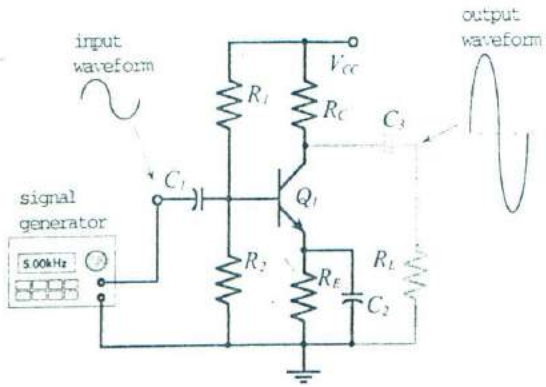


Figure 12-46
For ac testing, a signal generator should be connected at the circuit input, and an oscilloscope should be used to monitor the input and output waveforms.

AC Testing

When satisfactory *dc* levels are established throughout the circuit, *ac* tests may proceed. Connect a signal generator to the input, and connect a two-channel oscilloscope to simultaneously monitor the input and output voltage waveforms. (Fig. 12-46). Adjust the signal frequency to somewhere around the middle of the amplifier bandwidth, and adjust the signal amplitude to give maximum undistorted output voltage. If the signal generator amplitude cannot be set to a low enough level to give an undistorted output, a resistive voltage divider should be employed to further reduce the signal amplitude. (see Fig. 12-47).

The amplifier input and output voltage amplitudes (v_i and v_o) can be measured and the voltage gain can be calculated as $A_v = v_o/v_i$. When a two-stage circuit is being tested, one oscilloscope probe may be moved to monitor the output voltage (v_{o1}) of the first stage. The gain of the first stage is $A_{v1} = v_{o1}/v_i$, and that of the second stage is $A_{v2} = v_o/v_{o1}$.

With the oscilloscope monitoring the input and output waveforms, the frequency response of the circuit may be investigated. The signal voltage level should be maintained constant, and the signal frequency adjusted in convenient steps. At each frequency, v_o should be measured and A_v calculated. The upper and lower cutoff frequencies are found where v_o drops to 0.707 of its normal (mid-frequency) level with v_i still at it normal level.

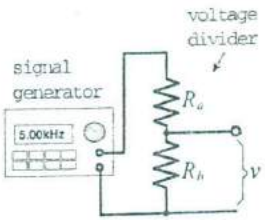


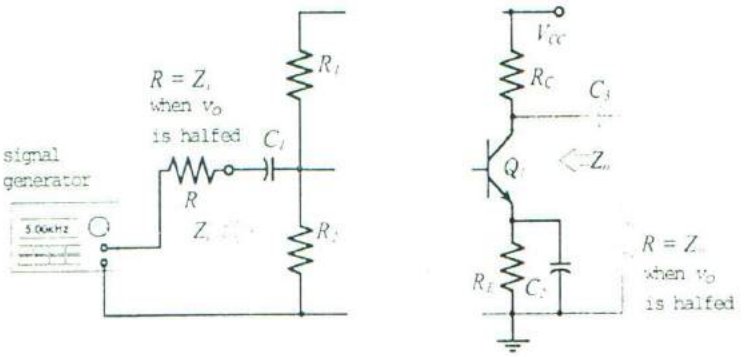
Figure 12-47
A resistive voltage divider might be required to reduce the signal generator amplitude to a low enough level for the circuit input voltage.

Input and Output Impedances

The amplifier input and output impedances should normally be measured with the signal frequency at the middle of the bandwidth. The simplest way to measure the input impedance is to connect a resistor (not a decade box) in series with the circuit input terminal and the signal source, [see Fig. 12-48(a)]. When the

ac output voltage drops to half its normal level, the series-connected resistor equals the input impedance. If the output voltage change is other than half, the input resistance can be calculated using the voltage divider equation.

The output impedance of a circuit may be determined by connecting a resistor as a capacitor-coupled load at the circuit output. [Fig. 12-48(b). The *ac* output voltage is once again halved when the load resistance equals the circuit output impedance.



(a) Input resistance measurement (b) Measurement of output resistance

Figure 12-48
Circuit input impedance is measured by connecting a resistor in series with the circuit input. Output resistance is measured by the use of a capacitor-coupled load resistor.

Section 12-10 Review

12-10.1 Prepare a point form list of the correct test procedure for a two-stage transistor amplifier circuit.

Practise Problem

12-10.1 Refer to the circuit designed in Examples 12-2 and 12-3. Calculate the percentage change in output voltage when a 1 kΩ resistor is connected in series with the signal source and the circuit input. Also, determine the effect on the output voltage when a 27 kΩ resistor is connected in place of the capacitor-coupled load.

Chapter-12 Review Questions

Section 12-1

12-1 Discuss the factors involved in the selection of I_C, R_C, and R_E for a single-stage common-emitter *BJT* amplifier circuit using voltage divider bias. Also, explain the process for determining suitable bias resistors.

12-2 Derive the equation for calculating the value of the emitter bypass capacitor for a single-stage common-emitter *BJT* amplifier using voltage divider bias.

12-3 Write an equation for calculating the coupling capacitors in a capacitor-coupled common-emitter amplifier. Show that, when this equation is used, the coupling capacitors have very little effect on the performance of the circuit.

12-4 Show how a capacitor may be used to obtain a desired upper cutoff frequency in a transistor common-emitter amplifier. Derive the equation for determining the capacitor value.

Section 12-2

12-5 Discuss the factors involved in the selection of I_D, R_D, and R_S for a single-stage common-source *FET* amplifier circuit using voltage divider bias. Also, explain the process for determining suitable bias resistors.

12-6 Derive the equation for calculating the value of the source bypass capacitor for a single-stage common-source amplifier using voltage divider bias.

Section 12-3

12-7 Sketch the circuit of a two-stage capacitor-coupled common-emitter *BJT* amplifier. Briefly explain its operation

12-8 Discuss the lower cutoff frequency for each stage of a two-stage common-emitter amplifier and the lower cutoff frequency for the complete circuit. Also, write equations for calculating the bypass capacitor values for each stage.

12-9 Write equations for calculating the coupling capacitors in a two-stage capacitor-coupled common-emitter amplifier. Explain.

12-10 Sketch the *h*-parameter equivalent circuit for a two-stage common-emitter amplifier. Write equations for Z_i, Z_o, A_{v1}, A_{v2}, and A_v.

Section 12-4

12-11 Sketch the circuit of a two-stage direct-coupled common-emitter amplifier using *npn BJTs*. Discuss the advantages of direct coupling between stages.

12-12 Sketch the *h*-parameter equivalent circuit for the amplifier in Review Question 12-11. Write equations for Z_i, Z_o, and A_v for the circuit.

12-13 Sketch a two-stage, direct-coupled, *BJT* amplifier using an *npn* input stage and a *pnp* output stage. Explain the advantages of using complementary transistors.

Section 12-5

12-14 Sketch the circuit of a two-stage, direct-coupled, *BJT* amplifier using a common-emitter input stage and an emitter follower output stage. Discuss the circuit operation.

12-15 Write equations for Z_i, Z_o, and A_v for the circuit in Review Question 12-14.

Section 12-6

12-16 Sketch the circuit of a *dc* feedback pair with two stages of amplification. Explain the circuit operation, and discuss its advantages and disadvantages.

12-17 Sketch the circuit of a *dc* feedback pair with an amplifier input stage and an emitter follower stage. Explain the capacitor bypassing for this circuit.

Section 12-7

12-18 Sketch the circuit of a two-stage, capacitor-coupled amplifier using an *FET* common-source input stage and a *BJT* common-emitter output stage. Discuss the advantages of this type of *BIFET* circuit.

12-19 Write equations for Z_i, Z_o, and A_v for the circuit in Review Question 12-18.

12-20 Sketch the circuit of a two-stage, direct-coupled amplifier using an *n*-channel *FET* common-source input stage and a *pnp BJT* common-emitter output stage. Explain the advantages of this arrangement.

Section 12-8

12-21 Draw the circuit diagram for a *BJT* differential amplifier: (a) using a single-polarity supply, (b) using a plus/minus supply. Explain the *dc* and *ac* operation of each circuit, and discuss the advantages and disadvantages of differential amplifiers.

12-22 Write equations voltage gain and impedance equations for a differential amplifier circuit.

Section 12-9

12-23 Sketch the circuit of a single-stage, capacitor-coupled common base amplifier, and then show the modifications required to convert it to a cascode amplifier. Explain the operation of the cascode amplifier.

12-24 Derive an equation for a cascode amplifier voltage gain. Also, write equations for input and output impedance.

12-25 Sketch a differential amplifier circuit for high-frequency use. Explain its advantages in this application.

Section 12-10

12-26 Briefly explain the measures that should be taken to stop a laboratory-constructed circuit from oscillating.

12-27 List the correct procedure for testing a laboratory-constructed amplifier circuit for voltage gain, frequency response, input impedance, and output impedance.

Chapter-12 Problems

Section 12-1

12-1 A single-stage, *BJT*, common-emitter amplifier with voltage divider bias is to be designed to use a *2N3903* transistor. A 15 V supply is to be used and 70 kΩ load resistor is to be capacitor-coupled to the output. Sketch the circuit and determine suitable resistor values.

12-2 Determine suitable capacitor values for the circuit in Problem 12-1 to give a 60 Hz lower cutoff frequency and a 60 kHz upper cutoff frequency. The signal source resistance is 300 Ω.

12-3 Analyze the circuit designed for Problems 12-1 and 12-2 to determine A_v, Z_i, and Z_o.

12-4 A single-stage common-emitter amplifier using a *2N3906* transistor with voltage divider bias is to be designed to have V_{CC} = 18 V, and R_L = 56 kΩ. Sketch the circuit and determine suitable resistor values.

12-5 The circuit in Problem 12-5 to have f_1 = 80 Hz and f_2 = 75 kHz. The signal source resistance is 500 Ω. Determine suitable capacitor values.

12-6 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-4 and 12-5.

12-7 A single-stage common-emitter amplifier with voltage divider bias is to use a *2N3904* transistor with V_{CC} = 12 V. The circuit is to be designed to have $Z_o \approx 3.9$ kΩ. Sketch the circuit and determine suitable resistor values.

12-8 The circuit in Problem 12-7 is to have f_1 = 50 Hz, R_L = 47 kΩ, and a signal source resistance r_s = 600 Ω. Determine suitable capacitor values.

12-9 Determine A_v, Z_i, and Z_o for the circuit designed for Problems 12-7 and 12-8.

Section 12-2

12-10 A single-stage common-source amplifier with voltage divider bias is to use a *2N5457 FET* with V_{DD} = 22 V and R_L = 70 kΩ. Sketch the circuit and determine suitable resistor values.

12-11 Determine suitable capacitor values for the circuit in Problem 12-10 to give a 60 Hz lower cutoff frequency and a 60 kHz upper cutoff frequency. The signal source resistance is 300 Ω.

12-12 Analyze the circuit designed for Problems 12-10 and 12-11 to determine A_v, Z_i, and Z_o.

12-13 A single-stage common-source amplifier using a *2N5458 FET* with voltage divider bias is to have to have V_{DD} = 25 V.

and R_L = 56 kΩ. Sketch the circuit and determine suitable resistor values.

12-14 The circuit in Problem 12-13 to have f_1 = 75 Hz and f_2 = 90 kHz. The signal source resistance is 500 Ω. Determine suitable capacitor values.

12-15 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-13 and 12-14.

12-16 A single-stage common-source amplifier with voltage divider bias is to use a *2N5459 FET* with V_{DD} = 20 V. The circuit is to be designed to have Z_i = 500 kΩ and Z_o = 5 kΩ. Draw the circuit diagram and determine suitable resistor values.

12-17 The circuit in Problem 12-16 is to have f_1 = 80 Hz, R_L = 47 kΩ, and a signal source resistance r_S = 600 Ω. Determine suitable capacitor values.

12-18 Determine A_v, Z_i, and Z_o for the circuit designed for Problems 12-16 and 12-17.

Section 12-3

12-19 A two-stage, capacitor-coupled, common-emitter amplifier is to be designed to have Z_o = 3.9 kΩ. The circuit is to use *2N3903* transistors with V_{CC} = 12 V. Draw the complete circuit diagram and calculate suitable resistor values.

12-20 The circuit in Problem 12-19 to have f_1 = 100 Hz, R_L = 47 kΩ, and r_S = 600 Ω. Determine suitable capacitor values.

12-21 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-19 and 12-20.

12-22 A two-stage, capacitor-coupled, common-emitter amplifier is to be designed to use *2N3906 pnp* transistors with V_{CC} = 18 V and R_L = 60 kΩ. Draw the circuit diagram and calculate suitable resistor values.

12-23 The circuit in Problem 12-22 to have f_1 = 120 Hz and f_2 = 82 kHz. The signal source resistance is r_S = 600 Ω. Determine suitable capacitor values.

12-24 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-22 and 12-23.

Section 12-4

12-25 A two-stage, direct-coupled, common-emitter amplifier is to be designed to use *2N3903* transistors with V_{CC} = 16 V. The capacitor-coupled load is R_L = 75 kΩ, and the signal source resistance is r_s = 200 Ω. Draw the circuit diagram and calculate suitable resistor values.

12-26 Determine suitable capacitor values for the circuit in Problem 12-25. The lower cutoff frequency is to be 90 Hz.

12-27 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-25 and 12-26.

12-28 A two-stage, direct-coupled, common-emitter amplifier is to be designed to use a *2N3904 npn* transistor as *stage 1*, and a *2N3906 pnp* device as *stage 2*. The circuit is to have V_{CC} = 17 V and R_L = 85 kΩ. Draw the circuit diagram and calculate suitable resistor values.

12-29 The circuit in Problem 12-28 to have f_l = 55 Hz. Determine suitable capacitor values if r_s = 600 Ω.

12-30 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-28 and 12-29.

12-31 A two-stage, direct-coupled, common-emitter amplifier is to use a *2N3905 pnp* transistor as *stage 1*, and a *2N3903 npn* device as *stage 2*. The circuit is to have V_{CC} = 11 V, R_L = 75 kΩ, f_l = 80 Hz, and r_s = 300 Ω. Sketch the circuit diagram and determine suitable resistor and capacitor values.

Section 12-5

12-32 A two-stage, direct-coupled, common-emitter amplifier with an emitter follower output is to be designed to use *2N3904* transistors. The circuit is to have V_{CC} = 16 V, R_L = 65 Ω, f_l = 50 Hz, and $v_o \approx \pm 75$ mV. Sketch the circuit and determine suitable resistor and capacitor values. Take r_s = 300 Ω.

12-33 Analyze the circuit designed for Problem 12-32 to calculate the overall voltage gain.

12-34 Design a two-stage, direct-coupled, common-emitter amplifier with an emitter follower output. The circuit is to use *2N3906 BJTs* with V_{CC} = 18 V. The load is R_L = 85 Ω, the lower cutoff frequency is f_l = 65 Hz, the output voltage is $v_o \approx \pm 55$ mV, and r_s = 100 Ω. Draw the circuit diagram and determine suitable resistor and capacitor values.

12-35 Determine the overall voltage gain for the amplifier circuit in Problem 12-34.

Section 12-6

12-36 A *dc* feedback pair with two stages of amplification is to be designed to use *2N3904* transistors. The circuit is to have V_{CC} = 18 V, R_L = 50 kΩ, f_l = 75 Hz, and r_s = 100 Ω. Sketch the circuit and determine suitable component values.

12-37 Analyze the circuit designed for Problem 12-36 to calculate the overall voltage gain.

12-38 A *dc* feedback pair with two stages of amplification is to be designed to use *2N3906 BJTs* and to have V_{CC} = 15 V, R_L = 60 kΩ, f_l = 150 Hz, and r_s = 220 Ω. Draw the circuit diagram and determine suitable component values.

12-39 A *dc* feedback pair with an emitter follower output stage is to use *2N3904 BJTs*, to have V_{CC} = 14 V, R_L = 40 Ω, r_s = 200 Ω, f_l = 60 Hz, and $v_o \approx \pm 65$ mV. Determine suitable component values.

12-40 Analyze the circuit designed for Problem 12-39 to calculate A_v, Z_i, and Z_o.

12-41 A *dc* feedback pair with an emitter follower output stage is to use *2N3906 BJTs*. The circuit is to have V_{CC} = 9 V, R_L = 100 Ω, and f_1 = 75 Hz, and $v_o \approx \pm 75$ mV. Sketch the circuit and determine suitable resistor and capacitor values.

12-42 Calculate A_v, Z_i, and Z_o for the circuit in Problem 12-41.

Section 12-7

12-43 A two-stage, capacitor-coupled, *BIFET* amplifier using a common-source input stage and a common-emitter output stage is to be designed to use a *2N5459 FET* and a *2N3904 BJT*. The external load resistance is 120 kΩ, the supply is 22 V, and the circuit input impedance is 800 kΩ. Draw the circuit diagram and calculate suitable resistor values.

12-44 The circuit in Problem 12-43 is to have f_1 = 140 Hz. Assuming that r_s = 220 Ω, determine suitable capacitor values.

12-45 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-43 and 12-44.

12-46 A two-stage, direct-coupled, *BIFET* amplifier using a common-source input stage with a *2N5457 FET* and a common-emitter output stage with a *2N3906 pnp BJT* is to be designed. The external load resistance is 100 kΩ, the supply is 25 V, and the circuit input impedance is to be approximately 300 kΩ. Draw the circuit diagram and calculate suitable resistor values.

12-47 The circuit in Problem 12-46 to have f_1 = 80 Hz. Determine suitable capacitor values. Assume that r_s = 800 Ω.

12-48 Calculate A_v, Z_i, and Z_o for the circuit designed for Problems 12-46 and 12-47.

12-49 Design a two-stage, capacitor-coupled, *BIFET* amplifier circuit using a *2N5486 FET* with self bias for Q_1 and a voltage divider biased *2N3904 BJT* for Q_2. The circuit specification is: V_{CC} = 23 V, R_L = 200 kΩ, f_1 = 80 Hz. For the *2N5486*, Y_{fs} = 6000 μS typical, 8000 μS maximum, I_{DSSmax} = 20 mA, and $V_{P(max)}$ = -6 V. Assume $r_s << Z_i$.

12-50 Calculate A_v, Z_i, and Z_o for the circuit in Problem 12-49.

12-51 Redesign the circuit in Problem 12-49 to use a *2N3905 pnp BJT* for the second stage with direct coupling between stages.

Section 12-8

12-52 A differential amplifier is to be designed to use *2N3904 BJTs*. The external capacitor-coupled load resistance is 120 kΩ, and the supply is ±12 V. Draw the circuit diagram and calculate suitable resistor values.

12-53 Determine suitable capacitor values for the circuit in Problem 12-52 to give f_l = 100 Hz. Assume that r_s = 600 Ω.

12-54 Determine A_v, Z_i, and Z_o for the circuit designed for Problems 12-52 and 12-53.

12-55 A differential amplifier is to use *2N3903 BJTs* with a 15 V supply. The external load resistance is 66 kΩ, the signal source resistance is 600 Ω, and the lower cutoff frequency is to be 75 Hz. Draw the circuit diagram and determine suitable resistor and capacitor values. Assume $r_s << Z_i$.

12-56 Determine A_v, Z_i, and Z_o for the circuit in Problem 12-55.

Section 12-9

12-57 Design a common-base *BJT* amplifier to use a *2N3904* transistor. The specification is: V_{CC} = 9 V, R_L = 27 kΩ, and f_l = 75 Hz. Sketch the circuit and determine suitable resistor and capacitor values.

12-58 Calculate A_v, Z_i, and Z_o for the circuit in Problem 12-57.

12-59 Design a cascode amplifier to use *2N3904* transistors. The specification is: V_{CC} = 19 V, R_L = 47 kΩ, and f_l = 85 Hz. Draw the circuit diagram and calculate suitable resistor and capacitor values.

12-60 Analyze the circuit in Problem 12-59 to determine A_v, Z_i, and Z_o.

Section 12-10

12-61 The output voltage of a transistor amplifier under test falls from ±2 V to ±1.5 V when a 4.7 kΩ resistor is connected in series with the 600 Ω source resistance and the circuit input. Calculate the circuit input resistance.

12-62 Determine the output resistance of a transistor amplifier if v_o changes from ±1 V to ±1.2 V when the capacitor-coupled 60 kΩ load resistance is disconnected.

12-63 The voltage gain of the first stage of a two-stage *BJT* amplifier drops from 300 to 66 when the second stage is connected. The first stage uses a 6.8 kΩ collector resistor. Calculate the input impedance of the second stage.

Practise Problem Answers

12-1.1 150 Ω, 33 kΩ, 6.8 kΩ, 3.3 kΩ
12-1.2 27 μF, 200 μF, 0.56 μF
12-2.1 3.3 MΩ, 1 MΩ, 8.2 kΩ, 8.2 kΩ
12-2.2 0.068 μF, 30 μF, 0.5 μF
12-3.1 100 kΩ, 56 kΩ, 8.2 kΩ, 5.6 kΩ, 100 kΩ, 56 kΩ, 8.2 kΩ, 5.6 kΩ
12-3.2 15 μF, 180 μF, 25 μF, 180 μF, 0.25 μF
12-3.3 14 616
12-4.1 (150 kΩ + 15 kΩ), 56 kΩ, 5.6 kΩ, 5.6 kΩ, 1.8 kΩ, 5.6 kΩ

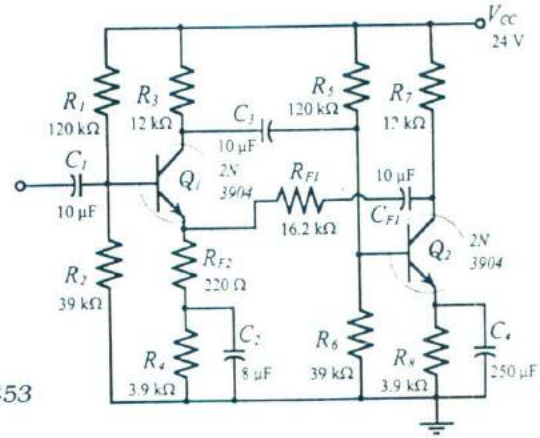
12-4.2 47 μF, 1000 μF, 500 μF, 1 μF
12-4.3 37 338
12-5.1 47 kΩ, (82 kΩ + 1.5 kΩ), 4.7 kΩ, 6.8 kΩ, 2.7 kΩ
12-5.2 15 μF, 250 μF, 39 μF, -182
12-6.1 10 kΩ, 220 kΩ, 4.7 kΩ, 3.3 kΩ
12-6.2 33 μF, 180 μF, 0.68 μF, 9737
12-7.1 $C_2 = 15\,\mu$F, $C_3 = 2\,\mu$F, $C_4 = 250\,\mu$F
12-7.2 5541
12-8.1 56 kΩ, 22 kΩ, 10 kΩ, 2.2 kΩ, 10 kΩ, 56 kΩ, 22 kΩ
12-8.2 1.2 μF, 0.2 μF, 454
12-9.1 (39 kΩ + 3.3 kΩ), (15 kΩ + 2.2 kΩ), 33 kΩ, 3.3 kΩ, 3.3 kΩ
12-9.2 18 μF, 18 μF, 180 μF, 0.47 μF, -300
12-10.1 -39%, -24%

Chapter 13

Amplifiers with Negative Feedback

Chapter Contents

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Objectives

You will be able to:

1. Using diagrams, explain series voltage negative feedback. List its effects on amplifier performance, and write voltage gain and impedance equations.
2. Sketch the following amplifier circuits using series voltage negative feedback, and explain the operation of each:
   - Two-stage, BJT capacitor-coupled
   - Complementary BJT direct-coupled
   - DC feedback pair
   - Two-stage BIFET
   - Differential-input
3. Analyze each of the circuit types listed in item 3 to determine its performance characteristics.
4. Design each of the circuit types listed in item 3 to fulfil a given specification.
5. Explain emitter current feedback. List its effects, and write voltage gain and impedance equations.
6. Design and analyze emitter current feedback circuits.
7. Explain p arallel current negative feedback. List its effects, and write current gain and impedance equations.
8. Design and analyze parallel current negative feedback circuits.
9. Explain the effects of negative feedback on circuit bandwidth, distortion, and phase shift, and make related calculations.

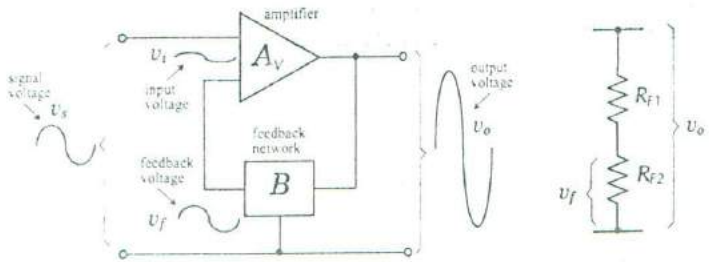
Introduction

Negative feedback is produced by feeding a portion of an amplifier output back to the input where it behaves as an additional signal. The feedback quantity is applied in opposition to the signal, so that the effective input is reduced. This results in stabilized amplifier gain, extended bandwidth, reduced distortion, and modified input and output impedances. *Series voltage feedback* increases input impedance; *parallel current feedback* reduces input impedance. The most important advantage of negative feedback is that it produces amplifiers with stable, predictable, voltage gains.

13-1 Series Voltage Negative Feedback

Negative Feedback Concept

In a negative feedback amplifier, a small portion of the output voltage is fed back to the input. When the feedback voltage is applied in series with the signal voltage, the arrangement is *series voltage feedback*. The instantaneous polarity of the feedback voltage is normally opposite to the signal voltage polarity, (they are in *series-opposition*). So, the feedback voltage is *negative* with respect to the signal voltage; hence the term *negative feedback*.



(a) Negative feedback amplifier (b) Feedback network

Figure 13-1
In a negative feedback amplifier a portion of the output is fed back to the input. The instantaneous polarity of the feedback voltage (v_f) is negative with respect to the signal voltage (v_s).

Consider the illustration in Fig. 13-1(a). An amplifier with two input terminals and one output is shown (in triangular representation). The amplifier has a voltage gain (A_v), and its output voltage (v_o) is applied to a feedback network that reduces v_o by a factor (B) to produce a feedback voltage (v_f). The feedback network may be as simple as the resistive voltage divider shown in Fig. 13-1(b). At the amplifier input, the instantaneous level of v_f is applied negative with respect to v_s, so that the amplifier input terminal voltage is,

$$v_i = v_s - v_f$$

Because the amplifier input voltage is lower than the signal voltage, the output voltage is lower than that produced when negative feedback is not used. This means, of course, that the

overall voltage gain (v_o/v_i) is reduced by negative feedback. However, as will be demonstrated, the stability of the voltage gain is greatly improved with negative feedback.

Voltage gain

Consider the feedback amplifier illustrated in Fig. 13-2, and recall that v_i is amplified to produce v_o, and that v_o is divided by the feedback network to produce v_f. Also, that v_f is applied (along with v_s) to the amplifier input. It is seen that there is a *closed loop* from the amplifier input to the output, and then back to the input. Because of this closed loop, the overall voltage gain with negative feedback is termed the *closed-loop gain* (A_{CL}).

When the feedback network is disconnected, the loop is opened, and the gain without feedback is referred to as the *open-loop gain* (A_v). Alternative symbols sometimes used for the open-loop gain are A_{OL} and $A_{v(OL)}$.

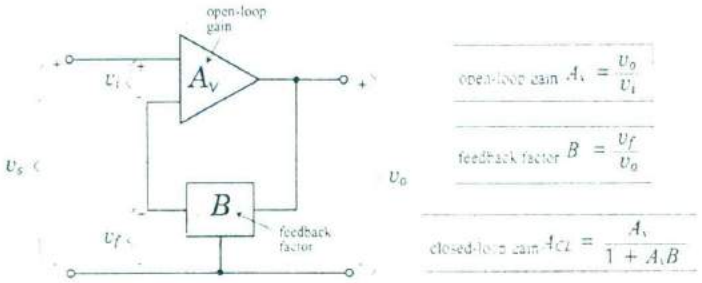


Figure 13-2
Open-loop voltage gain, feedback factor, and closed-loop voltage gain for a negative feedback amplifier.

The overall voltage gain (closed-loop gain) of the amplifier in Fig. 13-2 is,

$$A_{CL} = \frac{v_o}{v_s}$$

and the *feedback factor* is,

$$B = \frac{v_f}{v_o} \qquad \textbf{(13-1)}$$

The input voltage is,

$$v_i = v_s - v_f$$

so,

$$v_i = v_s - Bv_o$$

also,

$$v_o = A_v v_i = A_v(v_s - Bv_o)$$

$$= A_v v_s - A_v B v_o$$

or,

$$v_o(1 + A_v B) = A_v v_s$$

giving,

$$\frac{v_o}{v_s} = \frac{A_v}{1 + A_v B}$$

So, the equation for overall voltage gain with negative feedback is,

$$A_{CL} = \frac{A_v}{1 + A_v B} \qquad \textbf{(13-2)}$$

Analysis of any transistor amplifier not using negative feedback shows that the voltage gain has a wide range, depending on the actual h_{fe} values of the transistors used. Consequently, the open-loop gain of a negative feedback amplifier can vary significantly. However, as demonstrated in Ex. 13-1, the closed loop gain can be a very stable quantity.

Example 13-1

Calculate the closed-loop gain for the negative feedback amplifier shown in Fig. 13-3. Also, calculate the closed loop gain when the open-loop gain is changed by ±50%. Note that $A_v = 100\,000$ and $B = 1/100$.

Solution

when $A_v = 100\,000$,

Eq. 13-2, $$A_{CL} = \frac{A_v}{1 + A_v B} = \frac{100\,000}{1 + (100\,000/100)}$$

$$= 99.9$$

when $M = 150\,000$,

Eq. 13-2, $$A_{CL} = \frac{A_v}{1 + A_v B} = \frac{150\,000}{1 + (150\,000/100)}$$

$$= 99.93$$

when $M = 50\,000$,

Eq. 13-2, $$A_{CL} = \frac{A_v}{1 + A_v B} = \frac{50\,000}{1 + (50\,000/100)}$$

$$= 99.8$$

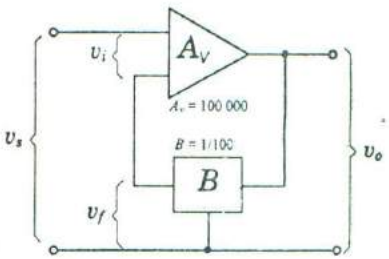


Figure 13-3
Negative feedback amplifier for Ex. 13-1.

Example 13-1 shows that when the open-loop gain changes by ±50% the closed-loop gain of the negative feedback amplifier remains stable within ±0.1%. Thus,

series-voltage negative feedback stabilizes amplifier voltage gain.

Amplifier gain stabilization is the most important advantage of negative feedback amplifiers. Amplifiers that are required to have stable voltage gain are always designed as negative feedback amplifiers. Examination of Eq. 13-2 reveals that if $A_v B >> 1$, then

$$A_{CL} \approx \frac{1}{B} \qquad \textbf{(13-3)}$$

From Eq. 13-3, it is seen that to design a negative feedback amplifier with a particular closed-loop gain, it is only necessary to design the feedback network to give $A_{CL} = 1/B$. For example, for $A_{CL} = 100$, $B = 1/100$. It must be remembered that for Eq. 13-3 to be correct, $A_v B >> 1$, or

$$A_v >> \frac{1}{B}$$

which means that,

$$A_v >> A_{CL}$$

Thus, for satisfactory operation of a negative feedback amplifier,

the open-loop voltage gain must be much greater than the required closed-loop gain.

In general, for A_{CL} to be stable within ±1%, A_v should be equal to or greater than 100 A_{CL}.

Input Impedance

The input impedance of a *BJT* amplifier without negative feedback is typically the impedance *looking into* the base of a transistor. If no negative feedback is present in the amplifier in Fig. 13-4, the input impedance is,

$$Z_b = \frac{v_i}{i_i}$$

and this gives,

$$i_i = \frac{v_i}{Z_b}$$

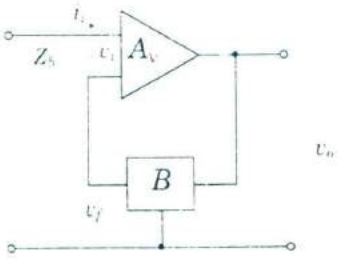


Figure 13-4
The input impedance of an amplifier is increased by a factor of (1 + $A_v B$) when series voltage negative feedback is employed.

With negative feedback, the input impedance is,

$$Z_i = \frac{v_s}{i_i} = \frac{v_s \times Z_b}{v_i} \qquad (1)$$

and,

$$\begin{aligned} v_i &= v_s - v_f \\ &= v_s - Bv_o \\ &= v_s - A_v Bv_i \end{aligned}$$

or,

$$v_i(1 + A_v B) = v_s \qquad (2)$$

Substituting for v_s from Eq. 2 into Eq. 1 gives,

$$\mathbf{Z_i = (1 + A_v B)Z_b} \qquad \mathbf{(13\text{-}4)}$$

where Z_i is the input impedance with negative feedback, and Z_b is the input impedance without negative feedback. It is seen that

series voltage feedback increases the input impedance of an amplifier by a factor of $\mathbf{(1 + A_v B)}$.

This is the same factor involved in gain reduction.

Input Impedance with Bias Resistors

The bias resistors at the input of a transistor circuit (*BJT* or *FET*) are not normally affected by series voltage negative feedback, (see Fig. 13-5). This is because the bias resistors are outside the feedback loop. The circuit input resistance in Fig 13-5 is,

$$\mathbf{Z_{in} = Z_i \| R_1 \| R_2} \qquad \mathbf{(13\text{-}5)}$$

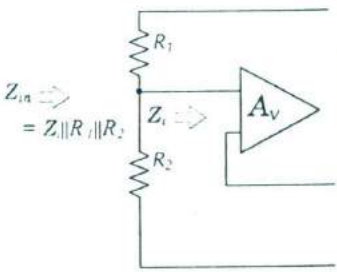


Figure 13-5
The bias resistors at the input of an amplifier are not affected by negative feedback.

Example 13-2

The input impedance of the amplifier in Fig. 13-6 is $Z_b = 1\ k\Omega$ when negative feedback is not used, and the open-loop voltage gain is 100 000. Calculate the circuit input impedance with negative feedback.

Solution

From Eq. 13-1,
$$B = \frac{v_f}{v_o} = \frac{R_{F2}}{R_{F1} + R_{F2}} = \frac{560\ \Omega}{560\ \Omega + 56\ k\Omega}$$
$$= \frac{1}{101}$$

Eq. 13-4,
$$Z_i = (1 + A_v B)Z_b = [1 + (\frac{100\,000}{101})] \times 1\ k\Omega$$
$$= 991\ k\Omega$$

Eq. 13-5,
$$Z_{in} = Z_i \| R_1 \| R_2 = 991\ k\Omega \| 68\ k\Omega \| 33\ k\Omega$$
$$= 21.7\ k\Omega$$

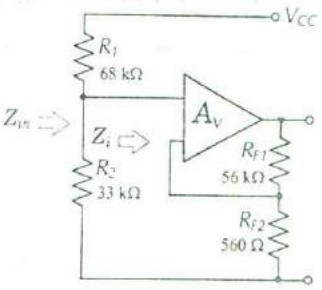


Figure 13-6
Negative feedback amplifier for Ex. 13-2.

Output Impedance

To derive an equation for the output impedance of a negative feedback amplifier, refer to Fig. 13-7. This is similar to the circuit of Fig. 13-1, but showing the internal impedance at the amplifier output terminal. The input terminals are short-circuited, so that v_f is the only voltage at the amplifier input. The output impedance without feedback is identified as Z_o (the output impedance at a *BJT* collector terminal, normally equal to $1/h_{oe}$).

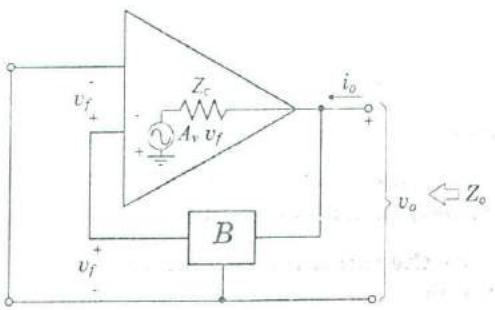


Figure 13-7
The output impedance of an amplifier is reduced by a factor of $(1 + A_v B)$ by series voltage negative feedback.

The output voltage (v_o) produces the feedback voltage (v_f), and this generates a voltage $A_v v_f$ in series with Z_o, as illustrated. Assuming an instantaneous positive polarity for v_o, the output current (i_o) occurs in the direction shown.

Writing an equation for the voltage drops around the output circuit of the negative feedback amplifier,

$$v_o = i_o Z_o - A_v v_f$$

or,
$$\begin{aligned} i_o Z_c &= v_o + A_v v_f \\ &= v_o + A_v B v_o \\ &= v_o(1 + A_v B) \end{aligned}$$

The output impedance of the negative feedback amplifier is,

$$Z_o = \frac{v_o}{i_o}$$

so,
$$\mathbf{Z_o = \frac{Z_c}{1 + A_v B}} \qquad \textbf{(13-6)}$$

In Eq. 13-6, Z_o is the output impedance with negative feedback, and Z_c is the output impedance without negative feedback. So,

series voltage feedback reduces the output impedance of an amplifier by a factor of $\mathbf{(1 + A_v B)}$.

This is the same factor involved in the reduction of amplifier gain, and in the increase of the input impedance.

Output Impedance with a Collector Resistor

The collector resistor in the second stage of a two-stage circuit is not normally affected by series voltage negative feedback, (see Fig. 13-8). This is because (like the case of input bias resistors) the collector resistor is outside the feedback loop.

Recall from Section 6-4 that, for a *CE* circuit, $Z_c = 1/h_{oe}$, and $Z_o = R_C \| (1/h_{oe})$. Because $1/h_{oe}$ is usually much larger than R_C, Z_o is usually taken as equal to R_C when there is no feedback involved. However, with negative feedback, the collector output impedance is much lower than $1/h_{oe}$.

From Eq. 13-6,
$$Z_o = \frac{1/h_{oe}}{1 + A_v B}$$

So, the circuit output impedance should be calculated as,

$$\mathbf{Z_{out} = R_C \| Z_o} \qquad \textbf{(13-7)}$$

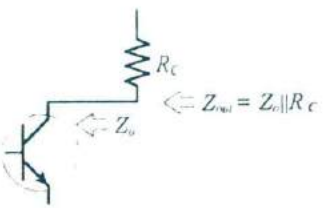


Figure 13-8
The output impedance at the collector of Q_2 is $R_C \| Z_o$. Resistor R_C is not affected by negative feedback.

Example 13-3

The amplifier circuit in Fig. 13-9 (reproduced from Fig. 12-21) is designed and analyzed in Examples 12-8 through 12-10. The input impedance at the base of Q_1 is Z_b = 1 kΩ, and Q_2 has $1/h_{oe}$ = 50 kΩ. Calculate the circuit input and output impedances when negative feedback is used with a feedback factor of 1/100.

Solution

Eq. 13-4,
$$Z_i = (1 + A_v B)Z_b = [1 + (\frac{7533}{100})] \times 1\ \text{k}\Omega$$
$$= 76\ \text{k}\Omega$$

Eq. 13-5, $Z_{in} = Z_i \| R_1 \| R_2 = 76\ \text{k}\Omega \| 68\ \text{k}\Omega \| 47\ \text{k}\Omega$
$= 20.3\ \text{k}\Omega$

Eq. 13-6, $Z_o = \dfrac{1/h_{oe}}{1 + A_v B} = \dfrac{50\ \text{k}\Omega}{1 + (7533/100)}$
$= 655\ \Omega$

Eq. 13-7, $Z_{out} = R_C \| Z_o = 3.9\ \text{k}\Omega \| 655\ \Omega$
$= 560\ \Omega$

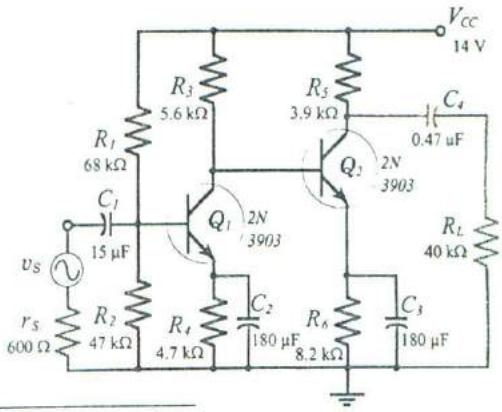


Figure 13-9
Amplifier circuit for Ex. 13-3.

Practise Problems

13-1.1 A *BJT* amplifier with an open-loop gain of 350 000 has transistor parameters of $h_{ie} = 1.5\ \text{k}\Omega$, $h_{fe} = 100$, and $1/h_{oe} = 73\ \text{k}\Omega$. The input bias resistors are $R_1 = 82\ \text{k}\Omega$ and $R_2 = 39\ \text{k}\Omega$, and the output collector resistor is $R_C = 5.6\ \text{k}\Omega$. Negative feedback is applied with $B = 1/135$. Calculate Z_{in} and Z_{out} without negative feedback and with negative feedback. Also, determine the closed-loop gain.

13-2 Two-Stage CE Amplifier with Series Voltage Negative Feedback

Negative Feedback Amplifier Circuit

A two-stage, capacitor-coupled *BJT* amplifier is shown in Fig. 13-10. This is the same two-stage *CE* circuit discussed in Section 12-3 with the addition of feedback components R_{F2}, R_{F1}, and C_{F1}. These components constitute the feedback network referred to in Section 13-1. The output voltage is divided across R_{F2} and R_{F1} to produce a feedback voltage in series with the signal at the base of Q_1.

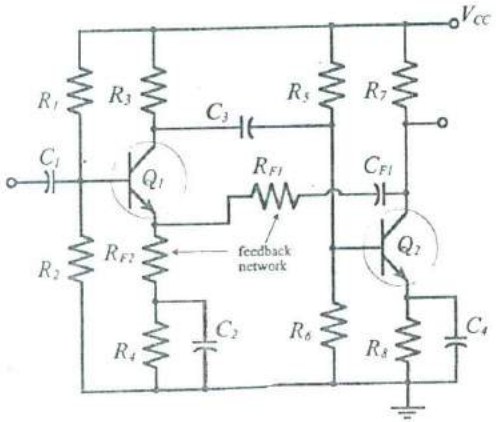


Figure 13-10
Two-stage capacitor-coupled BJT amplifier using series voltage negative feedback. R_{F1}, R_{F2}, and C_{F1} constitute the feedback network.

C_{F1} (in Fig. 13-10) is a *dc* blocking capacitor to prevent the *dc* voltage at Q_2 collector from affecting the Q_1 bias conditions. C_{F1} behaves as an open-circuit to *dc* and a short-circuit to *ac*. Consequently, C_{F1} is not included in the mid-frequency *ac* equivalent circuit of the feedback network in Fig. 13-11. Capacitor C_2 behaves as a short-circuit at middle and higher frequencies, so C_2 and R_4 (shorted by C_2) are also absent from the mid-frequency *ac* equivalent circuit.

The signal voltage (v_s) is applied between Q_1 base and ground, as illustrated in Fig. 13-11, and the output voltage (v_o) is developed between Q_2 collector and ground. The feedback voltage (v_f) is developed across resistor R_{F2}, between the Q_1 emitter terminal and ground. The input voltage (v_i) appears across the Q_1 base-emitter terminals as the difference between v_s and v_f.

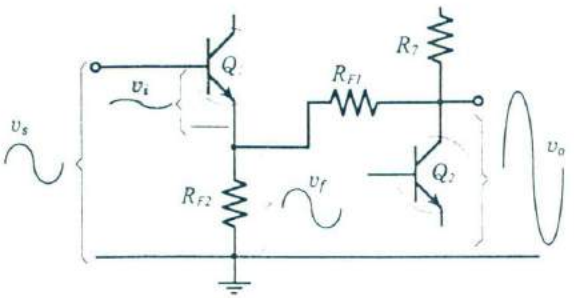


Figure 13-11
Mid-frequency ac equivalent circuit for the feedback network in the circuit of Fig. 13-10.

From previous studies of a two-stage amplifier circuit (Section 12-3), it is known that the circuit output voltage is in phase with the signal voltage. When the instantaneous level of v_s is positive-going, v_o is also positive-going, and consequently v_f is in *phase-opposition* with v_s. When v_s goes up (positively), v_f also goes up, and consequently, the voltage (v_i) at the base-emitter of Q_1 is reduced from v_s to,

$$v_i = v_s - v_f$$

Note that the Q_1 bias resistors (R_1 and R_2) in Fig. 13-10 are outside the feedback loop, and are unaffected by feedback, (as discussed in Section 13-1). The impedance *looking-into* the transistor base is within the feedback loop, so it is altered by feedback. Also, recall that the Q_2 collector resistor (R_7) is unaffected by negative feedback, and that the impedance *looking-into* the transistor collector terminal is changed by negative feedback.

The feedback factor for the circuit in Figs. 13-10 and 13-11 is,

$$B = \frac{R_{F2}}{R_{F1} + R_{F2}} \qquad (13\text{-}8)$$

From Eq. 13-3,

$$A_{CL} \approx \frac{R_{F1} + R_{F2}}{R_{F2}} \qquad (13\text{-}9)$$

Usually $R_{F1} >> R_{F2}$, so $$A_{CL} \approx \frac{R_{F1}}{R_{F2}} \qquad (13\text{-}10)$$

Example 13-4

Determine the voltage gain, input impedance, and output impedance for the amplifier in Fig. 13-12. Without the feedback network, the circuit has an open-loop voltage gain of 58 000, an input impedance at Q_1 base of $Z_b = 1$ kΩ, and a Q_2 collector resistance of $1/h_{oe} = 85$ kΩ.

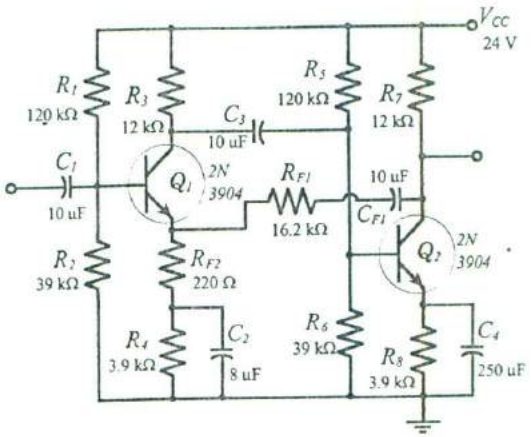


Figure 13-12
Negative feedback amplifier analyzed in Ex. 13-4.

Solution

Eq. 13-8, $$B = \frac{R_{f2}}{R_{F1} + R_{f2}} = \frac{220\ \Omega}{16.2\ \text{k}\Omega + 220\ \Omega}$$
$$= \frac{1}{74.6}$$

Eq. 13-2, $$A_{CL} = \frac{A_v}{(1 + A_v B)} = \frac{58\,000}{1 + (58\,000/74.6)}$$
$$= 74.5$$

or, using Eq. 13-9,
$$A_{CL} \approx \frac{R_{F1} + R_{F2}}{R_{F2}} = \frac{16.2\ \text{k}\Omega + 220\ \Omega}{220\ \Omega}$$
$$= 74.6$$

Eq. 13-4, $$Z_i = Z_b(1 + A_v B) = 1\ \text{k}\Omega[1 + (58\,000/74.6)$$
$$= 778\ \text{k}\Omega$$

Eq. 13-5, $$Z_{in} = Z_i \| R_1 \| R_2 = 778\ \text{k}\Omega \| 120\ \text{k}\Omega \| 39\ \text{k}\Omega$$
$$= 28.4\ \text{k}\Omega$$

Eq. 13-6, $$Z_o = \frac{1/h_{fe}}{(1 + A_v B)} = \frac{85\ \text{k}\Omega}{1 + (58\,000/74.6)}$$
$$= 109\ \Omega$$

Eq. 13-7, $$Z_{out} = R_7 \| Z_o = 12\ \text{k}\Omega \| 109\ \Omega$$
$$= 108\ \Omega$$

Negative Feedback Amplifier Design

A negative feedback amplifier, like the one shown in Fig. 13-12, is best designed first as an amplifier without feedback. The feedback component values are then determined, and the circuit is modified as necessary.

Like R_L, R_{F1} is an additional load at the collector of the second stage in Fig. 13-12. As illustrated in Fig. 13-13, the voltage gain of

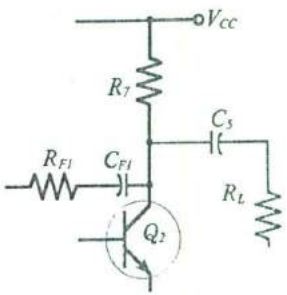


Figure 13-13
The circuit open-loop gain can be reduced by the presence of feedback resistor R_{F1}.

the second stage is proportional to the total load ($R_L \| R_7 \| R_{F1}$), consequently, R_{F1} has the effect of reducing the second stage gain. A large open-loop gain is required for good gain stability, so R_{F1} should be selected as large as possible.

Resistor R_{F2} is an unbypassed resistor in series with the emitter of Q_1. As such, it would seem to reduce the first stage voltage gain, and thus reduce the circuit open-loop gain. However, because v_f is applied to Q_1 emitter, the effective open-loop gain is the voltage gain from the *BE* terminals of Q_1 to the collector of Q_2. So, R_{F2} *does not alter the overall open-loop gain.* (R_{F2} is omitted when calculating the circuit open-loop gain.)

Another consideration for R_{F2} is that it is in parallel with the impedance (Z_{e1}) at the emitter of Q_1, (see Fig. 13-14). Without negative feedback, Z_{e1} would usually equal the transistor h_{ib} value, which is typically 26 Ω when I_C = 1 mA. With negative feedback, Z_{e1} can be shown to range from about 2.5 kΩ to 30 kΩ, depending upon A_v and *B*. Resistor R_{F2} should be selected much smaller than Z_{e1}. However, R_{F2} should be as large as possible to give the largest possible value for R_{F1}; (from Eq. 13-10, $R_{F1} \approx A_{CL} \times R_{F2}$).

A reasonable starting point for feedback network design is to select R_{F2} much lower than $Z_{e1}/10$; in the range of 100 Ω to 470 Ω. R_{F2} could also alter the *dc* bias conditions for Q_1. Consequently, it might be necessary to reduce R_4, so that R_4 and R_{F2} add up to the original resistance selected for R_4 (or R_E), (see Fig. 13-14).

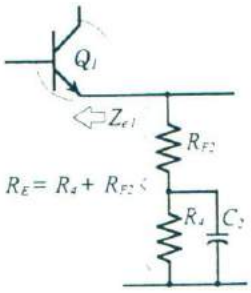


Figure 13-14
Resistor R_{F2} is in parallel with the impedance Z_{e1} 'looking into' the emitter of Q_1. The total (dc) emitter resistance (R_E) is also increased by the presence of R_{F2}.

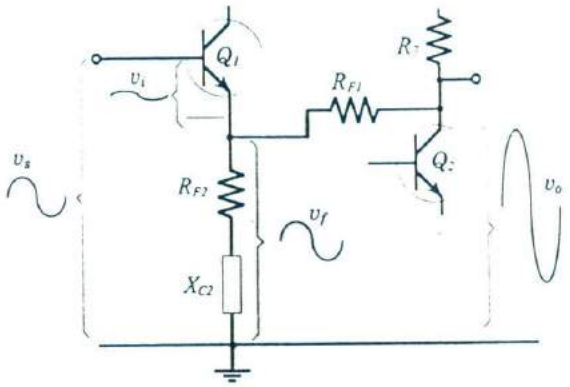


Figure 13-15
Low-frequency ac equivalent circuit for the feedback network in the circuit of Fig. 13-12. Note that X_{C2} is in series with R_{F2}.

Figure 13-15 shows a low-frequency *ac* equivalent circuit for the feedback network. Note that capacitor C_{F1} is still taken as an *ac* short circuit, so X_{CF1} is assumed to be very much smaller than R_{F1}. The impedance of capacitor C_2 is show, and because X_{C2} is assumed to be very much smaller than resistor R_4, R_4 is omitted.

From Fig. 13-15, v_o is divided across R_{F1} and $(R_{F2} + jX_{C2})$ to give v_f, so the feedback factor is,

$$B = \frac{R_{F2} - jX_{C2}}{(R_{F2} - jX_{C2}) + R_{F1}}$$

Assuming that $(R_{F2} - jX_{C2}) << R_{F1}$,

$$B \approx \frac{R_{F2} - jX_{C2}}{R_{F1}}$$

From Eq. 13-3,

$$A_{CL} \approx \frac{R_{F1}}{R_{F2} - jX_{C2}}$$

or,

$$|A_{CL}| \approx \frac{R_{F1}}{\sqrt{(R_{F2}^2 + X_{C2}^2)}}$$

When $X_{C2} = R_{F2}$,

$$|A_{CL}| \approx \frac{R_{F1}}{\sqrt{2}\, R_{F2}} \approx 0.707 \times \text{(mid-frequency gain)}$$

To set a desired frequency lower cutoff frequency (f_1),

$$\boldsymbol{X_{C2} = R_{F2} \text{ at } f_1} \qquad \textbf{(13-11)}$$

As already mentioned, X_{CF1} must be very much smaller than R_{F1} at the low cutoff frequency for the amplifier. It can be shown that, if $X_{CF1} = R_{F1}$ at f_1, the closed-loop gain would actually increase at frequencies below f_1. C_{F1} is normally calculated from,

$$\boldsymbol{X_{CF1} = \frac{R_{F1}}{100} \text{ at } f_1} \qquad \textbf{(13-12)}$$

Capacitor C_{F1} can often be eliminated. If R_{F1} is large enough, direct connection of R_{F1} from Q_{2C} to Q_{1E} in Fig. 13-12 will have a negligible effect on the circuit bias conditions. In fact, with a direct-coupled circuit, direct connection of the feedback resistors might enhance the circuit bias stability.

The circuit input impedance is increased by negative feedback, so input coupling capacitor C_1 can be recalculated as a smaller capacitor, ($X_{C1} = Z_{i1}/10$ at f_1). Recall that the bias resistors are not affected by feedback. Regardless of how high the circuit input impedance might become, C_1 should normally be selected as a minimum of 0.1 μF, to ensure that it is much larger than any stray capacitance at the circuit input.

The emitter bypass capacitor C_4 (in Fig. 13-12) was calculated (in Ex. 12-6) to have $X_{C4} = 0.65\, h_{ib2}$ at f_1. So, X_{C4} will reduce the circuit open-loop gain (A_v) at f_1. However, even with this gain reduction, A_v should still be much larger than A_{CL}, so C_4 can normally be left as calculated for an amplifier without feedback.

Example 13-5

Modify the two-stage capacitor-coupled *BJT* amplifier designed in Example 12-6 to use series voltage feedback, as in Fig. 13-16. The closed-loop gain is to be 75, and the lower cutoff frequency is to be 100 Hz.

Solution

Select $R_{f2} = 220\ \Omega$ $(R_{f2} < Z_i)$

R_4 becomes, R_4 = (original R_4) - R_{F2} = 3.9 kΩ - 220 Ω
= 3.68 kΩ (use 3.9 kΩ standard value)

From Eq. 13-9, $R_{f1} = (A_{CL} - 1)\, R_{F2} = (75 - 1) \times 220\ \Omega$
= 16.3 kΩ (use 15 kΩ + 1.2 kΩ)

Eq. 13-11, $X_{C2} = R_{f2}$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_{F2}}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times 220\ \Omega}$$

$$= 7.2\ \mu\text{F} \quad (\text{use } 8\ \mu\text{F})$$

Eq. 13-12, $X_{CF1} = \frac{R_{f1}}{100}$ at f_1

$$C_{F1} = \frac{1}{2\pi f_1 R_{f1}/100}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times 16.2\ \text{k}\Omega\ 100}$$

$$= 9.8\ \mu\text{F} \quad (\text{use } 10\ \mu\text{F})$$

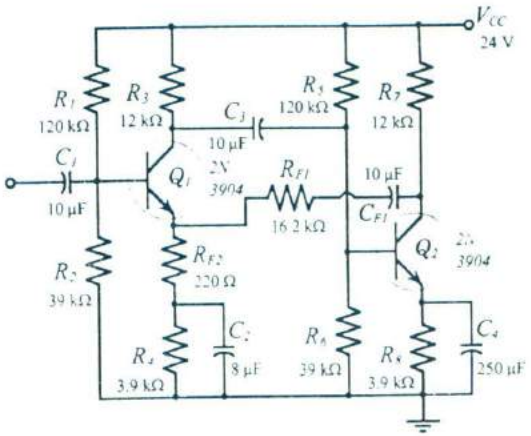


Figure 13-16
Negative feedback amplifier for Example 13-5. Note that this is the circuit analyzed in Ex. 13-4.

Recall from Chapter 12 that, when designing an amplifier without feedback, the collector resistor (R_{C2}) for the output transistor is usually selected as equal to, or less than, $R_L/10$. This is because without negative feedback $Z_o \approx R_{C2}$. Negative feedback normally reduces Z_o to a value much smaller than R_{C2} (see Ex. 13-4). So, R_{C2} (R_7 in Fig. 13-16) does not have to be selected as $R_L/10$ when designing a negative feedback amplifier. Instead, any convenient level of V_{RC} and I_C can be used for calculating a suitable R_{C2} value.

Practise Problems

13-2.1 Modify the circuit in Fig. 12-18 to use series voltage negative feedback (as in Fig. 13-16) to give $A_{CL} = 100$, and $f_1 = 50$ Hz.

13-2.2 Analyze the negative feedback circuit in Problem 13-2.1 to determine the input and output impedances. The transistor parameters are $h_{ie} = 1$ kΩ, $h_{oe} = 40\ \mu$S, and $h_{fe} = 100$.

13-3 More Amplifiers with Series Voltage Negative Feedback

Complementary Direct-Coupled Circuit with Feedback

The two-stage, direct-coupled *BJT* amplifier in Fig. 13-17 is reproduced from Fig. 12-22, and modified to include feedback components R_{F1} and R_{F2}. The feedback network design procedure is exactly as discussed in Section 13-2. Other direct-coupled circuits can be converted into negative feedback amplifiers by following the same procedure. Similarly, *BIFET* circuits, both direct-coupled and capacitor-coupled, can be designed for overall negative feedback. As always, the best approach is to first design the circuit as a non-feedback amplifier, then determine the feedback component values.

Note that there is no coupling-capacitor for the feedback network in the circuit shown in 13-17. This is because (as discussed in Section 13-2) the omission of the capacitor can have a negligible effect on the circuit *dc* conditions if feedback resistor R_{F1} is large enough.

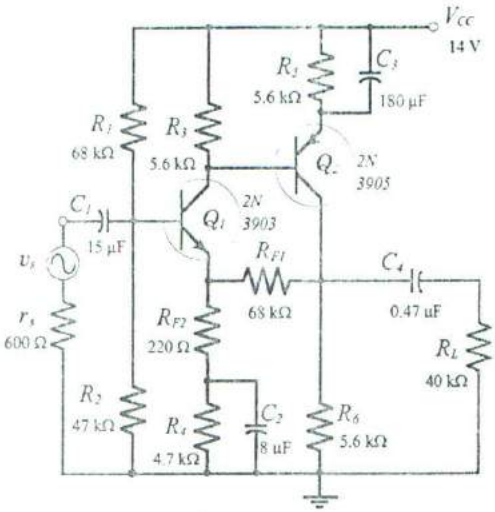


Figure 13-17
Complementary, direct-coupled amplifier using series-voltage negative feedback. The amplifier closed-loop voltage gain is, $A_{CL} = (R_{F1} + R_{F2})/R_{F2}$.

Example 13-6

Modify the direct-coupled amplifier in Fig. 12-22 to use series-voltage negative feedback as in Fig 13-17. The amplifier closed-loop voltage gain is to be approximately 300, and the lower cutoff frequency is to be 75 Hz.

Solution

$$R_{F2} < Z_{e1}$$

Select $R_{F2} = 220\ \Omega$

R_4 becomes, $R_4 = (\text{original } R_4) - R_{F2} = 4.7\ \text{k}\Omega - 220\ \Omega$

$= 4.48\ \text{k}\Omega$ (use 4.7 kΩ standard value)

From Eq. 13-9, $R_{F1} = (A_{CL} - 1)\, R_{F2} = (300 - 1) \times 220\ \Omega$
$\approx 66\ k\Omega$ (use 68 kΩ standard value)

Eq. 13-11, $X_{C2} = R_{F2}$ at f_1

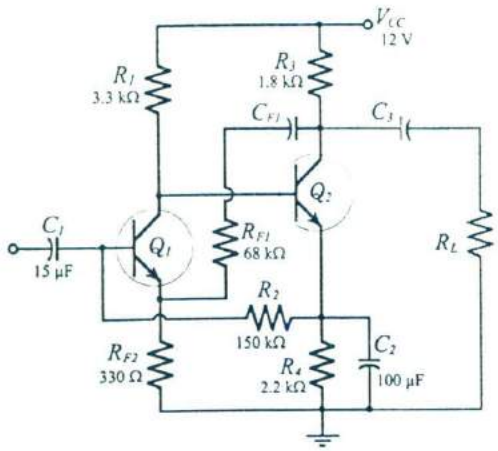
$$C_2 = \frac{1}{2\pi f_1 R_{F2}} = \frac{1}{2\pi \times 100\ Hz \times 220\ \Omega}$$

$= 7.2\ \mu F$ (use 8 μF standard value)

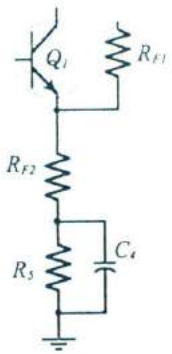
Analysis of the circuit in Ex. 13-6 reveals that the transistor *dc* collector currents are approximately 1 mA, and that the direct current through R_{F1} is around 4.4 μA.

DC Feedback Pair Using Negative Feedback

Figure 13-18(a) shows a *dc* feedback pair with *ac* feedback components C_{F1}, R_{F1}, and R_{F2}. This is the most economical of all two-stage *BJT* amplifier circuits, because it has the smallest quantity of components. It can have just as high a voltage gain (open-loop and closed-loop) as any other two-stage circuit. As a negative feedback amplifier, its input resistance is normally higher than that for a *BJT* circuit using voltage divider bias, (R_2 is usually larger than the parallel resistance of voltage divider resistors). As always, the feedback components are determined after the circuit is designed for the largest possible open-loop voltage gain.



(a) DC feedback pair using series-voltage negative feedback



(b) Circuit modification for predictable low 3 dB frequency

Figure 13-18
DC feedback pair as a negative feedback amplifier. The closed-loop voltage gain is,
$A_{CL} = (R_{F1} + R_{F2})/R_{F2}$.

The lower cutoff frequency for the circuit in Fig. 13-18(a) is unpredictable. The modification shown in Fig. 13-18(b) gives a definite low 3 dB frequency, (when $X_{C4} = R_{F2}$). In this case, emitter

resistor R_5 affects the circuit *dc* bias conditions, so it must be designed into the circuit from the start. As in other circuits, it might be possible to omit the feedback network coupling capacitor, (C_{F1} in Fig. 13-18). The direct current through R_{F1} should be calculated to ensure that it does not significantly affect the bias conditions of the circuit.

BIFET Two-Stage Circuit With Negative Feedback

A two-stage, direct-coupled, *BIFET* circuit with series-voltage negative feedback is shown in Fig. 13-19. This is a modified version of the circuit in Fig. 12-30, designed in Examples 12-15 and 12-16.

The open-loop voltage gain of a *BIFET* circuit is typically 50 to 100 times smaller than that for a two-stage *BJT* amplifier, (see Ex. 12-17). Therefore, *BIFET* negative feedback amplifiers must be designed for relative small closed-loop voltage gains, usually a maximum of around 30. The single major advantage of *BIFET* circuits, very high input impedance, is largely unchanged by negative feedback. The design procedure for the feedback network in the *BIFET* circuit is exactly as already discussed.

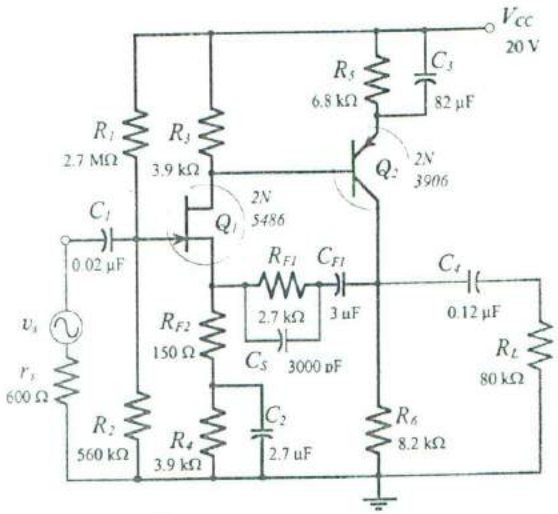


Figure 13-19
BIFET circuit using series-voltage negative feedback. The closed-loop voltage gain is,
$A_{CL} = (R_{F1} + R_{F2})/R_{F2}$

Setting the Circuit Upper Cutoff Frequency

The upper cutoff frequency of any of the series voltage negative feedback amplifiers already discussed can be set by the simple process of connecting a capacitor (C_S) across feedback resistor R_{F1}, as illustrated in Fig. 13-19. It can be shown that f_2 occurs when $X_{CS} = R_{F1}$, so long as the upper cutoff frequency without C_S is much higher than the desired f_2 value. Therefore, to determine C_S,

$$X_{CS} = R_{F1} \text{ at } f_2 \qquad (13\text{-}13)$$

Practise Problems

13-3.1 Determine suitable feedback network component values for the *dc* feedback pair in Fig. 13-18(a) to give $A_{CL} = 200$. Use a short-circuit in place of C_{F1}, and calculate the direct current through R_{F1}.

13-3.2 Design the feedback network for the *BIFET* circuit in Fig. 13-19 to give $A_{CL} = 20$, $f_1 = 200$ Hz, and $f_2 = 20$ kHz.

13-4 Two-Stage Differential Amplifier with Negative Feedback

Two-Stage Differential Amplifier

The circuit shown in Fig. 13-20 has a differential-amplifier input stage with *npn BJTs*, and a direct-coupled *pnp* transistor differential amplifier second stage. (The differential amplifier is discussed in detail in Section 12-8.) The circuit uses a plus/minus supply voltage, and the base terminals of Q_1 and Q_2 are biased to ground via resistors R_1 and R_6, respectively. Transistors Q_3 and Q_4 have the bases directly connected to the collector terminals of Q_1 and Q_2. So, bias voltage for Q_3 and Q_4 bases is provided by the voltage drops across the Q_1 and Q_2 collector resistors, (R_2 and R_4).

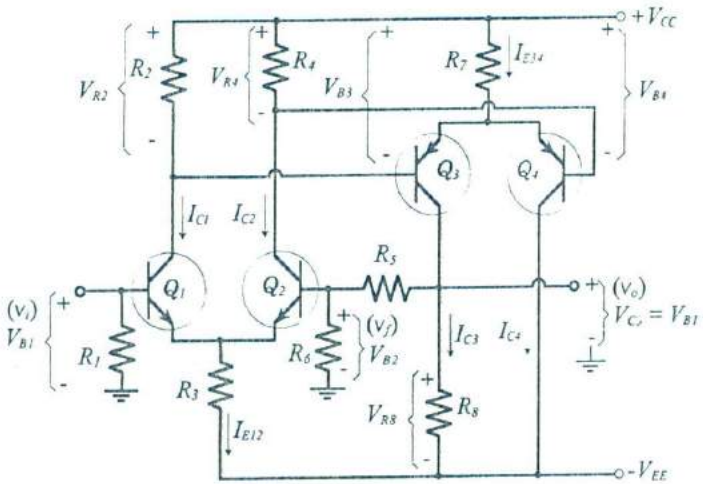


Figure 13-20
Two-stage direct-coupled differential amplifier with series-voltage negative feedback.

The amplifier input terminal is the base of Q_1, and the output is taken from Q_3 collector. No collector resistor is provided for Q_4, because no output or feedback is taken from Q_4. Note that the feedback network (R_5 and R_6) is connected from the output at the collector of Q_3 back to the base of Q_2. Because the emitter of Q_2 is directly coupled to Q_1 emitter, applying the feedback voltage (v_f) to Q_2 base is similar to applying it to Q_1 emitter.

DC Bias Conditions

The circuit in Fig. 13-20 is designed to have the *dc* bias voltage at Q_2 base equal to Q_1 base bias voltage; in this case, ground level. This means that the *dc* voltage at the collector of Q_3 must also equal the Q_1 base voltage, because Q_3 collector is directly connected to Q_2 base via R_5. Consider what would happen if V_{C3} (at the output terminal) is not exactly equal to V_{B1} (at the input).

Suppose V_{C3} goes lower than its normal level:

- V_{B2} is reduced below the level of V_{B1}, and this reduces I_{C2} and increases I_{C1}.
- The increased level of I_{C1} causes an increased voltage drop across R_2, and the reduced level of I_{C2} decreases the voltage drop across R_4. Thus V_{B3} is increased and V_{B4} is decreased.
- This raises the level of I_{C3} and lowers I_{C4}. So, V_{R8} is increased (by the I_{C3} increase) to drive V_{C3} back up to its normal voltage.

Similarly, if V_{C3} somehow drifts to a higher than normal level:

- V_{B2} is raised above the level of V_{B1}, thus increasing I_{C2} and reducing I_{C1}.
- The decreased level of I_{C1} and increased level of I_{C2} produces voltage drops across R_2 and R_4 that reduce V_{B3} and increase V_{B4}.
- This change reduces I_{C3}, thus decreasing V_{R8} to drive V_{C3} back down to its normal voltage.

It is seen that there is *dc negative feedback* that stabilizes the circuit bias conditions.

AC Operation

Consider the circuit waveforms shown in Fig. 13-21. A positive-going input signal (v_i) at the base of Q_1 produces a positive-going output (v_o) at Q_3 collector. As in the case of the *dc* bias conditions, the instantaneous *ac* voltage at Q_2 base follows the instantaneous level of the *ac* signal voltage at Q_1 base.

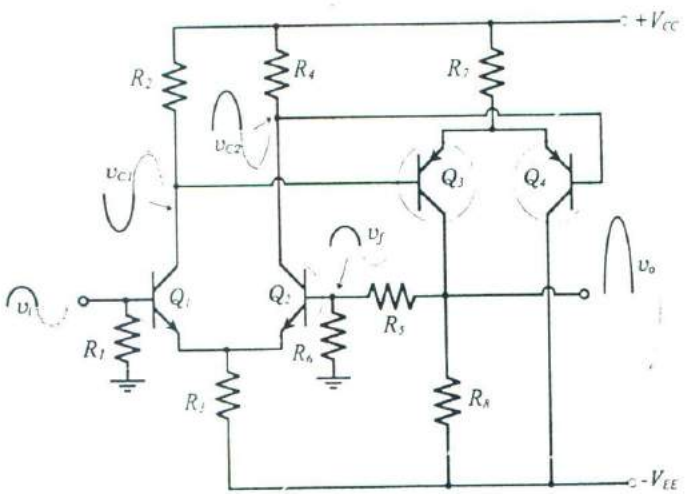


Figure 13-21
AC waveforms in a two-stage differential amplifier with series voltage negative feedback.

With $v_{b2} = v_{b1}$, or $v_i = v_f$,

$$v_f = B v_o = v_o \times \frac{R_6}{R_5 + R_6}$$

so,
$$v_o = v_f \times \frac{R_5 + R_6}{R_6} = v_i \times \frac{R_5 + R_6}{R_6}$$

giving,
$$A_{CL} = \frac{R_5 + R_6}{R_6}$$

Resistors R_5 and R_6 in Figs. 13-20 and 13-21 are comparable to R_{F1} and R_{F2}, respectively, in the other negative feedback circuits already discussed. So, the closed-loop gain equation is the same equation that applies in the case of all series-voltage negative feedback amplifiers. As always, the equation is true only when the open-loop gain is very much larger than the closed-loop gain.

The input and output impedances for a circuit with a differential input stage are calculated exactly as discussed for other negative feedback circuits.

Note that there are no bypass capacitors in the circuit in Figs. 13-20 and 13-21. If the signal and load are capacitor coupled to the circuit, the coupling capacitors determine the lower cutoff frequency. If the signal and load are direct coupled, then the circuit is a *dc amplifier;* one that amplifies direct voltage signals.

Circuit Design

The design procedure for the input stage is similar to that discussed in Section 12-8. The second stage components are determined in essentially the same way as the input stage components, bearing in mind that the second stage is *upside down* compared to the input stage. Feedback network resistor R_6 at the base of Q_2 is selected equal to bias resistor R_1 at Q_1 base. This is to equalize the resistances at the bases of Q_1 and Q_2, and thus equalize any voltage drops due to I_{B1} and I_{B2}. R_5 is calculated from the specified closed loop gain and the R_6 resistance.

Example 13-7

The two-stage differential amplifier in Fig. 13-22 is to use a ±10 V supply, and have a closed-loop gain of 33. Select suitable direct current and voltage levels, and calculate resistor values for the circuit. Assume that the transistors have $h_{fe} = 100$.

Solution

Select, $I_{C1} = I_{C2} = I_{C3} = I_{C4} \approx 1$ mA

From Eq. 5-17,
$$R_1 \approx \frac{V_{BE}}{10\, I_{C1}/h_{fe}} \approx \frac{0.7\text{ V}}{10 \times 1\text{ mA}/100}$$

$= 7$ kΩ (use 6.8 kΩ standard value)

$$R_3 \approx \frac{V_{EE} - V_{BE}}{I_{C1} + I_{C2}} = \frac{10\text{ V} - 0.7\text{ V}}{2\text{ mA}}$$

$$= 4.65\text{ k}\Omega \text{ (use 4.7 k}\Omega\text{ standard value)}$$

Select, $V_{CE1} \approx 3\text{ V}$

$$V_{R2} = V_{CC} + V_{BE1} - V_{CE1} = 10\text{ V} + 0.7\text{ V} - 3\text{ V}$$

$$= 7.7\text{ V}$$

$$R_2 = R_4 = \frac{V_{R2}}{I_{C1}} = \frac{7.7\text{ V}}{1\text{ mA}}$$

$$= 7.7\text{ k}\Omega \quad \text{(use 6.8 k}\Omega\text{ standard value)}$$

$$R_7 = \frac{V_{R2} - V_{BE}}{I_{C3} + I_{C4}} = \frac{7.7\text{ V} - 0.7\text{ V}}{2\text{ mA}}$$

$$= 3.5\text{ k}\Omega \quad \text{(use 3.3 k}\Omega\text{ standard value)}$$

$$R_8 = \frac{V_{EE}}{I_{C3}} = \frac{10\text{ V}}{1\text{ mA}}$$

$$= 10\text{ k}\Omega \quad \text{(standard value)}$$

Select, $R_6 = R_1 = 6.8\text{ k}\Omega$

From Eq. 13-9, $R_5 = (A_{CL} - 1)\,R_6 = (33 - 1) \times 6.8\text{ k}\Omega$

$$= 217.6\text{ k}\Omega \text{ (use 220 k}\Omega\text{ standard value)}$$

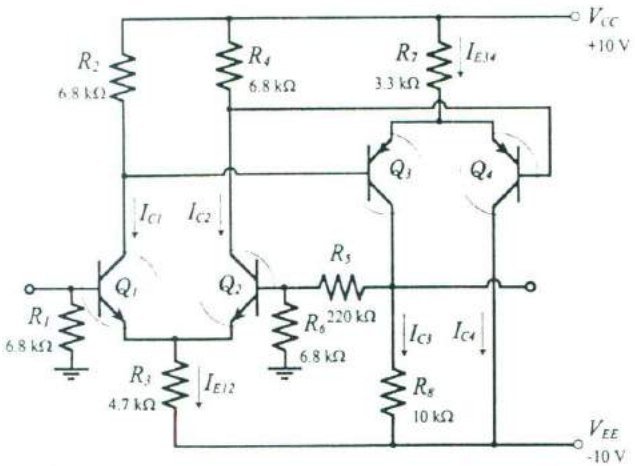


Figure 13-22
Amplifier circuit for Ex. 13-7.

Example 13-8

Assuming an open-loop gain of 25 000, $h_{ie} = 2\text{ k}\Omega$, $h_{ib} = 25\ \Omega$, and $1/h_{oe} = 100\text{ k}\Omega$, for the circuit in Ex. 13-7, calculate A_{CL}, Z_{in}, and Z_{out}.

Solution

From Eq. 13-8, $$B = \frac{R_6}{R_5 + R_6} = \frac{6.8\ \text{k}\Omega}{220\ \text{k}\Omega + 6.8\ \text{k}\Omega}$$
$$= \frac{1}{33.4}$$

Eq. 13-2, $$A_{CL} = \frac{A_v}{1 + A_v B} = \frac{25\,000}{1 + (25\,000/33.4)}$$
$$= 33.4$$

Eq. 13-4, $$Z_i = 2\,h_{ie}(1 + A_v B) = 2\ \text{k}\Omega[1 + (25\,000/33.4)]$$
$$= 3\ \text{M}\Omega$$

Eq. 13-5, $$Z_{in} = Z_i \| R_1 = 3\ \text{M}\Omega \| 6.8\ \text{k}\Omega$$
$$\approx 6.8\ \text{k}\Omega$$

Eq. 13-6, $$Z_o = \frac{1/h_{oe}}{1 + A_v B} = \frac{100\ \text{k}\Omega}{1 + (25\,000/33.4)}$$
$$= 133\ \Omega$$

Eq. 13-7, $$Z_{out} = R_8 \| Z_o = 10\ \text{k}\Omega \| 133\ \Omega$$
$$= 131\ \Omega$$

Modification for Reduced Z_{out}

Although the application of series-voltage negative feedback substantially reduces the output impedance of a circuit, further reduction of Z_{out} is sometimes required. Figure 13-23 shows the circuit of Fig. 13-22 with the addition of an emitter follower output stage (Q_5). Note that the feedback network is now connected at the emitter follower output terminal.

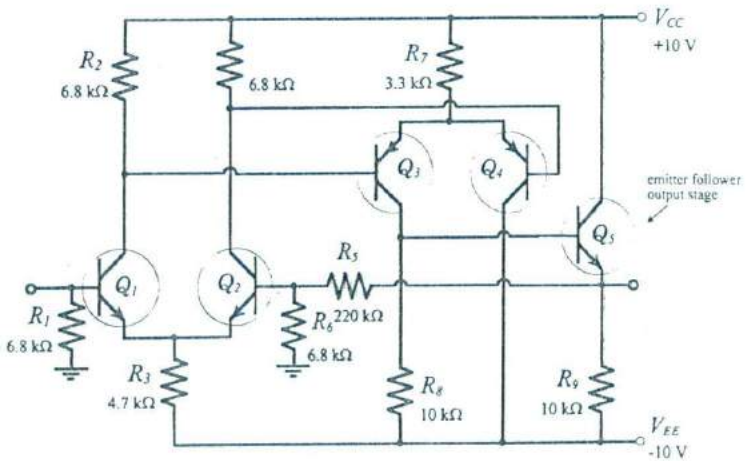


Figure 13-23
Use of an emitter follower output stage to provide very low output impedance.

The output impedance at Q_5 emitter terminal in Fig. 13-23 is found from the derivation of Eq. 6-24 (for a common-collector circuit).

$$Z_e = \frac{h_{ic} + (Z \text{ in series with } Q_5 \text{ base})}{h_{fc}}$$

This gives,

$$\mathbf{Z_e = \frac{h_{ic} + R_8}{h_{fc}}} \qquad \textbf{(13-14)}$$

This quantity is modified by negative feedback according to (a rewritten) Eq. 13-6.

$$Z_o = \frac{Z_e}{1 + A_v B}$$

Then, as always, the circuit output impedance is given by Eq. 13-7, which must also be rewritten for the circuit in Fig. 13-23.

$$Z_{out} = Z_o \| R_9$$

An emitter follower output stage can be added to any of the amplifiers previously discussed. However, the combination of an emitter follower output stage with a differential amplifier has a particular significance that will be explained in Chapter 14.

Example 13-9

Calculate the output impedance for the circuit modification in Fig. 13-23, assuming that $h_{ic} = h_{ie} = 2\ \text{k}\Omega$, and $h_{fc} = h_{fe} = 100$. Also assume that $A_v = 25\,000$ and $B = 1/33.4$, as for Ex. 13-7 and 13-8.

Solution

Eq. 13-14,
$$Z_e = \frac{h_{ic} + R_4}{h_{fc}} = \frac{2\ \text{k}\Omega + 10\ \text{k}\Omega}{100}$$
$$= 120\ \Omega$$

Eq. 13-6,
$$Z_o = \frac{Z_e}{1 + A_v B} = \frac{120\ \Omega}{1 + (25\,000/33.4)}$$
$$= 0.16\ \Omega$$

Eq. 13-7,
$$Z_{out} = R_5 \| Z_o = 10\ \text{k}\Omega \| 0.16\ \Omega$$
$$= 0.16\ \Omega$$

Practise Problems

13-4.1 A two-stage differential amplifier with negative feedback, as in Fig. 13-22, is to use *2N3904* and *2N3906 BJTs* with a ±15 V supply. The closed-loop gain is to be 50. Determine suitable resistor values.

13-4.2 Calculate the minimum open loop gain for the circuit in Problem 13-4.1. Also, determine Z_{in} and Z_{out}.

13-5 Emitter Current Feedback

Emitter Current Feedback Circuit

Emitter current feedback is produced by connecting an unbypassed resistor in series with the emitter terminal of a transistor, as shown in Fig. 13-24(a). The effects of an unbypassed emitter resistor in a *CE* circuit have been analyzed in Section 6-5, where it is shown that the circuit impedances and voltage gains are;

Eq. 6-20, $Z_b = h_{ie} + R_{E1}(1 + h_{fe})$

Eq. 6-12, $Z_{in} = R_1 \| R_2 \| Z_b$

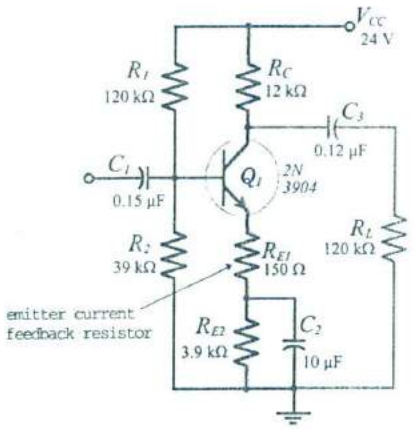
Eq. 6-14, $Z_{out} = (1/h_{oe}) \| R_C \approx R_C$

Eq. 6-21, $$A_v = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + R_{E1}(1 + h_{fe})}$$

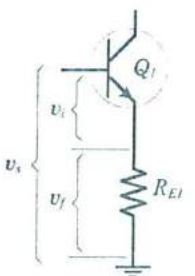
Eq. 6-22, $$A_v \approx \frac{R_C \| R_L}{R_{E1}}$$

Equation 6-20 shows that the input impedance at the base of a transistor with an unbypassed emitter resistor is considerably increased above its normal value without feedback (h_{ie}). This raises the circuit input impedance, as defined by Eq. 6-12. Therefore,

emitter current feedback increases the circuit input impedance.



(a) Emitter current feedback circuit



(b) Signal, input, and feedback voltages

Figure 13-24
Single-stage CE amplifier using emitter current feedback. The voltage gain is $A_v \approx (R_C \| R_L)/R_{E1}$.

Figure 13-24(b) shows that the circuit feedback loop is from the transistor base to the emitter, then back to the base again. The collector resistor is outside the feedback loop. The circuit output impedance remains approximately equal to R_C, (see Eq. 6-14). So,

emitter current feedback has no effect on the circuit output impedance, (see Section 6-5).

The precise voltage gain for the circuit in Fig. 13-24(a) is given by Eq. 6-21, and Eq. 6-22 can be used for calculation of the approximate voltage gain. Equation 6-22 is derived from Eq. 6-21 by assuming that $h_{ie} << R_{E1}(1 + h_{fe})$. Using typical values of R_{E1} = 100 Ω, h_{fe} = 100,

$$R_{E1}(1 + h_{fe}) \approx 10\ \text{k}\Omega$$

This is ten times the typical value for h_{ie}. So, Eq. 6-22 gives a reasonably close approximation to the circuit voltage gain.

It is apparent that,

emitter current feedback stabilizes single-stage amplifier voltage gain.

Example 13-10

The emitter current feedback circuit in Fig. 13-24 uses a transistor with $h_{fe\,min}$ = 100, $h_{fe(max)}$ = 400, $h_{ie(min)}$ = 1 kΩ, and $h_{ie(max)}$ = 5 kΩ. Calculate the precise value of the circuit voltage gain at the h_{fe} extremes, then calculate the approximate voltage gain using Eq. 6-22.

Solution

Eq. 6-21, $$A_v = \frac{h_{fe}(R_C \| R_L)}{h_{ie} + R_{E1}(1 + h_{fe})}$$

$$A_{v(max)} = \frac{h_{fe(max)}(R_C \| R_L)}{h_{ie(max)} + R_{E1}(1 + h_{fe(max)})} = \frac{400(12\ \text{k}\Omega \| 120\ \text{k}\Omega)}{5\ \text{k}\Omega + 150\ \Omega(1 + 400)}$$

$$= 67$$

$$A_{v(min)} = \frac{h_{fe(min)}(R_C \| R_L)}{h_{ie(min)} + R_{E1}(1 + h_{fe(min)})} = \frac{100(12\ \text{k}\Omega \| 120\ \text{k}\Omega)}{1\ \text{k}\Omega + 150\ \Omega(1 + 100)}$$

$$= 67.5$$

Eq. 6-22, $$A_v \approx \frac{R_C \| R_L}{R_{E1}} = \frac{12\ \text{k}\Omega \| 120\ \text{k}\Omega}{150\ \Omega}$$

$$= 72.7$$

Circuit Design

As in the case of other negative feedback amplifiers, an emitter current feedback circuit should first have its resistor values calculated as for a circuit without feedback. Resistor R_{E1} is then determined from Eq. 6-22, and R_{E2} is reduced to its original value minus R_{E1}, if R_{E1} is large enough to affect the circuit bias conditions. The input and output coupling capacitors are calculated in the usual way, remembering that Z_{in} is increased by

the presence of R_{E1}. The equation for the emitter bypass capacitor (Eq. 12-3) is rewritten to take R_{E1} into account. Equation 12-3 was derived from the fact that X_{C2} must equal the impedance in series with C_2 at the lower cutoff frequency for the circuit. For the circuit in Fig. 13-24(a),

$$X_{C2} = (h_{ib} + R_{E1}) \text{ at } f_1$$

usually, $R_{E1} >> h_{ib}$, so the capacitor can be calculated from,

$$\boldsymbol{X_{C2} = R_{E1} \text{ at } f_1} \qquad \textbf{(13-15)}$$

Example 13-11

Modify the *CE* amplifier circuit designed in Examples 12-2 and 12-3 to use emitter current feedback to give $A_v = 70$. The lower cutoff frequency is $f_1 = 100$ Hz, and the signal source resistance is $r_s = 600\ \Omega$.

Solution

From Eq. 6-22, $$R_{E1} \approx \frac{R_C \| R_L}{A_v} = \frac{12\ \text{k}\Omega \| 120\ \text{k}\Omega}{70}$$

$$\approx 156\ \Omega \text{ (use 150 } \Omega \text{ standard value)}$$

$$R_{E2} = R_E - R_{E1} = 3.9\ \text{k}\Omega - 150\ \Omega$$
$$= 3.75\ \text{k}\Omega \text{ (use 3.9 k}\Omega\text{)}$$

Eq. 6-20, $$Z_{b(min)} = h_{ie} + R_{E1}(1 + h_{fe}) = 1\ \text{k}\Omega + 150\ \Omega(1 + 100)$$
$$= 16.2\ \text{k}\Omega$$

Eq. 6-12, $$Z_{in} = R_1 \| R_2 \| Z_b = 120\ \text{k}\Omega \| 39\ \text{k}\Omega \| 16.2\ \text{k}\Omega$$
$$= 10.4\ \text{k}\Omega$$

Eq. 12-4, $$C_1 = \frac{1}{2\pi f_1 (Z_{in} + r_s)/10}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times (10.4\ \text{k}\Omega + 600\ \Omega)/10}$$

$$= 1.5\ \mu\text{F} \text{ (standard value)}$$

Eq. 13-15, $$X_{C2} = R_{E1} \text{ at } f_1$$

$$C_2 = \frac{1}{2\pi f_1 R_{E1}} = \frac{1}{2\pi \times 100\ \text{Hz} \times 150\ \Omega}$$
$$= 10.6\ \mu\text{F} \text{ (use 10 } \mu\text{F standard value)}$$

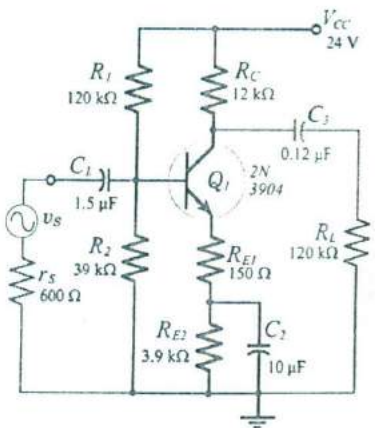


Figure 13-25
Emitter current feedback circuit for Ex. 13-11.

Two-Stage Circuit with Emitter Current Feedback

All of the two-stage amplifiers discussed in Ch. 12 can be designed to use emitter current feedback for voltage gain stabilization and increased input impedance. The design procedures are essentially those already discussed.

Consider the two-stage, capacitor-coupled circuit in Fig. 13-26. The voltage gain for *stage-1* is,

From Eq. 6-22, $$A_{v1} \approx \frac{R_3 \| Z_{in2}}{R_4} \qquad \textbf{(13-16)}$$

and for stage-2, $$A_{v2} \approx \frac{R_8 \| R_L}{R_9} \qquad \textbf{(13-17)}$$

The overall voltage gain is,

$$A_v = A_{v1} \times A_{v2}$$

When designing a two-stage circuit with emitter current feedback, the gain of each stage is determined as,

$$\mathbf{A_{v1} = A_{v2} = \sqrt{A_v}} \qquad \textbf{(13-18)}$$

Although the two stages can be designed for identical gains, $R_3 \| Z_{i2}$ is unlikely to equal $R_8 \| R_L$. So, R_4 and R_9 are likely to be unequal.

For the reasons discussed in Section 12-3, the emitter bypass capacitors are determined from,

$$\mathbf{X_{C2} = 0.65\ R_4 \text{ at } f_1} \qquad \textbf{(13-19)}$$

and $$\mathbf{X_{C4} = 0.65\ R_9 \text{ at } f_1} \qquad \textbf{(13-20)}$$

The circuit input impedance is, once again, given by Eqs. 6-20 and 6-12, and the output impedance is simply the collector resistor in the second stage, (see Eq. 6-14).

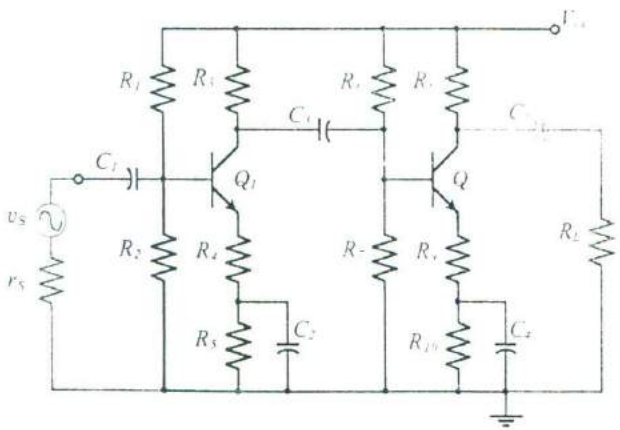


Figure 13-26
Two-stage, capacitor-coupled, BJT amplifier using emitter current feedback in each stage.

Example 13-12

The circuit in Fig. 13-25 is to be modified for use as each stage of the circuit in Fig. 13-26. The overall voltage gain is to be 1000, and the lower cutoff frequency is to be 100 Hz. Determine suitable emitter resistor values. Assume transistor parameters of $h_{ie} = 1\ \text{k}\Omega$ and $h_{fe} = 100$.

Solution

Eq. 13-18, $A_{v1} = A_{v2} = \sqrt{A_v} = \sqrt{1000}$
$= 31.6$

From Eq. 13-17, $R_9 \approx \dfrac{R_8 \| R_L}{A_{v2}} = \dfrac{12\ \text{k}\Omega \| 120\ \text{k}\Omega}{31.6}$
$\approx 345\ \Omega$ (use 330 Ω standard value)

$R_{10} = R_E - R_9 = 3.9\ \text{k}\Omega - 330\ \Omega$
$= 3.57\ \text{k}\Omega$ (use 3.9 kΩ)

A_{v2} becomes, $A_{v2} \approx \dfrac{R_8 \| R_L}{R_9} = \dfrac{12\ \text{k}\Omega \| 120\ \text{k}\Omega}{330\ \Omega}$
≈ 33

so, $A_{v1} \approx \dfrac{A_v}{A_{v2}} = \dfrac{1000}{33}$
$= 30.3$

From Eq. 6-20, $Z_{i2} = h_{ie} + R_9(1 + h_{fe})$
$= 1\ \text{k}\Omega + 330\ \Omega(1 + 100)$
$= 34.3\ \text{k}\Omega$

From Eq. 6-12, $Z_{in2} = R_6 \| R_7 \| Z_{i2} = 120\ \text{k}\Omega \| 39\ \text{k}\Omega \| 34.3\ \text{k}\Omega$
$= 15.8\ \text{k}\Omega$

From Eq. 13-16, $R_4 \approx \dfrac{R_3 \| Z_{in2}}{A_{v1}} = \dfrac{12\ \text{k}\Omega \| 15.8\ \text{k}\Omega}{30.3}$
$\approx 225\ \Omega$ (use 220 Ω standard value)

$R_5 = R_E - R_4 = 3.9\ \text{k}\Omega - 220\ \Omega$
$= 3.68\ \text{k}\Omega$ (use 3.9 kΩ)

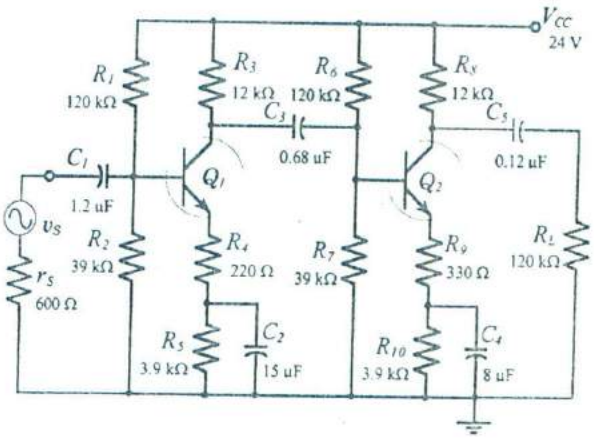


Figure 13-27
Emitter current feedback amplifier circuit for Ex. 13-12 and 13-13.

Example 13-13

Calculate suitable capacitor values for the two-stage circuit in Ex. 13-12.

Solution

Eq. 6-20, $Z_{i1} = h_{ie} + R_4(1 + h_{fe}) = 1\ \text{k}\Omega + 220\ \Omega(1 + 100)$
$= 23.2\ \text{k}\Omega$

Eq. 6-12, $Z_{in1} = R_1 \| R_2 \| Z_{i1} = 120\ \text{k}\Omega \| 39\ \text{k}\Omega \| 23.2\ \text{k}\Omega$
$= 13\ \text{k}\Omega$

Eq. 12-4, $C_1 = \dfrac{1}{2\pi f_1 (Z_{in1} + r_s)/10} = \dfrac{1}{2\pi \times 100\ \text{Hz} \times (13\ \text{k}\Omega + 600\ \Omega)/10}$
$= 1.2\ \mu\text{F}$ (standard value)

Eq. 13-19, $X_{C2} = 0.65\,R_4$ at f_1

$$C_2 = \frac{1}{2\pi f_1 0.65\,R_4} = \frac{1}{2\pi \times 100\text{ Hz} \times 0.65 \times 220\ \Omega}$$

$$= 11.1\ \mu\text{F} \text{ (use 15 } \mu\text{F standard value)}$$

Eq. 12-4, $$C_3 = \frac{1}{2\pi f_1 (Z_{in2} + R_3)/10} = \frac{1}{2\pi \times 100\text{ Hz} \times (15.8\ \text{k}\Omega + 12\ \text{k}\Omega)/10}$$

$$= 0.57\ \mu\text{F} \text{ (use 0.68 } \mu\text{F standard value)}$$

Eq. 13-20, $X_{C4} = 0.65\,R_9$ at f_1

$$C_4 = \frac{1}{2\pi f_1 0.65\,R_L} = \frac{1}{2\pi \times 100\text{ Hz} \times 0.65 \times 330\ \Omega}$$

$$= 7.4\ \mu\text{F} \text{ (use 8 } \mu\text{F standard value)}$$

Eq. 12-5, $$C_5 = \frac{1}{2\pi f_1 (R_8 + R_L)/10} = \frac{1}{2\pi \times 100\text{ Hz} \times (12\ \text{k}\Omega + 120\ \text{k}\Omega\ 10}$$

$$= 0.12\ \mu\text{F} \text{ (standard value)}$$

Other two-stage circuits can be designed to use emitter current bias, (for example, see Fig. 13-28). However, series voltage feedback produces more stable (closed-loop) voltage gains than single-stage emitter current feedback. Series voltage feedback also produces reduced output impedance, as well as increased input impedance. Emitter current feedback increases the circuit input impedance, but leaves the output impedance unaffected. Consequently, overall series voltage negative feedback is normally preferable to single-stage emitter current feedback.

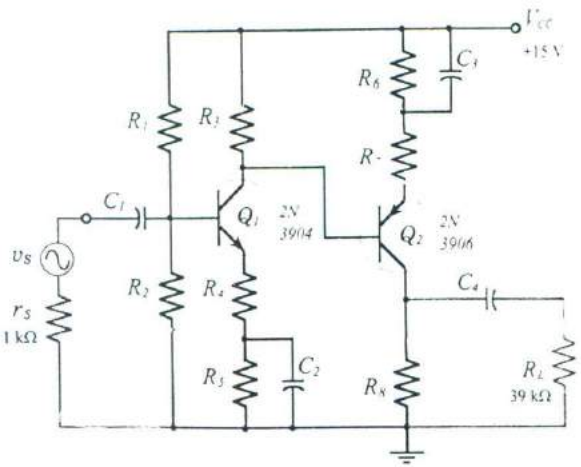


Figure 13-28
Two-stage direct-coupled BJT amplifier circuit using emitter current feedback.

Practise Problems

13-5.1 Calculate resistor values for the emitter current feedback circuit in Fig. 13-28 to give $A_v = 600$. The transistor parameters are $h_{ie} = 1.5$ kΩ and $h_{fe} = 60$, and the cutoff frequency is to be $f_1 = 80$ Hz.

13-5.2 Determine suitable capacitor values for the circuit in Problem 13-5.1.

13-6 Parallel Current Negative Feedback

Current Feedback Circuit

In series-voltage feedback, a portion of the output voltage is fed back in series with the signal source. In *parallel current feedback*, a portion of the output current is fed back in parallel with the signal source. Just as series voltage feedback stabilizes the voltage gain of a circuit, so parallel current feedback stabilizes the current gain.

Consider the *dc* feedback pair circuit in Fig. 13-29. An unbypassed resistor (R_{F2}) is connected in the emitter circuit of transistor Q_2, and Q_1 bias resistor (R_{F1}) is connected at the emitter terminal of Q_2. With this arrangement, any *ac* voltage developed across R_{F2} is applied to R_{F1}.

Look at the instantaneous polarities of the input voltage (v_i) and feedback voltage (v_f), as illustrated in the *ac* equivalent circuit in Fig. 13-30. When v_i is moving in a positive direction, v_{c1} is negative-going. Because the emitter of Q_2 follows the voltage (v_{c1}) at its base, v_f (across R_{F2}) is also negative-going at this time.

Now look at the instantaneous *ac* current directions indicated in Fig. 13-30. When v_i goes positive, the signal current (i_s) flows into the circuit, and an input current (i_i) flows into the base of Q_1, as shown. Because v_f goes negative when v_i is positive-going, a feedback current (i_f) flows in R_{F1} in the direction indicated, (from Q_1 base toward Q_2 emitter). Thus, some of the signal current is diverted away from the base of Q_1. This means that the output current (i_{c2}) is less than it would be if there was no current feedback, consequently, the circuit current gain is reduced.

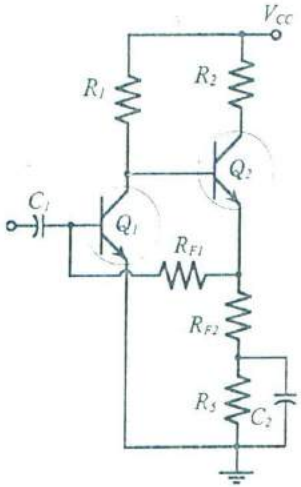


Figure 13-29
DC feedback pair with parallel current negative feedback. The circuit current gain is
$A_{i(CL)} \approx (R_{F1} + R_{F2})/R_{F2}$

Current Gain

To determine the effect of negative feedback on the circuit current gain, first investigate the current gain without feedback, (the open-loop current gain). Suppose that R_{F2} in Fig. 13-30 has a bypass capacitor connected across it, so that there is no negative feedback. Assuming that the resistance of R_{F1} is very much larger than the Q_1 input impedance (h_{ie1}), virtually all of i_s enters the base of Q_1, (see Fig. 13-30).

So, $\quad i_s \approx i_1$

and $\quad i_{c1} \approx h_{fe1}\, i_1$

i_{c1} divides between R_1 and Z_{i2}. Using the current divider equation,

$$i_{b2} = \frac{i_{c1} \times R_1}{R_1 + Z_{i2}}$$

$$i_o = i_{c2} = h_{fe2}\, i_{b2}$$

or,
$$i_o = \frac{h_{fe2}\, i_{c1}\, R_1}{R_1 + Z_{i2}} = \frac{h_{fe1}\, h_{fe2}\, i_i\, R_1}{R_1 + Z_{i2}}$$

The open-loop current gain is,

$$A_i = \frac{i_o}{i_i}$$

$$\boldsymbol{A_i = \frac{h_{fe1}\, h_{fe2}\, R_1}{R_1 + Z_{i2}}} \qquad \textbf{(13-21)}$$

Now derive an equation for the current gain with negative feedback. Referring to Fig. 13-30, it is seen that i_o (in the emitter circuit of Q_2) divides between R_{F1} and R_{F2}, giving

$$i_f = \frac{i_o \times R_{F2}}{R_{F1} + R_{F2}} = i_o B$$

where
$$B = \frac{R_{F2}}{R_{F1} + R_{F2}}$$

Also,
$$i_s = i_i + i_f = i_i + i_o B$$

and,
$$i_o = A_i\, i_i$$

so,
$$i_s = i_i + (A_i\, i_i B) = i_i(1 + A_i B)$$

The closed-loop current gain is,

$$A_{i(CL)} = \frac{i_o}{i_s} = \frac{A_i\, i_i}{i_i(1 + A_i B)}$$

$$\boldsymbol{A_{i(CL)} = \frac{A_i}{1 + A_i B}} \qquad \textbf{(13-22)}$$

If $A_i B >> 1$, then

$$\boldsymbol{A_{i(CL)} \approx \frac{1}{B} \approx \frac{R_{F1} + R_{F2}}{R_{F2}}} \qquad \textbf{(13-23)}$$

It is seen that,

parallel current negative feedback stabilizes circuit current gain.

It should be noted that, in the current gain equations, the ac output current is taken as the current in the collector circuit of transistor Q_2. How this current divides between a capacitor-

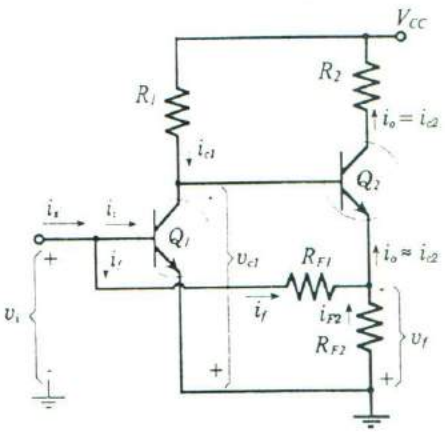


Figure 13-30
AC equivalent circuit for the current feedback circuit Fig. 13-29, showing ac voltages and currents.

coupled external load (R_L) and the Q_2 collector resistor (R_3) depends on the values of R_L and R_3.

Output and Input Impedances

In the circuit shown in Figs. 13-29 and 13-30, the Q_2 collector resistor (R_2) is outside the feedback loop. Therefore, like the case of emitter current feedback, the output impedance of this circuit is largely unaffected by feedback. (It can be shown that the impedance *looking into* the collector of Q_2 is increased by current feedback.) So, the circuit output impedance is, (from Eq. 6-14),

$$Z_o \approx R_2$$

Assuming that $R_{F1} >> h_{ie1}$, the circuit input impedance without feedback is,

$$Z_i \approx h_{ie1} = \frac{v_i}{i_s}$$

As already shown, with negative feedback,

$$i_s = i_i + i_f = i_i(1 + A_i B)$$

so,

$$Z_i = \frac{v_i}{i_s} = \frac{v_i}{i_i(1 + A_i B)}$$

or,

$$\mathbf{Z_i = \frac{h_{ie1}}{1 + A_i B}} \qquad \textbf{(13-24)}$$

Therefore,

parallel current negative feedback reduces circuit input impedance by a factor of $\mathbf{(1 + A_i B)}$.

Although R_{F1} is a bias resistor, it is also part of the feedback network, so it is *not* in parallel with the circuit input impedance.

Another way of looking at the circuit input impedance is in terms of the the feedback resistor R_{F1} and the voltage gain of the first stage. It can be shown that,

$$\mathbf{Z_i = h_{ie1} \| \frac{R_{F1}}{A_{v1}}} \qquad \textbf{(13-25)}$$

Circuit Design

As with other negative feedback circuits, design of a parallel current negative feedback amplifier is approached by first ignoring the *ac* negative feedback components. Resistors R_{F2} and R_5 in Fig. 13-29 are calculated as a single emitter resistor ($R_E = R_{F2} + R_5$) to fulfil the desired *dc* conditions. Also, R_{F1} is calculated (as for other *dc* feedback bias circuits) to provide the required base current to Q_1. R_{F2} is then calculated from Eq. 13-23. Usually, the resistance of R_{F1} is very large, and this results in a calculated resistance for R_{F2} larger than ($R_{F2} + R_5$)! In this case, the base resistor for Q_1

should be made up of two resistors one of which is bypassed: see ($R_2 = R_{F1} + R_7$) in Fig. 13-31. R_{F1} is the unbypassed portion of R_2, and this is calculated in relation to R_{F2}.

Bypass capacitor C_2 (in Fig. 13-31) is calculated to give $X_{C2} = R_{F2}$ at the desired lower cutoff frequency. Because the signal is derived from a current source, the impedance of the input coupling capacitor (C_1) at f_1 should be much smaller than the (normally-high) impedance of the signal source. Capacitor C_3 is determined by making X_{C3} very much smaller than R_{F1} at f_1.

Example 13-14

Analyze the circuit in Fig. 13-31 to determine the current gain and the input impedance. Assume transistor parameters of $h_{fe} = 100$, and $h_{ie} = 2$ kΩ.

Solution

From Eq. 6-20, $Z_{i2} = h_{ie2} + (1 + h_{fe2})R_4 = 2\text{ k}\Omega + (1 + 100)100\ \Omega$

$= 12.1$ kΩ

Open-loop current gain,

Eq. 13-21, $$A_i = \frac{h_{ie1}h_{fe2}R_1}{R_1 + Z_{i2}} = \frac{100 \times 100 \times 5.6\text{ k}\Omega}{5.6\text{ k}\Omega + 12.1\text{ k}\Omega}$$

$= 3164$

From Eq. 13-23, $$B = \frac{R_4}{R_5 + R_4} = \frac{100\ \Omega}{2.2\text{ k}\Omega + 100\ \Omega}$$

$$= \frac{1}{23}$$

Closed-loop current gain,

Eq. 13-22, $$A_{i(CL)} = \frac{A_i}{1 + A_i B} = \frac{3164}{1 + (3164/23)}$$

$= 22.8$

Eq. 13-24, $$Z_i = \frac{h_{ie1}}{1 + A_i B} = \frac{2\text{ k}\Omega}{1 + (3164/23)}$$

$= 14.6\ \Omega$

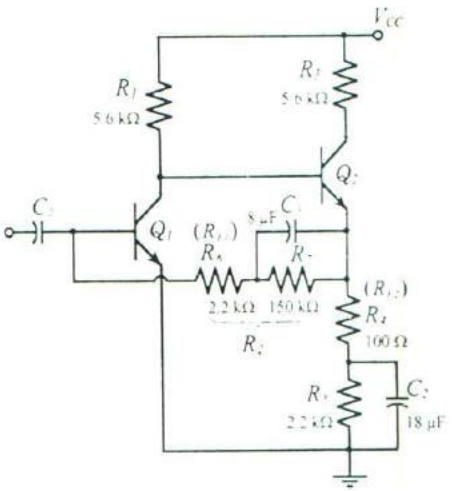


Figure 13-31
Current feedback circuit with a portion of R_2 bypassed to minimise R_4. The current gain is $A_{i(CL)} \approx (R_6 + R_4)/R_4$

Practise Problems

13-6.1 Modify the dc feedback pair circuit shown in Fig. 12-25(a) to give $A_{i(CL)} = 55$ and $f_1 = 80$ Hz. Assume $r_s = 12$ kΩ.

13-6.2 Assuming transistor parameters of $h_{ie} = 1$ kΩ and $h_{fe} = 50$, calculate Z_i and $A_{i(CL)}$ for the circuit in Problem 13-6.1.

13-7 Additional Effects of Negative Feedback

Decibels of Feedback

Negative feedback can be measured in decibels. A statement that 40 dB of feedback has been applied to an amplifier means that the amplifier gain has been reduced by 40 dB, (that is, by a factor of 100). Thus,

$$A_{CL} = A_v - 40 \text{ dB} = \frac{A_v}{100}$$

Bandwidth

Consider the typical gain-frequency response of an amplifier, as illustrated in Fig. 13-32. Without negative feedback, the amplifier open-loop (A_v) gain falls off to its lower 3 dB frequency ($f_{1(OL)}$), as illustrated. This is usually due to the impedance of bypass capacitors increasing as the frequency decreases. Similarly, the open-loop upper cutoff frequency ($f_{2(OL)}$) is produced by transistor cutoff, by shunting capacitance, or by a combination of both. As discussed in Section 8-2, the circuit open-loop bandwidth is,

$$BW_{OL} = f_{2(OL)} - f_{1(OL)}$$

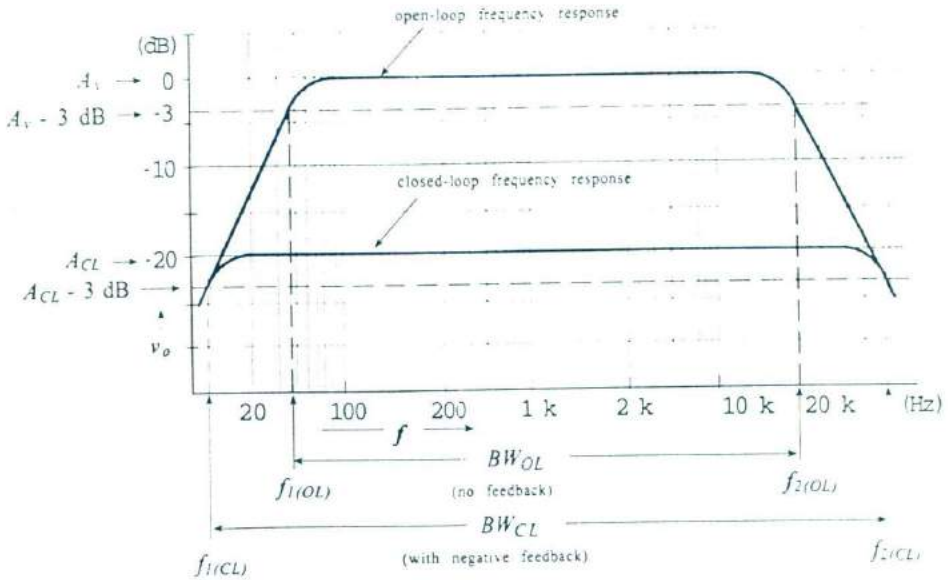


Figure 13-32
Amplifier frequency response with and without negative feedback. Negative feedback extends the amplifier bandwidth.

Now look at the typical frequency response for the same amplifier when negative feedback is used. The closed-loop gain (A_{CL}) is much smaller than the open-loop gain, and A_{CL} does not begin to fall off (at high or low frequencies) until A_v (open-loop) falls substantially. Consequently, $f_{1(CL)}$ is much lower than $f_{1(OL)}$, and $f_{2(CL)}$ is much higher than $f_{2(OL)}$. So, the circuit bandwidth with negative feedback (the closed-loop bandwidth) is much greater than the bandwidth without negative feedback.

$$BW_{CL} = f_{2(CL)} - f_{1(CL)}$$

From Eq. 13-2,

$$A_{CL} = \frac{A_v}{1 + A_v B}$$

It can be shown that there is a 90° phase shift associated with the open-loop gain at frequencies below $f_{1(OL)}$ and above $f_{2(OL)}$. Thus, Eq. 13-2 must be rewritten as,

$$A_{CL} = \frac{-jA_v}{1 - jA_v B}$$

or,
$$|A_{CL}| = \frac{A_v}{\sqrt{[1 + (A_v B)^2]}}$$

When $A_v = 1/B$,

$$|A_{CL}| = \frac{1/B}{\sqrt{[1 + 1]}} = \frac{A_{CL}}{\sqrt{2}}$$
$$= A_{CL} - 3 \text{ dB}$$

Thus, for a negative feedback amplifier designed to have the widest possible bandwidth, the cutoff frequencies would occur when the open-loop gain falls to the equivalent of $1/B$. Thus, $f_{2(CL)}$ occurs when,

$$\boldsymbol{A_v = 1/B = A_{CL}} \qquad \textbf{(13-26)}$$

So, for example, the cutoff frequencies for a negative feedback amplifier designed for a closed-loop gain of 100 would occur when the open-loop gain falls to 100. It is seen that,

negative feedback increases amplifier bandwidth.

The upper cutoff frequency for an amplifier is usually greater than 20 kHz, and the lower cutoff frequency is around 100 Hz, or lower. So, $f_2 >> f_1$, and consequently,

$$BW = f_2 - f_1 \approx f_2$$

This means that the amplifier bandwidth is essentially equal to the upper cutoff frequency.

Now refer to Fig. 13-32 once again. The amplifier gain multiplied by the upper cutoff frequency is a constant quantity. This is known as the *gain-bandwidth product*. Therefore,

$$A_{CL} \times f_{2(CL)} = A_v \times f_{1(OL)}$$

or,
$$f_{2(CL)} = \frac{A_v f_{1(OL)}}{A_{CL}} \qquad \textbf{(13-27)}$$

So, the closed-loop upper cut-off frequency for a negative feedback amplifier can be calculated from the open-loop upper cutoff

frequency, the open-loop gain, and the closed-loop gain.

Harmonic Distortion

Harmonic Distortion occurs when a transistor or other device is driven beyond the linear range of its characteristics. Figure 13-33 shows the I_C/V_{BE} characteristics of a transistor biased to a base-emitter voltage V_B. As illustrated, when the base-emitter voltage changes ($\pm v_{be}$) are very small, the collector current changes by equal positive and negative amounts ($\pm i_c$). When $\pm v_{be}$ is large, the change in $+i_c$ is greater than the change in $-i_c$. This is because of the nonlinearity in the I_C/V_{BE} characteristics. The result is *harmonic distortion* (or *nonlinear distortion*) in the waveform of i_c and in the amplifier output.

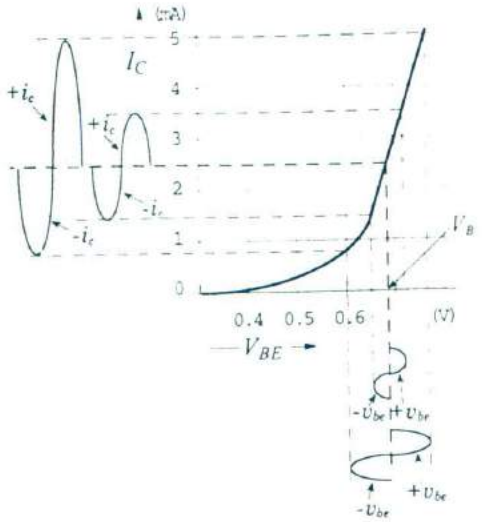


Figure 13-33
Harmonic distortion in the output of an amplifier is caused by nonlinearity in transistor characteristics. Negative feedback reduces this type of distortion by a factor of $(1 + A_v B)$.

The distorted waveform can be shown to consist of a *fundamental* frequency waveform and a number of smaller amplitude *harmonic* components, (see Fig. 13-34). The fundamental waveform is the amplified signal, or amplifier output voltage (v_o), and the harmonics are unwanted voltage components (v_H). The *harmonic distortion* is the rms value of v_H expressed as a percentage of the rms value of v_o. The harmonics (generated within the feedback loop) are reduced by negative feedback by a factor of $(1 + A_v B)$. So that,

$$\textbf{\% distortion with } \textit{NFB} = \frac{\textbf{\% distortion without } \textit{NFB}}{(1 + A_v B)} \qquad \textbf{(13-28)}$$

So,

negative feedback reduces harmonic distortion.

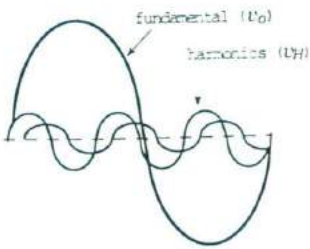


Figure 13-34
Harmonic distortion in an amplifier is reduced by negative feedback.

Attenuation Distortion

Attenuation distortion occurs when different frequencies are amplified by different amounts. This type of distortion is the result of the amplifier open-loop gain being frequency-dependent, (see Fig. 13-35). When negative feedback is used, the closed-loop gain is a constant quantity largely independent of signal frequency within the circuit bandwidth. Like harmonic distortion, attenuation distortion is reduced by a factor of $(1 + A_vB)$ by negative feedback. Equation 13-28 applies. Thus,

negative feedback reduces attenuation distortion.

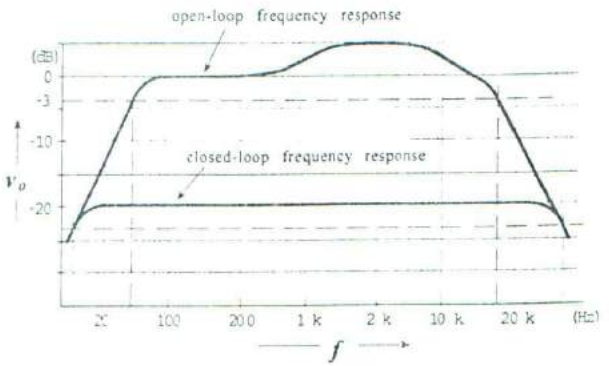


Figure 13-35
Attenuation distortion, resulting from different signal frequencies being amplified by different amounts, is reduced by negative feedback.

Phase Shift

Input signals to an amplifier go through phase-shifts from the input to the output. The waveforms in Fig. 13-36 show that, in a two-stage circuit, there is a 180° phase shift from v_s to v_{o1}, and a further 180° shift from v_{o1} to v_{o2}. In some cases, an amplifier can produce different phase shifts for different signal frequencies. For example, higher frequency signals might be shifted by more than 180° at each stage, resulting in an undesirable phase difference (ø) between input and output, as illustrated.

Audio (and other) signals at an amplifier input are usually made up of a combination of component waveforms with different amplitudes and different frequencies. So, any variation in amplifier-introduced phase shift will create distortion in the output waveform that is not present in the input.

To investigate the effect of negative feedback on amplifier phase shift, assume that the open-loop gain has a phase shift angle of ø, and that the closed-loop phase shift is $ø_{CL}$. Then,

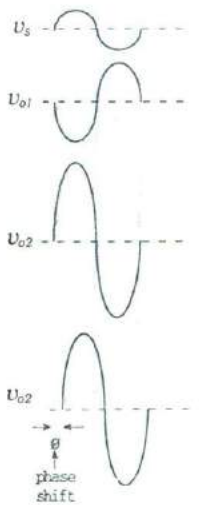


Figure 13-36
Undesirable phase shifts in amplifier ac waveforms are reduced by negative feedback.

$$\text{open-loop gain} = A_v\angle ø$$

and,
$$A_{CL}\angle ø_{CL} = \frac{A_v\angle ø}{1 + A_vB\angle ø} = \frac{A_vB \sin ø}{1 + A_vB\cos ø + jA_vB \sin ø}$$

giving,
$$ø_{CL} = ø - \tan^{-1}\frac{A_vB \sin ø}{1 + A_vB\cos ø} \qquad (13\text{-}29)$$

So,

negative feedback reduces amplifier phase shift

by an angle of,

$$\tan^{-1}\frac{A_v B \sin \phi}{1 + A_v B \cos \phi}$$

Example 13-15

A negative feedback amplifier has an open-loop gain of 60 000 and a closed-loop gain of 300. If the open-loop upper cutoff frequency is 15 kHz, estimate the closed-loop upper cutoff frequency. Also, calculate the total harmonic distortion with feedback if there is 10% harmonic distortion without feedback.

Solution

Eq. 13-27.
$$f_{2(CL)} = \frac{A_v \, f_{1(OL)}}{A_{CL}} = \frac{60\,000 \times 15 \text{ kHz}}{300}$$
$$= 3 \text{ MHz}$$

Eq. 13-28.
$$\%\text{ distortion with } NFB = \frac{\%\text{ distortion without } NFB}{(1 + A_v B)} = \frac{10\%}{1 + (60\,000/300)}$$
$$= 0.48\%$$

Noise

Circuit *noise* generated within the feedback loop of an amplifier is reduced by a factor of $(1 + A_v B)$ in the same way that unwanted harmonics are reduced. It should be noted that only the noise generated within the feedback loop is reduced by feedback. Noise produced by bias resistors outside the feedback loop will not be affected by feedback.

Negative feedback reduces circuit noise.

Circuit Stability

In Chapter 16, it is explained that, for a circuit to oscillate, the *loop phase shift* must be 360° when the *loop gain* is 1. The loop phase shift is the phase shift around the loop from the amplifier input to the output, and back via the feedback network to the input. Similarly, the loop gain is the product of the amplifier open-loop gain and the feedback network attenuation, $(A_v B)$.

The loop phase shift of an amplifier can approach 360° as the gain falls off at the high end of the bandwidth. In this case, the amplifier might oscillate, and it is said to be *unstable*. The usual method of combating this kind of instability is to include small shunting capacitors from the transistor collector terminals to ground. These tend to cause the loop gain to fall below 1 before the loop phase shift approaches 360°.

Amplifier instability and compensation techniques are further covered in Ch. 15.

Practise Problems

13-7.1 The amplifier in Ex. 13-15 has a 15° open-loop phase shift at high signal frequencies. Calculate the phase shift with negative feedback.

13-7.2 A negative feedback amplifier with a closed loop gain of 250 has a 4 MHz upper cutoff frequency. Calculate the open-loop cutoff frequency if the open-loop gain is 200 000.

Chapter-13 Review Questions

Section 13-1

13-1 Draw a sketch to illustrate the principle of series voltage negative feedback, and briefly explain. Also, list the major effects of negative feedback on an amplifier.

13-2 Derive an equation for the voltage gain of an amplifier that uses series voltage negative feedback.

13-3 Derive an equation for the input impedance of an amplifier that uses series voltage negative feedback.

13-4 Derive an equation for the output impedance of an amplifier that uses series voltage negative feedback.

13-5 Discuss the effect of input bias resistors on the input impedance of a negative feedback amplifier, and the effect of a collector resistor at the output of a *BJT* negative feedback amplifier.

Section 13-2

13-6 Sketch the circuit of a two-stage, capacitor-coupled, *BJT* amplifier that uses series voltage negative feedback. Briefly explain how the feedback operates, and write an equation for the voltage gain in terms of the feedback components.

13-7 Briefly discuss the procedure for determining the negative feedback components for the circuit in Question 13-6

13-8 For the circuit in Question 13-6, write equations for the input impedance and output impedance in terms of the circuit components and transistor parameters.

Section 13-3

13-9 Sketch the circuit of a direct-coupled, two-stage *BJT* amplifier that uses series voltage negative feedback. Q_1 should be an *npn* device, and Q_2 should be a *pnp* transistor. Briefly explain the feedback operation, and write the equation for voltage gain in terms of the circuit components.

13-10 For the circuits in Question 13-9, write equations for Z_{in} and Z_{out} in terms of the transistor parameters and the circuit components.

13-11 Briefly discuss the design procedures for the circuit in Questions 13-9.

13-12 Sketch the circuit of a *dc* feedback pair that uses series voltage negative feedback. Explain the operation of the feedback network, and write an equation for the voltage gain in terms of the circuit components.

13-13 For the circuits in Questions 13-12, write equations for Z_{in} and Z_{out} in terms of the transistor parameters and the circuit components.

13-14 Briefly discuss the design procedures for the circuit in Questions 13-12.

13-15 Sketch the circuit of a direct-coupled, two-stage, *BIFET* amplifier that uses series voltage negative feedback. Explain the operation of the circuit, and write an equation for the voltage gain in terms of the circuit components.

13-16 For the circuits in Questions 13-15, write equations for Z_{in} and Z_{out} in terms of the transistor parameters and the circuit components.

13-17 Briefly discuss the design procedures for the circuit in Questions 13-15.

Section 13-4

13-18 Sketch the circuit of a two-stage, direct-coupled negative feedback amplifier that uses a two-transistor, emitter-coupled input stage. Explain the operation of the circuit.

13-19 Write equations for $A_{v(CL)}$, Z_{in}, and Z_{out} for the circuit in Questions 13-18.

13-20 Briefly discuss the design procedures for the circuit in Questions 13-18.

Section 13-5

13-21 Sketch the circuit of a single-stage common emitter amplifier that uses emitter current feedback. Briefly explain the operation of the circuit.

13-22 For the single-stage circuit sketched for Question 13-21, write equations for $A_{v(CL)}$, Z_{in}, and Z_{out}.

13-23 Briefly explain the design procedure for the circuit in Question 13-21.

13-24 Sketch a two-stage, capacitor-coupled, *BJT* amplifier that uses emitter current feedback in each stage. Briefly explain the operation of the circuit.

13-25 Discuss the design procedure for the two-stage circuit in Question 13-24.

13-26 Sketch the circuit of a direct-coupled, two-stage, *BJT* amplifier that uses emitter current feedback. Q_1 should be

an *npn* device, and Q_2 should be a *pnp* transistor.

13-27 Write equations for $A_{v(CL)}$, Z_{in}, and Z_{out} for the circuit in Question 13-26.

Section 13-6

13-28 Sketch a direct-coupled *dc* feedback pair amplifier that uses parallel current negative feedback. Briefly explain the operation of the circuit, and discuss its performance characteristics.

13-29 Write equations for $A_{i(CL)}$, Z_{in}, and Z_{out} for the circuit in Question 13-28.

13-30 Discuss the design procedure for the two-stage circuit in Question 13-28.

Section 13-7

13-31 Using illustrations, explain the effects of negative feedback on the bandwidth of an amplifier. Discuss the effect of open-loop gain reduction on the closed-loop gain.

13-32 Draw sketches to explain how harmonic distortion occurs in an amplifier. Discuss the effects of negative feedback on harmonic distortion.

13-33 Explain attenuation distortion, and discuss the effects of negative feedback on attenuation distortion.

13-34 Explain how phase shift distortion occurs in an amplifier, and discuss how negative feedback affects phase shift.

13-35 Discuss the effect of negative feedback on circuit noise.

13-36 Briefly discuss amplifier stability with negative feedback.

Chapter-13 Problems

Section 13-1

13-1 A two-stage *BJT* amplifier has an open-loop voltage gain of 224 000 when the transistors have a maximum h_{fe} value, and 14 000 when the transistor h_{fe} values are a minimum. Calculate the closed-loop gain for both cases when negative feedback is used with a feedback factor of 1/125.

13-2 The amplifier in Problem 13-1 has an input impedance of 1.2 kΩ at the base of the input transistor when negative feedback is not used. Voltage divider bias with R_1 = 150 kΩ and R_2 = 56 kΩ is used at the input transistor. Calculate the circuit input impedance (with negative feedback) at both h_{fe} extremes.

13-3 The output transistor in the amplifier in Problem 13-1 has $1/h_{oe}$ = 80 kΩ, and a 5.6 kΩ collector resistor. Calculate the circuit output impedance at both h_{fe} extremes.

13-4 The closed loop gain of a negative feedback amplifier is measured as 99.7 when the feedback factor is 1/100, and as 297 when a feedback factor of 1/300 is used. Determine the open-loop gain.

Section 13-2

13-5 The circuit in Fig. 13-16 is to be modified to have an overall voltage gain of 50 and a lower cutoff frequency of 150 Hz. Calculate the new values for R_{F1}, R_{F2}, C_2, and C_{F1}.

13-6 Analyze the negative feedback amplifier in Problem 13-5 to determine the input and output impedances. Assume that the transistor parameters are h_{ie} = 800 Ω, h_{fe} = 60, and $1/h_{oe}$ = 90 kΩ. The open-loop gain is 97 000.

13-7 A two-stage, capacitor-coupled, *BJT* amplifier as in Fig. 12-15 has the following components: R_1 = 150 kΩ, R_2 = 56 kΩ, R_3 = 4.7 kΩ, R_4 = 5.6 kΩ, R_5 = 150 kΩ, R_6 = 56 kΩ, R_7 = 4.7 kΩ, R_8 = 5.6 kΩ, R_L = 47 kΩ, C_1 = 10 μF, C_2 = 180 μF, C_3 = 10 μF, C_4 = 180 μF. Modify the circuit to use series voltage negative feedback. The voltage gain is to be 180, and the required lower cutoff frequency is 90 Hz.

13-8 Calculate the input and output impedances for the circuit in Problem 13-7. Take the transistor parameters as: h_{ie} = 1.2 kΩ, h_{fe} = 90, and $1/h_{oe}$ = 75 kΩ.

Section 13-3

13-9 A two-stage, direct-coupled, *BJT* amplifier as in Fig. 12-20 has the following components: R_1 = 100 kΩ, R_2 = 39 kΩ, R_3 = 3.9 kΩ, R_4 = 3.9 kΩ, R_5 = 2.7 kΩ, R_6 = 3.9 kΩ, R_L = 33 kΩ, C_1 = 8 μF, C_2 = 150 μF, C_3 = 150 μF. Modify the circuit to use series voltage negative feedback to give a gain of 75, and a lower cutoff frequency of 60 Hz.

13-10 Calculate the input and output impedances for the circuit in Problem 13-9 if the transistor parameters are: h_{ie} = 1 kΩ, h_{fe} = 120, and $1/h_{oe}$ = 100 kΩ.

13-11 The two-stage, direct-coupled, *BJT* amplifier designed in Exs. 12-8 and 12-9 (and analyzed in Ex. 12-10) is to be converted into a negative feedback amplifier with a voltage gain of 120, and a lower cutoff frequency of 20 Hz. Make the necessary modifications and determine the new component values.

13-12 A two-stage, direct-coupled amplifier with complementary transistors is to be designed to use negative feedback, as in Fig. 13-17. The overall voltage gain is to be 150, and the lower 3 dB frequency is to be 200 Hz. Calculate suitable values for R_{F1}, R_{F2}, and C_2.

13-13 A *dc* feedback pair using negative feedback (as in Fig. 13-18) is to have $A_{v(CL)}$ = 80, f_1 = 120 Hz, and f_2 = 50 kHz. Calculate suitable component values for the feedback network.

13-14 Calculate Z_{in} and Z_{out} for the circuit in Fig. 13-18. Use the component values shown, and transistor parameters of: h_{ie} = 1.2 kΩ, h_{fe} = 90, and $1/h_{oe}$ = 95 kΩ.

13-15 A two-stage, negative feedback, *BIFET* amplifier, as in Fig. 13-19, is to have $A_{v(CL)}$ = 19, and f_1 = 400 Hz. Calculate suitable values for R_{F1}, R_{F2}, and C_{F1}.

13-16 Calculate the direct current through the feedback networks in the circuits in Figures 13-17 and 13-19 when the feedback network is directly connected instead of capacitor coupled.

Section 13-4

13-17 The circuit in Fig. 13-21 is to be designed to have $A_{v(CL)}$ = 175. Using V_{CC} = ±12.5 V, select suitable current and voltage levels, and calculate resistor values. Use *2N3904* and *2N3906* transistors.

13-18 Calculate the minimum values of $A_{v(CL)}$, Z_{in}, and Z_{out} for the circuit in Problem 13-17.

13-19 A two-stage differential amplifier circuit (as in Fig. 13-21) is to be designed to amplify a 10 mV input to 750 mV. The amplifier supply is ±9 V, and the transistors to be used have h_{FE} = h_{fe} = 150, h_{ie} = 1.5 kΩ, and $1/h_{oe}$ = 150 kΩ. determine suitable resistor values.

13-20 Calculate Z_i and Z_o for the circuit in Problem 13-19.

Section 13-5

13-21 Design a single-stage *BJT* common emitter amplifier with emitter current feedback. The circuit specification is: Q_1 = 2N3906, V_{CC} = -18 V, R_L = 150 kΩ, A_v = 45, f_1 = 50 Hz.

13-22 Analyze the circuit designed for Problem 13-21 to determine A_v, Z_{in}, Z_{out}, and f_1.

13-23 A common emitter amplifier as in Fig. 12-1 has the following components: R_1 = 120 kΩ, R_2 = 33 kΩ, R_C = 6.8 kΩ, R_E = 3.3 kΩ, and R_L = 68 kΩ. Modify the circuit to use emitter current feedback. The voltage gain is to be 23, and the required lower cutoff frequency is 60 Hz. The transistor parameters are: h_{ie} = 1.2 kΩ, h_{fe} = 90, and $1/h_{oe}$ = 95 kΩ.

13-24 Calculate A_v, Z_{in}, and Z_{out} for the circuit in Problem 13-23.

13-25 Two stages of the circuit in Problem 13-23 are to be connected in cascade to give an overall voltage gain of approximately 1600 and a lower cutoff frequency of 50 Hz. Determine the necessary modifications.

13-26 An amplifier is to be designed using two stages of the circuit designed for Problem 13-21. The overall voltage gain is to be 900 and the lower cutoff frequency is to be 100 Hz. Determine the necessary modifications.

13-27 Analyze the circuit designed for Problem 13-25 to determine A_v, Z_{in}, and Z_{out}.

13-28 Analyze the circuit designed for Problem 13-26 to determine A_v, Z_{in}, and Z_{out}.

13-29 A *dc* feedback pair [as in Fig 12-25(a)] is to be modified to use emitter current feedback. The circuit specification is: V_{CC} = 15 V, R_L = 80 kΩ, A_v = 400, f_l = 70 Hz. Design the circuit to use *2N3904 BJTs*.

13-30 Analyze the circuit designed for Problem 13-29 to determine A_v, Z_{in}, and Z_{out}.

Section 13-6

13-31 A *dc* feedback pair is to be designed to use parallel current negative feedback, as in Fig. 13-29. Using V_{CC} = 22 V, and transistors with $h_{FE} = h_{fe}$ = 75 and h_{ie} = 1.5 kΩ, design the circuit to have I_C = 0.9 mA, A_i = 22, f_l = 200 Hz.

13-32 Calculate A_i and Z_{in} for the circuit in Problem 13-31.

13-33 A *dc* feedback pair as in Fig. 12-25(a) has the following components: R_1 = 12 kΩ, R_2 = 330 kΩ, R_3 = 4.7 kΩ, R_4 = 2.7 kΩ, and C_2 = 240 μF. Determine the necessary modification to give A_i = 30 and f_l = 75 Hz.

13-34 Analyze the circuit designed for Problem 13-33 to determine A_i and Z_{in}. Assume $h_{fe1} = h_{fe2}$ = 100, and $h_{ie1} = h_{ie2}$ = 1 kΩ.

Section 13-7

13-35 The amplifier in Example 13-4 has 5% total harmonic distortion in its output waveform when negative feedback is not used. Calculate the new distortion content with negative feedback.

13-36 If the amplifier in Example 13-4 has a 17° open-loop phase shift at high frequencies, determine the phase shift with negative feedback.

13-37 The negative feedback amplifier in Examples 13-7 and 13-8 has a 30 kHz open-loop upper cutoff frequency. Calculate the upper cutoff frequency with negative feedback.

13-38 A negative feedback with B = 1/105 produces a 2 V output when the input is 20 mV. Distortion content in the output is 1%. Find the new signal level to give 2 V output when the negative feedback is disconnected. Also, determine the new distortion content in the output.

Practise Problem Answers

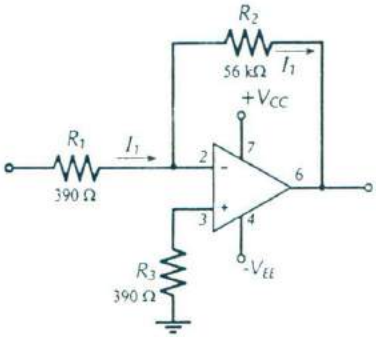
13-1.1 1.42 kΩ, 5.2 kΩ, 26.3 kΩ, 28 Ω, 134.9
13-2.1 100 Ω, 3.9 kΩ, 33 μF, 10 kΩ, 33 μF
13-2.2 27.7 kΩ, 52 Ω
13-3.1 330 Ω, 68 kΩ, 171 μA

13-3.2 150 Ω, 2.7 kΩ, 5.6 μF, 30 μF, 3000 pF
13-4.1 4.7 kΩ, 10 kΩ, 6.8 kΩ, 10 kΩ, (220 kΩ + 10 kΩ), 4.7 kΩ, 4.7 kΩ, 15 kΩ
13-4.2 4.7 kΩ, 12.4 Ω
13-5.1 (68 kΩ + 10 kΩ), 47 kΩ, 4.7 kΩ, 120 Ω, 4.7 kΩ, 2.7 kΩ, 150 Ω, 3.9 kΩ
13-5.2 2.7 μF, 27 μF, 22 μF, 0.47 μF
13-6.1 100 Ω, 5.6 kΩ, 1.8 μF, 20 μF, 39 μF
13-6.2 61 Ω, 878
13-7.1 0.08°
13-7.2 5 kHz

Chapter 14
IC Operational Amplifiers and Basic Op-Amp Circuits

Chapter Contents

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Objectives

You will be able to:

1. Sketch and briefly explain an operational amplifier circuit symbol and the basic input and output stages. Identify all terminals.
2. List and discuss the most important op-amp parameters.
3. Design op-amp bias circuits, and show how to null the output offset.
4. Sketch the following linear op-amp circuits in direct-coupled and capacitor-coupled configuration, and explain the operation of each:
   - Voltage follower
   - Noninverting amplifier
   - Inverting amplifier
5. Analyze and design circuits of the type listed in item 4 above.
6. Sketch the following linear op-amp circuits and explain the operation of each:
   - Summing amplifier
   - Difference amplifier
   - Instrumentation amplifier
7. Analyze and design circuits of the type listed in item 6 above.
8. Sketch the following nonlinear op-amp circuits and explain the operation of each:
   - Zero crossing detectors
   - Inverting Schmitt trigger circuits
   - Noninverting Schmitt triggers
9. Analyze and design circuits of the type listed in item 8 above.

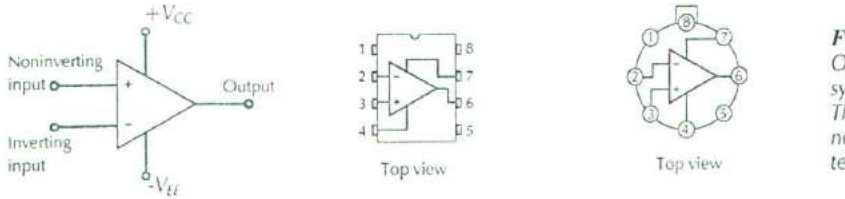
Introduction

An operational amplifier is a high-gain amplifier circuit with two high-impedance input terminals and one low-impedance output. The inputs are identified as *inverting input* and *noninverting input*. The basic circuit consists of a differential amplifier input stage and a low impedance emitter-follower output stage. The voltage gains of integrated circuit (*IC*) operational amplifiers are extremely high, typically 200 000. Because of this high voltage gain, externally connected resistors must be employed to provide negative feedback. Design of *IC* op-amp circuits involves determination of suitable values for the external components. The design calculations are usually much simpler than discrete-component circuit design.

14-1 Integrated Circuit Operational Amplifiers

Circuit Symbol and Packages

Figure 14-1(a) shows the triangular circuit symbol for an operational amplifier (op-amp). As illustrated, there are two input terminals, one output terminal, and two supply terminals. The inputs are identified as *the inverting input* (- sign) and *the noninverting input* (+ sign). A positive-going voltage at the inverting input produces a negative-going (inverted) voltage at the output terminal. Conversely, a positive-going voltage at the noninverting input generates an output which is also positive-going (noninverted). Plus-minus supplies are normally used with op-amps, so the supply terminals are identified as $+V_{CC}$ and $-V_{EE}$.



(a) Op-amp circuit symbol (b) Terminal connections for *DIL* package (c) Terminal connections for metal-can package

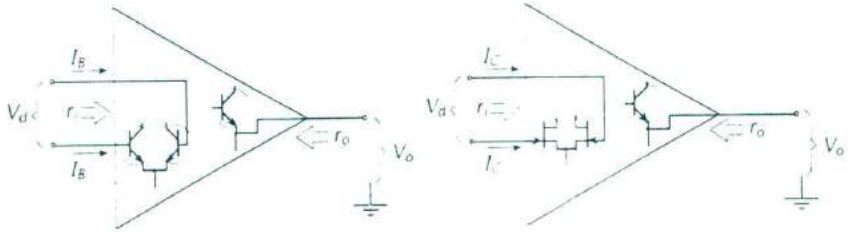
Figure 14-1
Operational amplifier circuit symbol and terminal connections. The + and - signs identify the noninverting and inverting input terminals, respectively.

Two typical op-amp packages are illustrated in Figs. 14-1 (b) and (c). For both the *dual-in-line* (*DIL*) plastic package and the metal can package, terminals 2 and 3 are the inverting and noninverting inputs respectively, terminal 6 is the output, and terminals 7 and 4 are the + and - supply terminals.

Basic Op-Amp Circuit

The basic circuit of an *IC* operational Amplifier is essentially as shown in Fig. 13-23, and further illustrated in Figs. 14-2(a) and (b). The differential-amplifier input stage has two (inverting and

noninverting) high-impedance input terminals, and the emitter follower output stage has a low impedance. An intermediate stage (between the input and output stages) is largely responsible for the op-amp high voltage gain. Figure 14-2(a) shows a *BJT* input stage, while Fig. 14-2(b) has a *FET* input stage. Appropriately, op-amps that exclusively use *BJTs* are termed bipolar op-amps, and those that use a *FET* input stage with *BJT* additional stages are referred to as *BIFET* op-amps.



(a) Basic input and output stages for a bipolar op-amp

(b) Basic input and output stages for a *BIFET* op-amp

Figure 14-2
Input and output stages for bipolar and BIFET operational amplifiers. The FET gate current is very much smaller than the BJT base current.

Important Parameters

Some of the most important parameters for the *741* operational amplifier (one of the most commonly used) are listed in the data sheet portion shown in Fig. 14-3.

The *large signal voltage gain* (A_v), also identified as the *open-loop gain* (A_{vfOL}), for the *741* is listed as as 50 000 minimum and 200 000 typical. This means, for example, that a signal applied as a voltage difference between the two input terminals is amplified at least by a factor 50 000. The typical amplification is 200 000, and the maximum amplification can be considerably greater. This is similar to the situation with the h_{fe} of a *BJT*, where the manufacturer specifies minimum, typical, and maximum values.

The *input bias current* (I_{IB}) is the base current for the op-amp input stage transistors. In Fig. 14-3 I_{IB} is listed as 80 nA typical, and 500 nA maximum.

Ideally, the input stage transistors should be perfectly matched, so that zero voltage difference between the two input (base) terminals should produce a zero output voltage. In practise, there is always some difference between the base-emitter voltages of the transistors, and this results in an *input offset voltage* (V_{IO}), that might be as large as 5 mV for a 741 op-amp. Similarly, because of mismatch of input transistors, there is also an *input offset current* (I_{IO}). For the 741 I_{IO} is a maximum of 200 nA.

The *input resistance* (r_i) and the *output resistance* (r_o) are the resistances at the op-amp terminals when no feedback is involved. Virtually all op-amp applications use negative feedback, so these (resistance) quantities are modified in practical circuits.

The *dc* supply voltage for electronic circuits can vary when the supply current changes, and in some cases there is an *ac ripple*

voltage superimposed on the *dc*. The supply voltage changes can be passed to the output of an amplifier. Ideally, the supply voltage variations should have no effect on the circuit output. How good the amplifier is at attenuating supply voltage variations is defined by the *power supply voltage rejection ratio* (*PSRR*). This is usually specified in decibel form.

Common mode inputs are voltage changes that are applied simultaneously to both input terminal of an operational amplifier. Common mode input voltages can be passed to the output. The *common mode rejection ratio* (*CMRR*) (expressed in *dB*) defines how good the amplifier is at attenuating common mode input voltages.

Electrical characteristics (V_S = ±15 V, T_A = 25°C unless otherwise specified)

Parameters	Conditions	Min	Typ	Max	Unit
Large signal voltage gain (A_v)	$R_L \geq 2$ kΩ, V_{out} = ±10 V	50 000	200 000		
Input bias current (I_{IB})			80	500	nA
Input offset voltage (V_{IO})	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input offset current (I_{IO})			20	200	nA
Input resistance (r_i)		0.3	2		MΩ
Output resistance (r_o)			75		Ω

Figure 14-3
Portion of data sheet for a 741 op-amp.

Practise Problems

14-1.1 Determine the following parameter values from the *LM108* op-amp data sheet in Appendix 1-14: large signal voltage gain, input bias current, input offset voltage, input resistance.

14-1.2 Repeat Problem 14-1.1 for the *LF353* op-amp in Appendix 1-15.

14-2 Biasing Operational Amplifiers

Biasing Bipolar Op-amps

Like other electronic devices, operational amplifiers must be correctly biased if they are to function properly. As already discussed, the inputs of an operational amplifier are the base terminals of the transistors in a differential amplifier. Base currents must flow into these terminals for the transistors to operate. Consequently, the input terminals must be directly

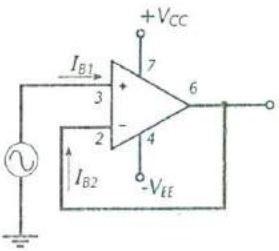


Figure 14-4
Op-amp circuit with one input terminal grounded via a signal generator, and the other input directly connected to the output.

connected to suitable *dc* bias voltage sources.

The most appropriate *dc* bias voltage level for op-amp inputs is approximately halfway between the + and - supply voltages. One of the two input terminals is usually connected in some way to the op-amp output to facilitate negative feedback. Where a +/- supply is used, the other input might be biased directly to ground via a signal source [see Fig. 14-4]. Base current I_{B1} flows into the op-amp noninverting input via the signal source, while I_{B2} flows from the output into the inverting input, as illustrated.

Figure 14-5 shows a situation in which one input is connected via resistor R_1 to ground, and the other is connected via R_2 to the op-amp output. Once again base current for the input stage transistors flows into both input terminals. R_1 and R_2 should have equal resistance values, so that voltage drops $I_{B1}R_1$ and $I_{B2}R_2$ are approximately equal. Any difference in these two voltage drops appears as an op-amp *dc* input voltage which may be amplified to produce a *dc* offset at the output.

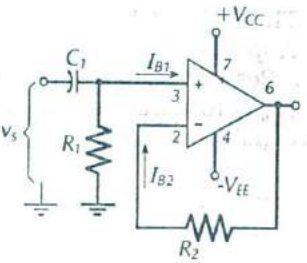


Figure 14-5
Op-amp circuit with one input grounded via resistor R_1, and the other input connected to the output via R_2.

If very small resistance values are selected for R_1 and R_2 in the circuit in Fig. 14-5, then a very small input resistance (R_1) would be offered to a capacitor-coupled signal source, [see Fig. 14-5]. On the other hand, if R_1 and R_2 are very large, the voltage drops $I_{B1}R_1$ and $I_{B2}R_2$ might be ridiculously large. An acceptable maximum voltage drop across these resistors must be very much smaller than the typical V_{BE} level for a forward-biased base-emitter junction.

Select, $V_{R1} \approx V_{BE}/10$

and, $R_{1(max)} = V_{R1}/I_{B(max)}$

or,
$$R_{1(max)} = \frac{V_{BE}}{10\ I_{B(max)}} \qquad (14\text{-}1)$$

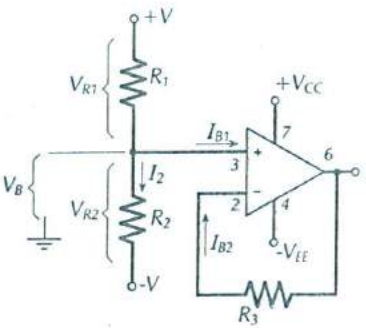


Figure 14-6
Op-amp circuit using a voltage divider bias circuit.

Figure 14-6 shows a voltage divider (R_1 and R_2) providing an input terminal bias level from the the supply voltages. The voltage divider current I_2 should be selected to be very much larger than the input bias current. This is to ensure that I_B has a negligible

is selected as,

$$I_{2(min)} = 100\, I_{B(max)} \qquad (14\text{-}2)$$

Then R_1 and R_2 are simply calculated as, V_{R1}/I_2 and V_{R2}/I_2 respectively.

Resistor R_3 in Fig. 14-6 should be selected approximately equal to $R_1 \| R_2$ to minimize any difference between $I_{B1}(R_1 \| R_2)$ and $I_{B1}R_3$ that could behave as a *dc* input voltage.

Example 14-1

Calculate the maximum resistance for R_1 and R_2 in Fig. 14-7(a) if a *741* op-amp is used. Also, determine suitable resistances for R_1, R_2, and R_3 in Fig. 14-7(b) to give $V_B = 0$ when the supply voltages are ±15 V.

Solution

For Fig. 14-7(a),

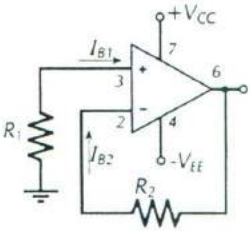
$$V_{BE} \approx 0.7 \text{ V} \quad \text{(for op-amps with } BJT \text{ input stages)}$$

From the 741 data sheet,

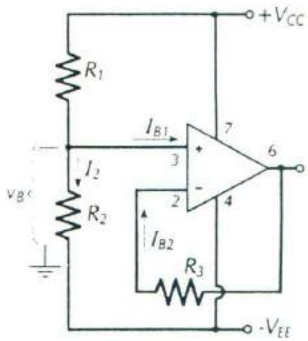
$$I_{B(max)} = 500 \text{ nA}$$

Eq. 14-1,
$$R_{1(max)} = \frac{V_{BE}}{10\, I_{B(max)}} = \frac{0.7 \text{ V}}{10 \times 500 \text{ nA}}$$

$$= 140 \text{ k}\Omega \text{ (use 120 k}\Omega \text{ standard value)}$$



(a) Grounded input circuit



(b) Voltage divider bias

Figure 14-7
Op-amp circuits for Ex. 14-1.

For Fig. 14-7(b),

Eq. 14-2,
$$I_2 = 100\, I_{B(max)} = 100 \times 500 \text{ nA}$$
$$= 50\, \mu\text{A}$$

$$V_{R1} = V_{R2} = 15 \text{ V}$$

$$R_1 = R_2 = \frac{V_{R1}}{I_2} = \frac{15 \text{ V}}{50\, \mu\text{A}}$$

$$= 300 \text{ k}\Omega \text{ (use 270 k}\Omega \text{ standard value)}$$

$$R_3 = R_1 \| R_2 = 270 \text{ k}\Omega \| 270 \text{ k}\Omega$$
$$= 135 \text{ k}\Omega \text{ (use 120 k}\Omega \text{ standard value)}$$

A single-polarity supply voltage can be used with an operational amplifier. For example, a 741 could use a +30 V (as illustrated in Fig. 14-8) instead of a ±15 V supply. Resistors R_1 and R_2 are normally selected to set $V_B = V_{CC}/2$.

The input offset voltage referred to in Section 14-1, and the resultant output offset, can be reduced or eliminated in the circuit shown in Fig. 14-6 by making one of the resistors adjustable. Similarly, if R_3 in Fig. 14-8 is a variable resistor, it could be

adjusted to reduce the op-amp output offset voltage. The process is termed *voltage offset nulling*.

Figure 14-9 shows another method of voltage offset nulling with a 741 op-amp. A 10 kΩ potentiometer is connected to the differential amplifier input stage via terminals 1 and 5, as illustrated. With the moving contact connected to $-V_{EE}$, the potentiometer can be adjusted to null the output offset voltage.

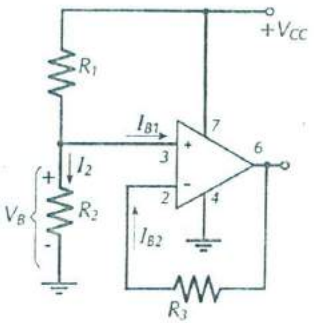


Figure 14-8
Op-amp circuit using a single-polarity supply.

Biasing BIFET Op-amps

The input bias current for a *BIFET* op-amp is typically 50 pA, which is very much smaller that that for a *Bioplar* op-amp. So, the bias resistor selection method already discussed would produce very high resistor values. This is undesirable because electric charges can accumulate at the *FET* gates, and thus make the bias levels unstable. Also, stray capacitance becomes more effective with high value bias resistors, possibly resulting in unwanted circuit oscillations. To combat these effects, the largest resistor in a *BIFET* op-amp bias circuit should normally not exceed 1 MΩ.

Example 14-2

Determine suitable resistor values for the type of circuit shown in Fig. 14-7(b) when a *BIFET* op-amp is used with a ±9 V supply.

Solution

Select, $R_1 = R_2 = 1\ \text{M}\Omega$

$R_3 = R_1 \| R_2 = 1\ \text{M}\Omega \| 1\ \text{M}\Omega$

$= 500\ \text{k}\Omega$ (use 470 kΩ standard value)

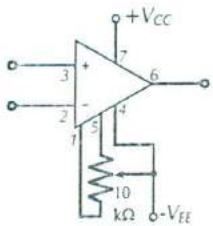


Figure 14-9
Output offset nulling can be accomplished in a 741 op-amp by the use of a 10 kΩ potentiometer connected to terminals 1 and 5.

Practise Problems

14-2.1 A *741* op-amp is used with a +24 V supply in the type of circuit shown in Fig. 14-8. Determine suitable bias resistor values.

14-2.2 Repeat Problem 14-2.1 to bias the input to +10 V.

14-3 Voltage Follower Circuits

Direct-Coupled Voltage Follower

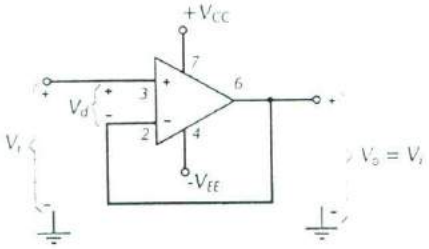
The *IC* operational amplifier can be employed for an infinite variety of applications. The very simplest application is the direct-coupled *voltage follower* shown in Fig. 14-10(a). The output terminal is connected directly to the inverting input terminal, the signal is applied to the noninverting input, and the load is directly-coupled to the output.

Figure 14-10(b) shows the basic op-amp circuit connected as a voltage follower. With the differential amplifier input stage, V_2 (which equals V_o) must equal V_i. When V_2 is higher or lower than

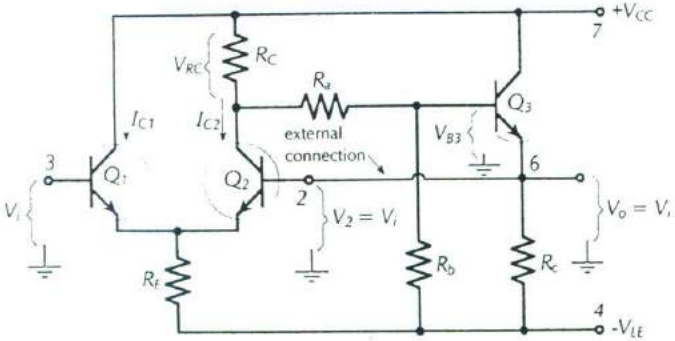
V_i, the voltage difference is amplified to move the output back to equality with the input. Suppose V_o was slightly higher than V_i. The voltage at Q_2 base (terminal 2) would be higher than that at Q_1 base (terminal 3), therefore I_{C2} would be increased above its normal level. This would cause an increase in the voltage drop across R_C, thus reducing V_{B3} and driving V_o back to equality with V_i. Similarly, when V_o is lower than V_i, Q_2 base voltage is lower than that at Q_1 base, I_{C2} is reduced, thus reducing V_{RC}, increasing V_{B3}, and driving V_o back up toward V_i.

When the input voltage (at terminal 3) is increased or decreased, the feedback effect causes the output to almost perfectly follow the input. The actual difference between the input and output voltage is easily calculated from the output voltage level and the op-amp open-loop voltage gain.

Like an emitter follower, the voltage follower has a high input impedance, a low output impedance, and a voltage gain of 1. The voltage follower performance is superior to that of the emitter follower. As demonstrated in Example 14-3, the typical difference between input and output voltage with a voltage follower is only 5 μV when the input amplitude is 1 V. With an emitter follower, there is a 0.7 V *dc* voltage difference between input and output. The voltage follower also has a much higher input impedance and a much lower output impedance than the emitter follower. The actual values of Z_{if} and Z_o can be calculated from the negative feedback equations derived in Chapter 13.



(a) Voltage follower circuit



(b) Basic op-amp circuit connected as a voltage follower

Figure 14-10
In a voltage follower circuit, the output terminal is directly connected to the inverting input terminal. As the input voltage changes, the output follows the input to keep the inverting input terminal voltage equal to the noninverting terminal voltage.

Example 14-3

Calculate the typical difference between the input and output voltage for a voltage follower using a 741 op-amp with a 1 V input, as in Fig. 14-11. Also, determine typical Z_{in} and Z_{out} values.

Solution

From Appendix 1-13, typical parameters are:

$$A_v = 200\,000,\ r_i = 2\ \text{M}\Omega,\ r_o = 75\Omega$$

$$V_d = V_o - V_i$$

$$V_d = \frac{V_o}{A_v} = \frac{1\ \text{V}}{200\,000}$$

$$= 5\ \mu\text{V}$$

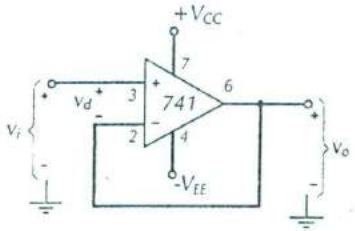


Figure 14-11
Voltage follower circuit for Example 14-3.

from Eq. 13-4, $Z_i = (1 + A_v B)r_i = [1 + (200\,000 \times 1)] \times 2\ \text{M}\Omega$

$$= 400\,000\ \text{M}\Omega$$

from Eq. 13-6, $Z_o = \dfrac{r_o}{1 + A_v B} = \dfrac{75\ \Omega}{1 + (200\,000 \times 1)}$

$$= 0.375 \times 10^{-3}\ \Omega$$

Capacitor-Coupled Voltage Follower

When a voltage follower is to have capacitor-coupled input and output terminals, the noninverting input must be grounded via a resistor, [see (R_1) Fig. 14-12]. As discussed, the resistor is required for passing bias current to the noninverting input terminal. It also offers an input resistance to the signal source, rather than a short-circuit. Because the load is capacitor-coupled, the *dc* output offset voltage might seem to be unimportant. However, the *dc* offset voltage at the op-amp output terminal can limit the amplitude of the output voltage. So, a resistor (R_2) equal to R_1 should be included in series with the inverting input terminal to equalize the $I_B R_B$ voltage drops and thus minimize output offset voltage, as already discussed.

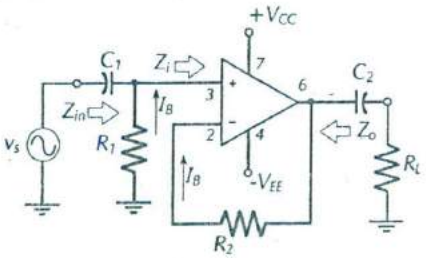


Figure 14-12
A capacitor-coupled voltage follower must have the op-amp noninverting terminal grounded via a resistor to provide a path for input bias current.

Design of the capacitor-coupled circuit in Fig. 14-12 involves calculation of R_1, C_1, and C_2. The circuit input impedance is $R_1 \| Z_i$.

however, Z_i is always much larger than R_1. So, the circuit input impedance is simply taken as.

$$Z_{in} = R_1 \qquad (14\text{-}3)$$

Normally, The load resistance R_L is much smaller R_1, and consequently, the smallest capacitor values are calculated when C_2 is selected to set f_1. Therefore.

$$X_{C2} = (Z_o + R_L) \text{ at } f_1 \qquad (14\text{-}4)$$

Capacitor C_1 should then be calculated from. $X_{C1} = (Z_{in} + r_s)/10$ at f_1, so that it has no significant effect on the circuit lower cutoff frequency.

$$X_{C1} = (R_1 + r_s)/10 \text{ at } f_1 \qquad (14\text{-}5)$$

Coupling capacitor equations are explained in Section 12-1.

Example 14-4

Design a capacitor-coupled voltage follower using a 741 op-amp. The circuit lower cutoff frequency is to be 70 Hz, the load resistance is 4 kΩ, and the signal source resistance is much smaller than R_1.

Solution

From the 741 data sheet,

$$I_{B(max)} = 500 \text{ nA}$$

Eq. 14-1, $$R_{1(max)} = \frac{V_{BE}}{10\, I_{B(max)}} = \frac{0.7 \text{ V}}{10 \times 500 \text{ nA}}$$

$$= 140 \text{ k}\Omega \text{ (use 120 k}\Omega \text{ standard value)}$$

From Eq. 14-4, $$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 70 \text{ Hz} \times 4 \text{ k}\Omega}$$

$$\approx 0.56\ \mu\text{F (standard value)}$$

From Eq. 14-5, $$C_1 = \frac{1}{2\pi f_1 R_1/10} = \frac{1}{2\pi \times 70 \text{ Hz} \times 120 \text{ k}\Omega/10}$$

$$\approx 0.19\ \mu\text{F (use 0.2 } \mu\text{F standard value)}$$

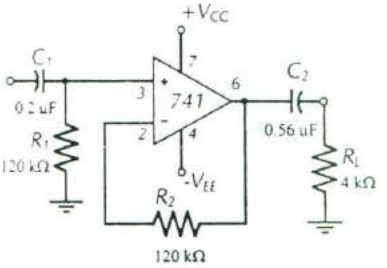


Figure 14-13
Capacitor-coupled voltage follower for Example 14-4.

Practise Problems

14-3.1 A capacitor-coupled voltage follower with Z_{in} = 22 kΩ and R_L = 10 kΩ is to have f_1 = 50 Hz. Determine suitable capacitor values.

14-3.2 Determine coupling capacitor values for the circuit in part (b) of Ex. 14-1, if r_s = 600 Ω, R_L = 8.2 kΩ, and f_1 = 20 Hz.

14-3.3 Calculate the maximum *dc* offset voltage that might be produced at the output of the circuit designed in part (a) of Ex. 14-1 when R_2 is replaced with a short circuit.

14-4 Noninverting Amplifiers

Direct-Coupled Noninverting Amplifier

The noninverting amplifier circuit in Fig. 14-14 behaves similarly to a voltage follower circuit with one major difference. Instead of all of the output voltage being fed directly back to the inverting input terminal (as in a voltage follower), only a portion of V_o is fed back. The output voltage is divided by resistors R_2 and R_3, and the voltage across R_3 is applied to the inverting input terminal. As in the case of the voltage follower, the output voltage changes as necessary to keep the inverting input terminal voltage equal to that at the noninverting input. Thus, the voltage V_{R3} always equals V_i, and the output voltage is then determined by the resistances of R_2 and R_3.

Because the signal voltage is applied to the op-amp noninverting input terminal, the output always has the same polarity as the input. A positive-going input produces a positive-going output, and vice versa. Thus, the input is not inverted (at the output), and the circuit is identified as a *noninverting amplifier.*

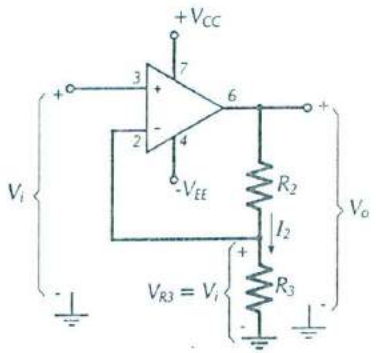


Figure 14-14
Op-amp noninverting amplifier circuit. The signal is applied to the noninverting input terminal. The circuit voltage gain is,
$A_{CL} = (R_2 + R_3)/R_3$

The voltage divider current (I_2) is always selected to be very much larger than the operational amplifier input bias current, and

$$V_{R3} = V_i = I_2 R_3 \qquad (14\text{-}6)$$

Also, in Fig. 14-14 it is seen that,

$$I_2 = \frac{V_o}{R_2 + R_3} \qquad (14\text{-}7)$$

The circuit voltage gain is,

$$A_{CL} = \frac{V_o}{V_i} = \frac{I_2 (R_2 + R_3)}{I_2 R_3}$$

or,
$$A_{CL} = \frac{R_2 + R_3}{R_3} \qquad \textbf{(14-8)}$$

Figure 14-15 shows a noninverting amplifier circuit with a resistor (R_1) connected in series with the noninverting input terminal. As in the case of other op-amp circuits, this is done to equalize the resistor voltage drops produced by input bias current. In this case, R_1 is selected to be approximately equal to the resistance seen looking out of the inverting input terminal. Thus,

$$R_1 = R_2 \| R_3 \qquad \textbf{(14-9)}$$

The input and output impedances for a noninverting amplifier are easily determined from the negative feedback equations in Chapter 13.

Design of a noninverting amplifier mostly involves determining suitable voltage divider resistors (R_2 and R_3). So, as discussed in Section 14-2, design commences with selection of the voltage divider current to be much larger than the op-amp input bias current.

Example 14-5

Design a direct-coupled noninverting amplifier (as in Fig. 14-15) to use a 741 op-amp. The output voltage is to be 2 V when the input is 50 mV.

Solution

From the 741 data sheet,

$$I_{B(max)} = 500 \text{ nA}$$

From Eq. 14-2, $I_{2(min)} = 100\, I_{B(max)} = 100 \times 500 \text{ nA}$
$= 50\ \mu\text{A}$

From Eq. 14-6, $R_3 = \dfrac{V_i}{I_2} = \dfrac{50 \text{ mV}}{50\ \mu\text{A}}$
$= 1 \text{ k}\Omega$ (standard resistor value)

From Eq. 14-7, $R_2 + R_3 = \dfrac{V_o}{I_2} = \dfrac{2 \text{ V}}{50\ \mu\text{A}}$
$= 40 \text{ k}\Omega$

$R_2 = (R_2 + R_3) - R_3 = 40 \text{ k}\Omega - 1 \text{ k}\Omega$
$= 39 \text{ k}\Omega$ (standard value)

From Eq. 14-9, $R_1 = R_2 \| R_3 = 39 \text{ k}\Omega \| 1 \text{ k}\Omega$
$\approx 1 \text{ k}\Omega$ (use 1 kΩ)

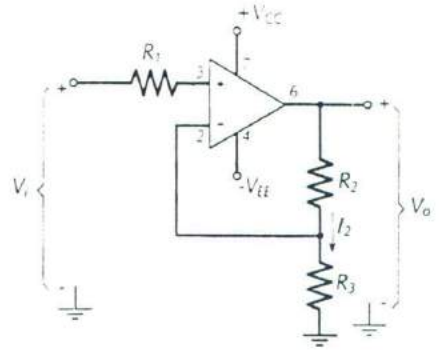


Figure 14-15
Noninverting amplifier circuit with a resistor R_1 in series with the input. R_1 is selected to be approximately equal to $R_2 \| R_3$.

Example 14-6

Calculate typical input and output impedances for the noninverting amplifier designed in Example 14-5.

Solution

From Appendix 1-13, typical parameters are:

$$A_v = 200\,000,\ r_i = 2\ \text{M}\Omega,\ r_o = 75\Omega$$

Also,
$$B = \frac{R_3}{R_2 + R_3} = \frac{1\ \text{k}\Omega}{39\ \text{k}\Omega + 1\ \text{k}\Omega}$$
$$= \frac{1}{40}$$

from Eq. 13-4,
$$Z_i = (1 + A_v B)\, r_i = [1 + \frac{200\,000}{40}] \times 2\ \text{M}\Omega$$
$$\approx 10\,000\ \text{M}\Omega$$

from Eq. 13-6,
$$Z_o = \frac{r_o}{1 + A_v B} = \frac{75\ \Omega}{1 + (200\,000/40)}$$
$$\approx 0.015\ \Omega$$

Capacitor-Coupled Noninverting Amplifier

When a noninverting amplifier is to have a signal capacitor-coupled to its input, the op-amp noninverting input terminal must be grounded via a resistor to provide a path for the input bias current. This is illustrated in Fig. 14-16, where R_1 allows for the passage of I_{B1}. As in the case of the capacitor-coupled voltage follower, the input resistance is essentially equal to R_1 for the capacitor-coupled noninverting amplifier.

Resistors R_1, R_2, and R_3 in the capacitor-coupled circuit are determined exactly as for a direct-coupled noninverting amplifier. The capacitor values are calculated in the same way as for a capacitor-coupled voltage follower, using Eqs. 14-4 and 14-5.

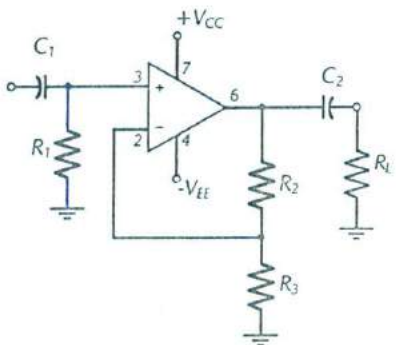


Figure 14-16
A capacitor-coupled noninverting amplifier circuit must have the noninverting input terminal grounded via a resistor to provide a path for the input bias current.

Example 14-7

Calculate the voltage gain and lower cutoff frequency for the capacitor-coupled noninverting amplifier circuit in Fig. 14-17.

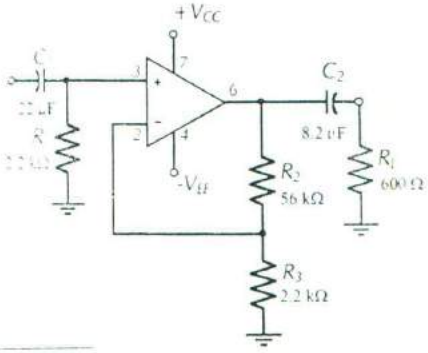


Figure 14-17
Capacitor-coupled noninverting amplifier circuit for Ex. 14-7.

Solution

Eq. 14-8, $$A_{CL} = \frac{R_F + R_1}{R_1} = \frac{56\ \text{k}\Omega + 2.2\ \text{k}\Omega}{2.2\ \text{k}\Omega}$$

$$= 26.5$$

From Eq. 14-4, $$f_1 = \frac{1}{2\pi C_2 R_L} = \frac{1}{2\pi \times 8.2\ \mu\text{F} \times 600\ \Omega}$$

$$= 32.3\ \text{Hz}$$

Practise Problems

14-4.1 A direct-coupled noninverting amplifier using a 741 op-amp is to have a 100 mV input voltage amplitude and a voltage gain of 40. Select suitable resistor values.

14-4.2 Design a capacitor-coupled noninverting amplifier using a 741 op-amp to have a ±5 V output amplitude when the input is ±250 mV. The load resistance is $R_L = 820\ \Omega$, and the lower cutoff frequency is to be $f_1 = 20$ Hz.

14-4.3 Redesign the circuit in Problem 14-4.1 to use a *BIFET* op-amp.

14-5 Inverting Amplifiers

Direct-Coupled Inverting Amplifier

The circuit in Fig. 14-18 is termed an *inverting amplifier* because, with V_i applied via R_1 to the inverting input terminal, the output goes negative when the input goes positive, and vice versa. Note that the noninverting input terminal is grounded via resistor R_3. With the noninverting terminal grounded, the voltage at the op-amp inverting input terminal remains close to ground. Any increase or decrease in the (very small) difference voltage between the two input terminals is amplified by the op-amp open-loop gain and fed back via R_2 and R_1 to correct the change. Because the inverting input terminal is not grounded but remains close to ground, the inverting input terminal in this application is termed a *virtual ground* or *virtual earth*.

The circuit input current in Fig. 14-18 can be calculated as,

$$I_1 = \frac{V_{R1}}{R_1}$$

The input voltage is applied to one end of R_1, and the other end of R_1 is at ground level. Consequently,

$$V_{R1} = V_i$$

and,
$$I_1 = \frac{V_i}{R_1} \qquad \textbf{(14-10)}$$

I_1 is always selected to be very much larger than the op-amp input bias current (I_B). Consequently, virtually all of I_1 flows through resistor R_2, (see Fig.14-18), and the voltage drop across R_2 is,

$$V_{R2} = I_1 R_2$$

The left side of R_2 is connected to the op-amp inverting input terminal, which, as discussed, is always at ground level. This means that the right side of R_2 (the output terminal) is V_{R2} below ground. So,

$$\mathbf{V_o = -I_1 R_2} \qquad \textbf{(14-11)}$$

From Eq. 14-10, $V_i = I_1 R_1$

So, the circuit voltage gain is,

$$A_{CL} = \frac{V_o}{V_i} = \frac{-I_1 R_2}{I_1 R_1}$$

or,
$$\mathbf{A_{CL} = \frac{-R_2}{R_1}} \qquad \textbf{(14-12)}$$

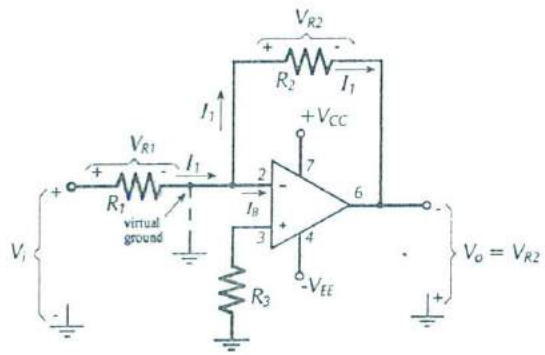


Figure 14-18
Op-amp inverting amplifier. The signal voltage is applied via resistor R_1 to the inverting input terminal. The circuit voltage gain is $A_{CL} = -R_2/R_1$.

If the input of the inverting amplifier is grounded, the circuit is seen to be exactly the same as noninverting amplifier with R_3 as the input resistor and zero input voltage. Thus, negative feedback occurs (as in a noninverting amplifier) to maintain the op-amp inverting input terminal at the same voltage level as the noninverting input terminal.

The output impedance of an inverting amplifier is calculated in exactly the same way as for a noninverting amplifier, (using Eq. 13-6). Like the case of the noninverting amplifier, the output impedance is very low for an inverting amplifier.

The input impedance of an inverting amplifier is easily determined by recalling that the right side of R_1 (in Fig. 14-18) is always at ground level, and that the signal is applied to the left side of R_1. Therefore,

$$\boldsymbol{Z_i = R_1} \qquad \textbf{(14-13)}$$

Design of an inverting amplifier is very simple. Voltage divider current I_1 is selected very much larger than the op-amp input bias current. Resistors R_1 and R_2 are calculated from Eqs. 14-10 and 14-11, or 14-12, and R_3 is selected approximately equal to $R_1 \| R_2$.

Example 14-8

Design a direct-coupled inverting amplifier, as in Fig. 14-19, to use a 741 op-amp. The input voltage amplitude is 20 mV and the voltage gain is to be 144.

Solution

For the 741, $I_{B(max)} = 500$ nA

select $I_{1(min)} = 100\, I_{B(max)} = 100 \times 500$ nA
$= 50\ \mu$A

From Eq. 14-10, $R_1 = \dfrac{V_i}{I_1} = \dfrac{20\text{ mV}}{50\ \mu\text{A}}$
$= 400\ \Omega$ (use 390 Ω standard value)

From Eq. 14-12, $R_2 = A_{v_f} R_1 = 144 \times 390\ \Omega$
$= 56.2$ kΩ (use 56 kΩ standard value)

$R_3 = R_1 \| R_2 = 390\ \Omega \| 56$ kΩ
$\approx 390\ \Omega$ (use 390 Ω)

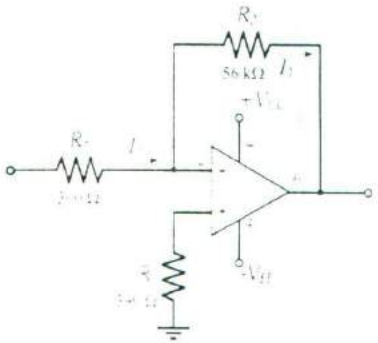


Figure 14-19
Inverting amplifier for Ex. 14-8.

Capacitor-Coupled Inverting Amplifier

A capacitor-coupled inverting amplifier circuit is shown in Fig. 14-20. In this case, the bias current to the op-amp inverting input terminal flows (from the output) via resistor R_2, so that the input coupling capacitor does not interrupt the input bias current. A voltage drop $I_B R_2$ is produced at the inverting input by the bias current flow, and this must be equalized by the $I_B R_3$ voltage drop at the noninverting input. Therefore, for the capacitor-coupled noninverting circuit,

$$\boldsymbol{R_3 = R_2} \qquad \textbf{(14-14)}$$

Apart from the selection of R_3, the circuit is designed exactly as the direct-coupled circuit, and the capacitor values are calculated in the same way as for a capacitor-coupled noninverting amplifier.

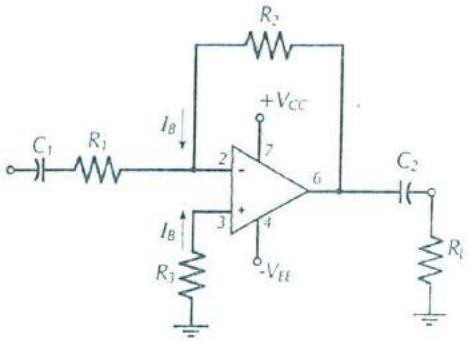


Figure 14-20
Capacitor-coupled inverting amplifier circuit. Note that the flow of bias current is not interrupted by capacitor C_1.

Practise Problems

14-5.1 A direct-coupled inverting amplifier using a 741 op-amp is to have a 300 mV input voltage amplitude and a voltage gain of 15. Select suitable resistor values.

14-5.2 The circuit in Problem 14-5.1 is to have a 1 kΩ capacitor-coupled load and a 600 Ω capacitor coupled signal source. Determine suitable capacitor values for a 20 Hz lower cutoff frequency

14-5.3 Redesign the circuit in Problem 14-5.1 to use a *BIFET* op-amp.

14-6 Summing Amplifier

The *summing amplifier* circuit in Fig. 14-21 is simply a direct-coupled inverting amplifier with two inputs applied to two resistors (R_1 and R_2). With two input voltages (V_{i1} and V_{i2}) there are two input currents (I_1 and I_2). Also, because the op-amp inverting input terminal behaves as a virtual ground (as for an inverting amplifier), the input currents are,

$$I_1 = \frac{V_{i1}}{R_1} \qquad I_2 = \frac{V_{i2}}{R_2}$$

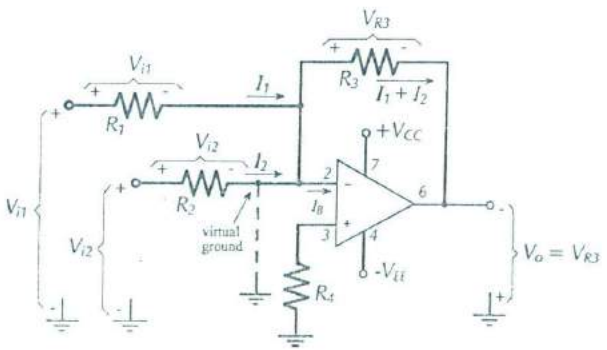


Figure 14-21
An op-amp summing amplifier amplifies the sum of two, or more, input voltages.

All of I_1 and I_2 flows through resistor R_3, giving

$$V_o = -(I_1 + I_2) R_3$$

or,

$$V_o = \left[\frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2}\right] R_3$$

With $R_1 = R_2$,

$$V_o = \frac{-R_3}{R_1}(V_{i1} + V_{i2}) \qquad \textbf{(14-15)}$$

When $R_3 = R_1 = R_2$, the output voltage is the direct (inverted) sum of the two inputs. When R_3 is greater than R_1 and R_2, the output is an amplified version of the sum of the inputs.

A summing amplifier is not limited to two inputs. There can be almost any number of inputs, and the output remains the sum of the inputs. Summing amplifiers are designed in the same way as ordinary inverting amplifiers.

Example 14-9

Design a three-input summing amplifier, as in Fig. 14-22, to use a *BIFET* op-amp and to have a voltage gain of 3. Calculate the resistor currents and the output voltage when all three inputs are 1 V.

Solution

Select, $R_4 = 1\ \text{M}\Omega$

From Eq. 14-12, $R_1 = R_2 = R_3 = \dfrac{R_4}{A_{CL}} = \dfrac{1\ \text{M}\Omega}{3}$

$= 333\ \text{k}\Omega$ (use 330 kΩ standard value)

$R_5 = R_1 \| R_2 \| R_3 \| R_4 = 330\ \text{k}\Omega \| 330\ \text{k}\Omega \| 330\ \text{k}\Omega \| 1\ \text{M}\Omega$

$= 99\ \text{k}\Omega$ (use 100 kΩ standard value)

$$I_1 = I_2 = I_3 = \frac{V_i}{R_1} = \frac{1\ \text{V}}{330\ \text{k}\Omega}$$

$= 3.03\ \mu\text{A}$

$I_4 = I_1 + I_2 + I_3 = 3.03\ \mu\text{A} + 3.03\ \mu\text{A} + 3.03\ \mu\text{A}$

$= 9.09\ \mu\text{A}$

$V_o = -I_4 R_4 = -9.09\ \mu\text{A} \times 1\ \text{M}\Omega$

$= -9.09\ \text{V}$

or, from Eq 14-15,

$$V_o = \frac{-R_4}{R_1}(V_{i2} + V_{i2} + V_{i3}) = \frac{-1\ \text{M}\Omega}{330\ \text{k}\Omega}(1\ \text{V} + 1\ \text{V} + 1\text{V})$$

$= -9.09\ \text{V}$

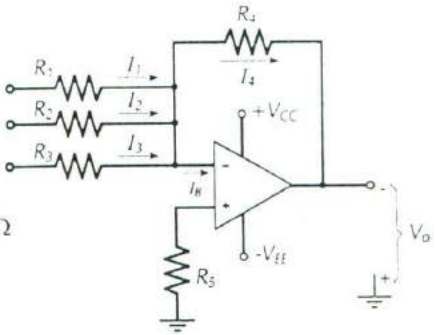


Figure 14-22
Three-input summing amplifier for Example 14-9.

Practise Problems

14-6.1 A two-input summing amplifier is to be designed to produce a 5 V output from two 0.25 V inputs. Determine suitable resistor values for a circuit using a *741* op-amp.

14-6.2 If the circuit designed in Example 14-9 has 0.75 V, 1.5 V, and 1.25 V inputs, determine V_o, I_1, I_2, I_3, and I_4.

14-7 Difference Amplifier

Circuit Operation

A *difference amplifier* amplifies the difference between two inputs. The circuit shown in Fig. 14-23 is a combination of inverting and noninverting amplifiers. Resistors R_1, R_2, and the op-amp constitutes an inverting amplifier for a voltage (V_{i1}) applied to R_1. The same components (R_1, R_2, and the op-amp) also function as a noninverting amplifier for a voltage (V_{R4}) at the noninverting input terminal. It is seen that V_{R4} is derived from input voltage V_{i2} by the voltage divider R_3 and R_4. To understand the circuit operation, consider the output produced by each input voltage when the other input is zero:

with $V_{i2} = 0$, $$V_{o1} = \frac{-R_2}{R_1} \times V_{i1}$$

with $V_{i1} = 0$, $$V_{o2} = \frac{R_1 + R_2}{R_1} \times V_{R4}$$

and, $$V_{R4} = \frac{R_4}{R_3 + R_4} \times V_{i2}$$

so, $$V_{o2} = \frac{R_1 + R_2}{R_1} \times \frac{R_4}{R_3 + R_4} \times V_{i2}$$

with $R_3 = R_1$, and $R_4 = R_2$,

$$V_{o2} = \frac{R_2}{R_1} \times V_{i2}$$

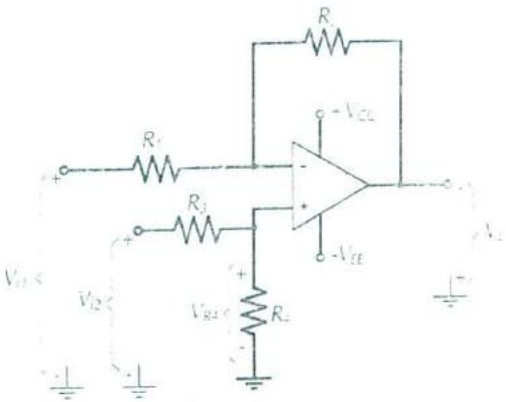


Figure 14-23
An op-amp difference amplifier amplifies the difference between two input voltages.

When both inputs are present,

$$V_o = V_{o2} + V_{o1}$$
$$= \frac{R_2}{R_1} V_{i2} + \frac{-R_2}{R_1} V_{i1}$$

giving, $$\boldsymbol{V_o = \frac{R_2}{R_1} (V_{i2} - V_{i1})} \qquad \textbf{(14-16)}$$

When $R_2 = R_1$, the output voltage (as calculated by Eq. 14-16) is

the direct difference between the two inputs. With R_2 greater than R_1, the output becomes an amplifier version of $(V_{i2} - V_{i1})$.

Input resistances

Consider the input portion of the difference amplifier circuit reproduced in Fig. 14-24. The resistance at input *terminal 1* is the same as the input impedance for an inverting amplifier: $Z_{i1} = R_1$. The input resistance at the op-amp noninverting input terminal, is very high (as in the case of a noninverting amplifier), and this is in parallel with resistor R_4. So, the input impedance at *terminal 2* in Fig. 14-24 is $Z_{i2} = R_3 + R_4$.

Equation 14-16 was derived by assuming that $R_3 = R_1$, and $R_4 = R_2$. It can be shown that the same result is obtained when the *ratio* R_4/R_3 equals R_2/R_1, so that the actual resistor values do not have to be equal. For equal resistances at the two input terminals

select, $$\boldsymbol{R_3 + R_4 = R_1} \qquad \textbf{(14-17)}$$

Then, calculate the resistances of R_3 and R_4 from,

$$\frac{\boldsymbol{R_4}}{\boldsymbol{R_3}} = \frac{\boldsymbol{R_2}}{\boldsymbol{R_1}} \qquad \textbf{(14-18)}$$

A simple rule-of-thumb can be used for determining suitable resistance values for R_3 and R_4 when the two input resistances do not have to be exactly equal. Select, $R_4 = R_2/A_{CL}$; which always makes $R_4 = R_1$. Then, calculate R_3 as, $R_3 = R_1/A_{CL}$.

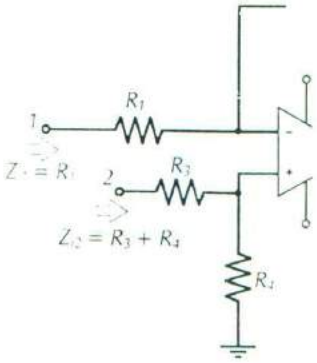


Figure 14-24
Difference amplifier circuit input impedances.

Example 14-10

A difference amplifier is to be designed to amplify the difference between two voltages by a factor of 10. The inputs each approximately equal 1 V. Determine suitable resistor values for a circuit using a 741 op-amp.

Solution

Select, $I_1 \approx 100\, I_B = 100 \times 500\ \text{nA}$

$= 50\ \mu\text{A}$

$$R_1 = \frac{V_{i1}}{I_1} = \frac{1\ \text{V}}{50\ \mu\text{A}}$$

$= 20\ \text{k}\Omega$ (use 18 kΩ standard value)

$R_2 = A_{CL} R_1 = 10 \times 18\ \text{k}\Omega$

$= 180\ \text{k}\Omega$ (standard values)

$R_4 = R_1 = 18\ \text{k}\Omega$

$$R_3 = \frac{R_1}{A_{CL}} = \frac{18\ \text{k}\Omega}{10}$$

$= 1.8\ \text{k}\Omega$ (standard value)

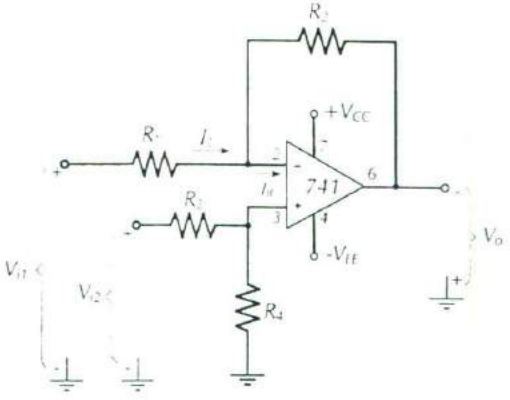


Figure 14-25
Difference amplifier circuit for Ex. 14-10.

Common-Mode Voltages

A common-mode input voltage is a signal voltage (*dc* or *ac*) applied to both input terminals at the same time. This is illustrated in Fig. 14-26, where V_{i1}, V_{i2}, and the common-mode voltage (V_n) are all represented as inputs from *dc* sources. As shown, the input voltages at *terminals 1* and *2* are changed from V_{i1} and V_{i2} to (V_n + V_{i1}) and (V_n + V_{i2}).

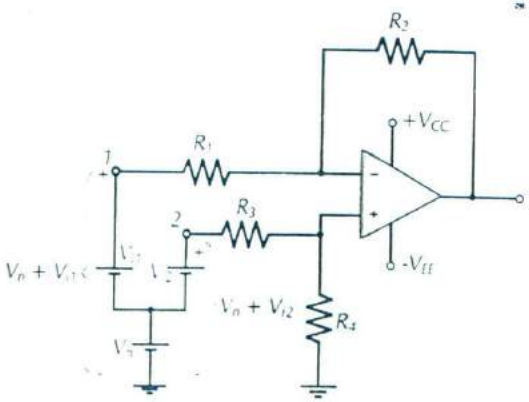


Figure 14-26
Common-mode input voltage applied to a difference amplifier.

Equation 14-16 shows that the output voltage is the amplified difference between the two input voltages. So,

$$V_o = \frac{R_2}{R_1}[(V_{i2} + V_n) - (V_{i1} + V_n)]$$

$$= \frac{R_2}{R_1}(V_{i2} - V_{i1})$$

This shows that the common-mode input is completely cancelled. However, recall that the gain equation depends upon the resistor ratios (R_4/R_3 and R_2/R_1) being equal. If the ratios are not exactly equal, one input will experience a larger amplification than the other. Also, the common-mode voltage at one input terminal will be amplified by a larger amount than that applied to the other input terminal. In this case, common-mode inputs will not be completely cancelled.

Because it is difficult to perfectly match resistor ratios (especially for standard-value components), some common-mode output voltage is almost certain to be produced where a common-mode input exists. Figure 14-27 shows a circuit modification for minimizing common-mode outputs from a difference amplifier. Resistor R_4 is made up of a fixed-value resistor and a small-value adjustable resistor connected in series. This provides adjustment of the ratio R_4/R_3 to match R_2/R_1, so that common-mode outputs can be nulled to zero.

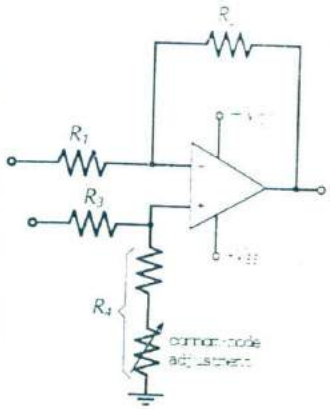


Figure 14-27
Common-mode outputs may be nulled by adjustment of R_4.

ıctise Problems

-7.1 If the circuit designed in Example 14-10 has $V_{i1} = 0.75$ V and $V_{i2} = 1.5$ V, determine V_o, I_{R1}, I_{R2}, I_{R3}, and V_{R4}.

14-7.2 A 500 Ω resistor is connected in series with R_4 in the circuit designed in Ex. 14-10. Calculate the common-mode gain.

14-7.3 A difference amplifier is to be designed to produce a 3 V output when the inputs are 1.5 V and 2 V. Determine suitable resistor values for a circuit using a *BIFET* op-amp.

14-8 Instrumentation Amplifier

Circuit Operation

At first glance, the *instrumentation amplifier* circuit in Fig. 14-28 looks complex, but when considered section by section it is found to be quite simple. First, note that the second stage (consisting of op-amp A_3 and resistors R_4 through R_7) is a difference amplifier that operates exactly as described in Section 14-7. Next, look at A_1 and resistors R_1 and R_2: this is a noninverting amplifier. Similarly, A_2 combined with resistors R_2 and R_3 constitutes another noninverting amplifier. Because the first stage circuits share a single resistor, their operation is slightly different from the usual noninverting amplifier operation.

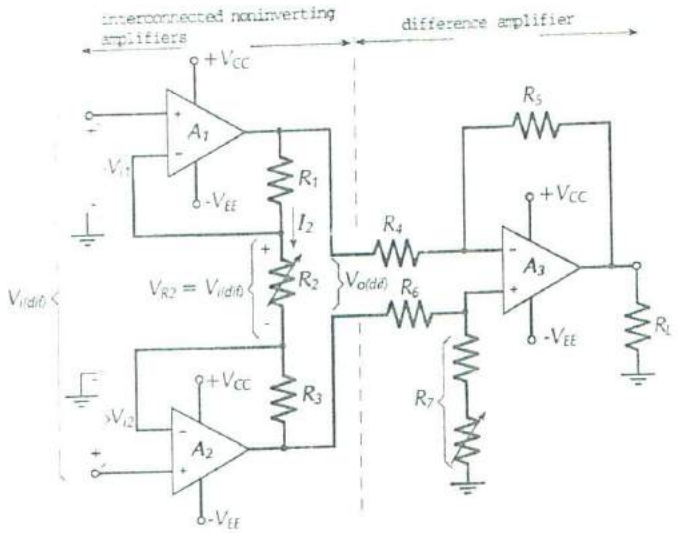


Figure 14-28
An instrumentation amplifier has two interconnected noninverting amplifiers as the first stage, and a difference amplifier as the second stage.

The first stage accepts a *differential input voltage* ($V_{i(diff)}$), and produces a *differential output voltage* ($V_{o(diff)}$). The differential input could be the difference between two grounded inputs (V_{i1} and V_{i2}), as illustrated. But, is often a differential ungrounded input voltage derived, for example, from two voltage monitoring electrodes

connected to a human body for medical purposes. In this case, there is often a large common mode input voltage, which can be shown to pass to the output of the first stage without amplification.

The difference amplifier second stage accepts $V_{o(dif)}$ from the first stage as an input, and produces an output to a grounded load, as shown on the circuit diagram. As explained in Section 14-7, the difference amplifier tends to reject common-mode voltages, and the circuit can also have an adjustment for reducing common-mode outputs to zero.

The instrumentation amplifier is now seen to be a circuit with two high-impedance input terminals, and one low-impedance output. The differential input voltage is amplified and converted to a single-ended output, and common-mode inputs are attenuated.

Voltage Gain

Recall that, with a noninverting amplifier, the feedback voltage to the op-amp inverting input terminal always equals the input voltage to the noninverting input terminal. Therefore, the voltage at the R_1R_2 junction equals V_{i1}, and that at the R_2R_3 junction equals V_{i2}. Consequently, the voltage drop across R_3 equals the difference between the two input voltages, which also means that V_{R2} equals the differential input voltage ($V_{i(dif)}$). The current through R_2 can now be calculated as,

$$I_2 = \frac{V_{i(dif)}}{R_2}$$

The voltage drop across R_1, R_2, and R_3 is the differential output voltage of the first stage ($V_{o(dif)}$).

$$V_{o(dif)} = I_2 (R_1 + R_2 + R_3)$$

$$= \frac{V_{i(dif)}}{R_2} (R_1 + R_2 + R_3)$$

The (closed-loop) voltage gain of the *differential input-differential output* first stage is,

$$A_{CL1} = \frac{V_{o(dif)}}{V_{i(dif)}} = \frac{R_1 + R_2 + R_3}{R_2}$$

Normally, R_1 and R_3 are always equal. So, the first stage gain can be written as,

$$\mathbf{A_{CL1} = \frac{2R_1 + R_2}{R_2}} \qquad \textbf{(14-19)}$$

From Eq. 14-16, the second-stage gain is,

$$A_{CL2} = \frac{R_5}{R_4}$$

The overall voltage gain is,

$$A_{CL} = A_{CL1} \times A_{CL2}$$

The second stage is often designed for a gain of one, so that the overall voltage gain can be calculated from Eq. 14-19. Note that, as shown in Fig. 14-28, R_2 can be a variable resistor for adjustment of the circuit overall voltage gain.

Example 14-11

Calculate the overall voltage gain for the instrumentation amplifier in Fig. 14-29. Also, determine the current and voltage levels throughout the circuit when a +1 V common-mode input (V_{cm}) is present along with the ±10 mV signals.

Solution

From Eqs. 14-16 and 14-19,

$$A_{CL} = \frac{2R_1 + R_2}{R_2} \times \frac{R_5}{R_4}$$

$$= \frac{(2 \times 33\ \text{k}\Omega) + 300\ \Omega}{300\ \Omega} \times \frac{15\ \text{k}\Omega}{15\ \text{k}\Omega}$$

$$= 221$$

at the junction of R_1 and R_2,

$$V_b = V_{i1} + V_{cm} = 10\ \text{mV} + 1\ \text{V}$$
$$= +1.01\ \text{V}$$

at the junction of R_2 and R_3,

$$V_c = V_{i2} + V_{cm} = -10\ \text{mV} + 1\ \text{V}$$
$$= +0.99\ \text{V}$$

current through R_2,

$$I_2 = \frac{V_b - V_c}{R_2} = \frac{1.01\ \text{V} - 0.99\ \text{V}}{300\ \Omega}$$
$$= 66.67\ \mu\text{A}$$

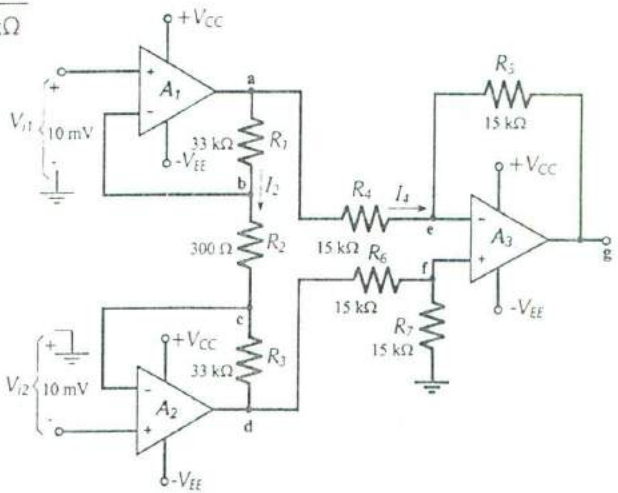


Figure 14-29
Instrumentation amplifier circuit for Ex.14-11.

at the output of A_1,

$$V_a = V_b + (I_2 \times R_1) = 1.01\ \text{V} + (66.67\ \mu\text{A} \times 33\ \text{k}\Omega)$$
$$= +3.21\ \text{V}$$

at the output of A_2,

$$V_d = V_c - (I_2 \times R_3) = 0.99\ \text{V} - (66.67\ \mu\text{A} \times 33\ \text{k}\Omega)$$
$$= -1.21\ \text{V}$$

at the junction of R_6 and R_7,

$$V_f = V_d \times \frac{R_-}{R_6 + R_-} = -1.21\ \text{V} \times \frac{15\ \text{k}\Omega}{15\ \text{k}\Omega + 15\ \text{k}\Omega}$$

$$= -0.605\ \text{V}$$

at the junction of R_4 and R_5,

$$V_e = V_f = -0.605\ \text{V}$$

current through R_4,

$$I_4 = \frac{V_a - V_e}{R_2} = \frac{3.21\ \text{V} - (-0.605\ \text{V})}{15\ \text{k}\Omega}$$

$$= 254.3\ \mu\text{A}$$

at the output of A_3,

$$V_g = V_e - (I_4 \times R_5) = -0.605\ \text{V} - (254.3\ \mu\text{A} \times 15\ \text{k}\Omega)$$

$$= -4.42\ \text{V}$$

Practise Problems

14-8.1 An instrumentation amplifier is to be designed to produce a 4.75 V output when the differential input is 50 mV. Using *741* op-amps, determine suitable resistor values.

14-9 Voltage Level Detectors

Op-amps in Switching Applications

Operational amplifiers are often used in circuits in which the output is switched between the positive and negative saturation voltages, $+V_{o(sat)}$ and $-V_{o(sat)}$. The actual voltage change that occurs is known as the *output voltage swing*. For many op-amps (such as a *741*, for example), the output saturation voltages are typically the supply voltage levels minus 1 V. Thus, as illustrated in Fig. 14-30, the typical output voltage swing is,

$$\Delta V \approx (V_{CC} - 1\ \text{V}) - (V_{EE} + 1\ \text{V}) \qquad \textbf{(14-20)}$$

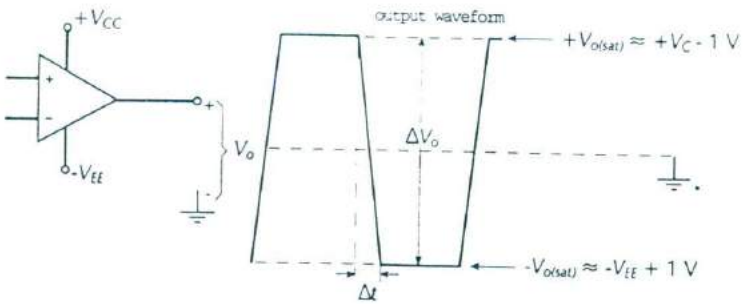


Figure 14-30
An operational amplifier used in a switching application produces an output voltage that switches between positive and negative saturation levels.

For many op-amps the output can be switched from one supply level to the other (there is no 1 V drop), so that

$$\Delta V \approx V_{CC} - V_{EE} \qquad \textbf{(14-21)}$$

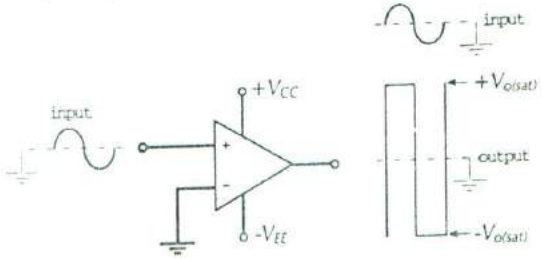
This is referred to as *rail-to-rail* operation.

The switching speed, or rate-of change, of the op-amp output voltage is termed the *slew rate (SR)*. Refering to Fig. 14-30,

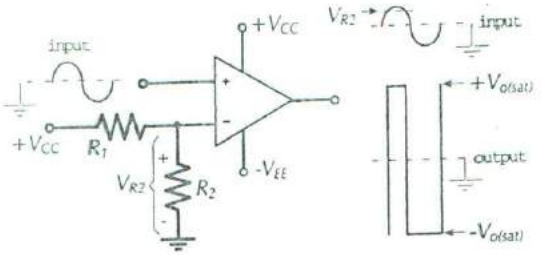
$$SR = \frac{\Delta V}{\Delta t} \qquad \textbf{(14-22)}$$

Suppose the output changes from -10 to +10 V; the voltage change is $\Delta V = 20$ V. If the transition time (or *rise time*, see Section 8-5), is $\Delta t = 1$ μs, the slew rate is 20 V/μs.

Another integrated circuit known as a *voltage comparator*[1] is often substituted in place of an operational amplifier in switching applications. Voltage comparators are similar to op-amps in that they have two (inverting and noninverting) input terminals and one output. However, comparators are designed exclusively for switching, and they have slew rates much faster that those available with op-amps.



(a) Noninverting zero crossing detector



(b) Voltage level detector

Figure 14-31
Operation amplifiers can be connected to function as zero crossing detectors, or as voltage level detectors.

Zero Crossing Detector

The *zero crossing detector* circuit in Fig. 14-31(a) is seen to be simply an operational amplifier with the inverting input grounded and the signal applied to the noninverting input. When the input is above ground level the output is saturated at its positive

[1] David A. Bell, *Solid State Pulse Circuits*, 4th ed. (1997), p. 193.

maximum, and when the input is below ground the output is at its negative maximum level. This is illustrated by the input and output waveforms which show that the output voltage changes from one extreme to the other each time the input voltage crosses zero. The input waveform could have any shape (sinusoidal, pulse, ramp, etc.), and the output will always be a rectangular-type wave.

The actual input voltage that causes the output to switch is not precisely zero, but some very small voltage above or below zero, depending upon the op-amp open-loop gain.

If the op-amp non-inverting input is grounded and the signal is applied to the inverting input in Fig. 14-31(a), the output is negative when the input is above ground, and vice versa. Because of the waveform inversion, this circuit is often termed an *inverter*.

The circuit in Fig. 14-31(b) has the op-amp inverting input biased via a voltage divider (R_1 and R_2). The bias voltage level (V_{R2}) could be positive or negative. In the circuit illustrated, the bias voltage is a positive quantity. The waveforms show that the output voltage changes when the input voltage crosses the bias level. This circuit is appropriately named a *voltage level detector*.

Example 14-12

For the zero crossing detector in Fig. 14-32 determine the typical output voltage swing, and the typical input voltage level above and below ground at which the output switches. Also, calculate the rise time of the output voltage.

Solution

Eq. 14-20, $\Delta V \approx (V_{CC} - 1\text{ V}) - (V_{II} + 1\text{ V}) \approx (15\text{ V} - 1\text{ V}) - (-15\text{ V} + 1\text{ V})$

$\approx 28\text{ V}$

From Appendix 1-13,

$A_v = 200\,000$ (typical), and $SR = 0.5\text{ V}/\mu\text{s}$

$$V_i = \frac{V_o}{A_v} = \frac{\pm 14\text{ V}}{200\,000}$$

$$= \pm 70\,\mu\text{V}$$

From Eq. 14-22,

$$\Delta t = \frac{\Delta V}{SR} = \frac{28\text{ V}}{0.5\text{ V}/\mu\text{s}}$$

$$= 56\,\mu\text{s}$$

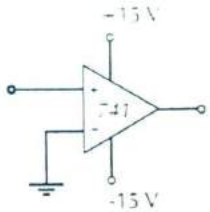


Figure 14-32
Zero crossing detector circuit for Ex. 14-12.

Practise Problems

14-9.1 A 353 op-amp with a ±18 V supply is used as a zero crossing detector. Determine the typical output voltage swing, and the typical input voltage level required to switch the output. Also, calculate the rise time of the output voltage. Appendix 1-15 shows a partial specification for the 353.

14-10 Schmitt Trigger Circuits

Inverting Schmitt Trigger

A *Schmitt trigger* circuit is a fast-operating voltage level detector. When the input voltage arrives at a level determined by the circuit components, the output voltage switches rapidly between its maximum positive level and its maximum negative level.

An op-amp inverting Schmitt trigger circuit is shown in Fig. 14-33 together with input and output waveforms. At first glance the circuit looks like a noninverting amplifier. But note that (unlike a noninverting amplifier) the input voltage (V_i) is applied to the inverting input terminal, and the feedback voltage goes to the noninverting input. The waveforms show that the output switches rapidly from the positive saturation ($+V_{o(sat)}$) voltage to the negative saturation level ($-V_{o(sat)}$) when the input exceeds a certain positive level; the *upper trigger point* (*UTP*). Similarly, the output voltage switches from low to high when the input goes below a negative triggering point; the *lower trigger point* (*LTP*).

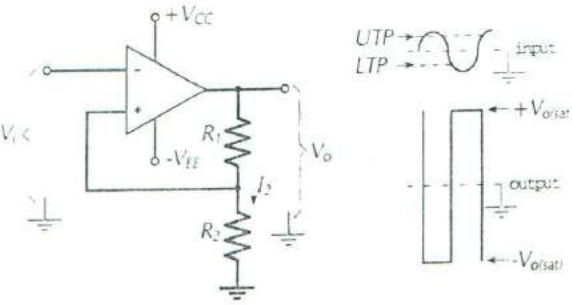


Figure 14-33
A Schmitt trigger circuit is a fast-operating voltage level detector that switches between negative and positive output voltage levels. In an inverting Schmitt trigger circuit the output goes negative when the input goes positive, and vice versa.

Note that after V_i has increased to the *UTP* and V_o has switched to $-V_{o(sat)}$, the output remains at $-V_{o(sat)}$ even when V_i falls below the *UTP*. Switch over from $-V_{o(sat)}$ to $+V_{o(sat)}$ does not occur until V_i = *LTP*. Similarly, after V_i has been reduced to the *LTP* and V_o has switched to $+V_{o(sat)}$, the output remains at $+V_{o(sat)}$ when V_i is increased above the *LTP*. Switch-over from $+V_{o(sat)}$ to $-V_{o(sat)}$ does not occur again until V_i = *UTP*.

Triggering Points

If the output voltage to the circuit in Fig. 14-33 is high, the voltage at the noninverting terminal is,

$$V_{R2} = \frac{+V_o \times R_2}{R_1 + R_2}$$

If the input voltage (at the inverting input terminal) is below V_{R2} (at the noninverting input), the output voltage is kept at its high positive level. For the output to switch to its low level, the input voltage must exceed V_{R2} by a very small amount (approximately 70 μV for a *741* op-amp). So, the *UTP* essentially equals V_{R2}.

$$UTP = \frac{+V_o \times R_2}{R_1 + R_2} \qquad (14\text{-}23)$$

When the output is negative, the *LTP* can be calculated as,

$$LTP = \frac{-V_o \times R_2}{R_1 + R_2} \qquad (14\text{-}24)$$

Input/Output Characteristic

A graph of output voltage (V_o) versus input voltage (V_i) can be plotted for an inverting Schmitt trigger circuit, as shown in Fig. 14-34. This is the circuit input/output characteristic. To understand the characteristic, consider the voltages at each of the numbered points on the graph:

- At *point 1*, $V_o = +V_{o(sat)}$, and $V_i < LTP$, thus keeping $V_o = +V_{o(sat)}$.
- From *point 1* through *points 2* and *3*, V_o remains at $+V_{o(sat)}$ as V_i is increased through the *LTP* and through zero, until $V_i = UTP$.
- From *point 3* to *point 4*, V_o switches rapidly from $+V_{o(sat)}$ to $-V_{o(sat)}$ when $V_i = UTP$.
- From *point 4* to *point 5*, V_o remains at $-V_{o(sat)}$ as V_i is increased above the *UTP*.
- From *point 5* through *points 4* and *6*, V_o remains at $-V_{o(sat)}$ as V_i is reduced through the *UTP* and through zero, until $V_i = LTP$.
- From *point 6* to *point 2*, V_o switches rapidly from $-V_{o(sat)}$ to $+V_{o(sat)}$ when $V_i = LTP$.
- From *point 2* to *point 1*, V_o remains at $+V_{o(sat)}$ as V_i is reduced below the *LTP*.

The difference between the *UTP* and the *LTP* is termed *hysteresis*. Some applications require a small amount of hysteresis, and for other applications a large amount of hysteresis is essential.

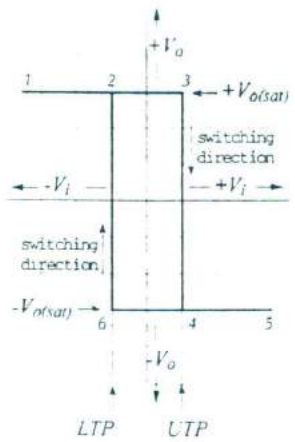


Figure 14-34
Output/input characteristics for an inverting Schmitt trigger circuit.

Circuit Design

Design procedure for a Schmitt trigger circuit is similar to op-amp amplifier design. A voltage divider current (I_2 in Fig. 14-33) is selected much larger than the op-amp input bias current. The resistor values are then calculated as,

$$R_2 = \frac{UTP}{I_2} \qquad (14\text{-}25)$$

and,

$$R_1 = \frac{V_{o(sat)} - UTP}{I_2} \qquad (14\text{-}26)$$

Example 14-13

Using a *741* op-amp, calculate resistor values for the Schmitt trigger circuit in Fig. 14-35 to give triggering points of ±5 V.

Solution

Select, $I_1 \approx 100\, I_B = 100 \times 500$ nA

$= 50\,\mu A$

Eq. 14-25, $$R_2 = \frac{UTP}{I_2} = \frac{5\text{ V}}{50\,\mu A}$$

$= 100\text{ k}\Omega$ (standard value)

Eq. 14-26, $$R_1 = \frac{V_{o(sat)} - UTP}{I_2} \approx \frac{(15\text{ V} - 1\text{ V}) - 5\text{ V}}{50\,\mu A}$$

$= 180\text{ k}\Omega$ (standard value)

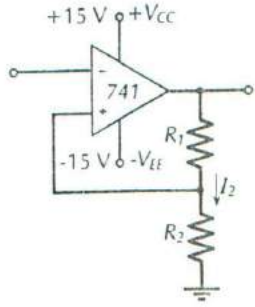
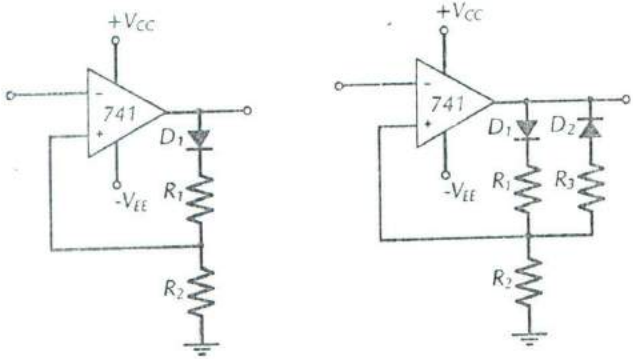


Figure 14-35
Inverting Schmitt trigger circuit for Ex. 14-13.

Adjusting the Trigger Points

Many Schmitt trigger circuit applications require *UTP* and *LTP* levels that are not equal in magnitude. This is usually achieved by the use of diodes, as illustrated in Fig. 14-36.

The circuit shown in Fig. 14-36(a) simply has a diode (D_1) connected in series with resistor R_1. The diode is forward biased only when the op-amp output is a positive quantity. At this time, the *UTP* is V_{R2}, as before. When V_o is negative, D_1 is reverse biased, making I_2 equal zero. Consequently, there is no voltage drop across R_2, and so the noninverting terminal is grounded via R_2. This gives a zero level for the *LTP*. Thus, this circuit has a positive *UTP* and a zero voltage *LTP*.



(a) Schmitt circuit with *LTP* = 0

(b) Schmitt circuit with different *UTP* and *LTP* levels

Figure 14-36
Diodes can be used with inverting Schmitt trigger circuits to produce different levels of positive and negative triggering voltages.

Figure 14-36(b) shows a circuit with two different-level trigger points. When V_o is positive, D_1 is forward biased and D_2 is reversed, and the *UTP* is set by resistors R_1 and R_2. With V_o negative, D_2 is forward biased and D_1 is reversed. The *LTP* is now determined by the resistances of R_3 and R_2.

The diode forward voltage drop (V_F) must be accounted for when calculating the trigger points for both of the circuits in Fig. 14-36. This is done simply by replacing V_o with ($V_{o(sat)} - V_F$) in Eqs. 14-25 and 14-26. Another important design consideration is that the

voltage divider current (I_2) should normally be a minimum of 100 μA for satisfactory diode operation.

Noninverting Schmitt Trigger

A noninverting Schmitt trigger circuit is shown in Fig. 14-37. This circuit looks like an inverting amplifier, but note that (unlike an inverting amplifier) the inverting input is grounded and the noninverting input is connected to the junction of R_1 and R_2. The waveforms in Fig. 14-37 show that V_o switches rapidly from $-V_{o(sat)}$ to $+V_{o(sat)}$ when V_i arrives at the *UTP*, and that V_o switches back to $-V_{o(sat)}$ when V_i falls to the *LTP*.

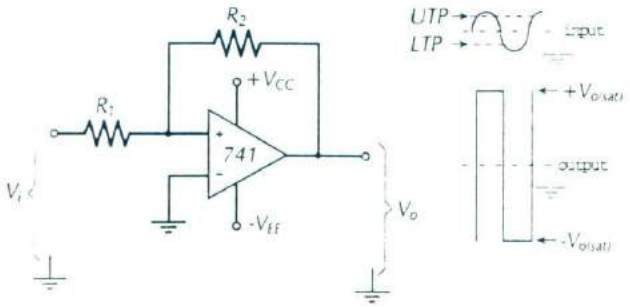


Figure 14-37 Noninverting Schmitt trigger circuit. The output goes positive when the input arrives at the *UTP*, and negative when $V_i = LTP$.

Consider the situation when $V_i = UTP$ and V_o has just switched to $+V_{o(sat)}$. The voltage at the junction of R_1 and R_2 is pulled up far above the ground level voltage at the op-amp inverting input terminal. So, the positive voltage at the noninverting input keeps the output at its positive saturation level. To switch the output to $-V_{o(sat)}$, the voltage at the junction of R_1 and R_2 must be pulled down to the (ground level) voltage at the inverting input terminal. This occurs when V_i is at the *LTP*, [see Fig. 14-38(a)]. So, switching occurs when one end of R_1 (the right end) is at ground, and the other (left) end is at $V_i = LTP$; that is, when $V_{R1} = LTP$. Similarly, switching in the other direction occurs when $V_{R1} = UTP$, [Fig. 14-38(b)]. So, at the trigger points,

$$V_i = UTP = LTP = I_2 R_1$$

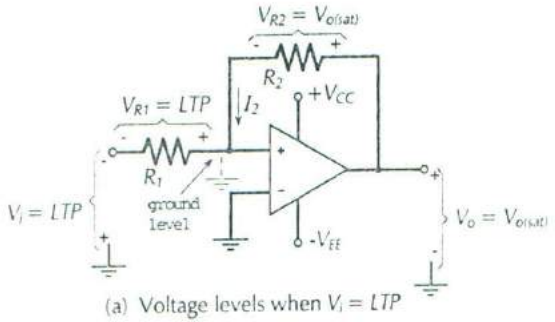
Figure 14-38(a) and (b) show that the output voltage is at one of its saturation levels at the instant of triggering. This means that one end of R_2 is at ground (left end), and the other (right) end is at $V_{o(sat)}$. So, $V_{R2} = V_{o(sat)}$ when triggering occurs.

giving, $$I_2 = \frac{V_{o(sat)}}{R_2}$$

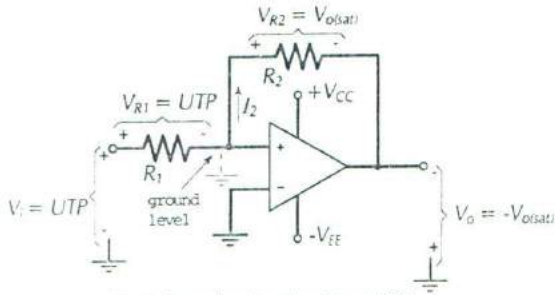
also, $$UTP = I_2 R_1$$

so, $$\boldsymbol{UTP = V_{o(sat)} \times \frac{R_1}{R_2}} \qquad \textbf{(14-27)}$$

and, $$LTP = V_{o(sat)} \times \frac{R_1}{R_2} \quad (14\text{-}28)$$



(a) Voltage levels when $V_i = LTP$



(b) Voltage levels when $V_i = UTP$

Figure 14-38
At the instant of switching in a noninverting Schmitt trigger circuit, the op-amp noninverting input terminal voltage must be at ground level.

Design procedure for a noninverting Schmitt trigger circuit is just as simple as for the inverting circuit. Voltage divider current I_2 is again selected much larger than the op-amp input bias current. Then the resistor values are,

$$R_1 = \frac{UTP}{I_2} \quad (14\text{-}29)$$

and, $$R_2 = \frac{V_{o(sat)}}{I_2} \quad (14\text{-}30)$$

Noninverting Schmitt trigger circuits can be designed for different upper and lower trigger point voltages by the use of diodes, as in the case of the inverting circuit. Figure 14-39(a) and (b) shows two possible circuits. The diode forward voltage drop (V_F) must be included in the *UTP* and *LTP* calculations.

Example 14-14

Determine the upper and lower trigger points for the noninverting Schmitt trigger circuit shown in Fig. 14-39(b). Assume that the op-amp used can be rail-to-rail operated.

Solution

With rail-to-rail operation,

$$V_{o(sat)} = \pm V_{CC} = \pm 15 \text{ V}$$

UTP calculation (including V_F):

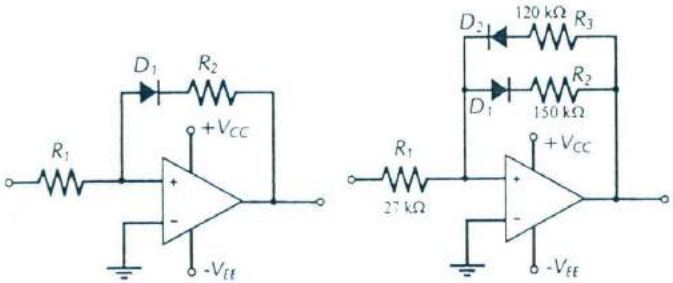
From Eq. 14-30, $$I_2 = \frac{V_{o(sat)} - V_F}{R_2} = \frac{15 \text{ V} - 0.7 \text{ V}}{150 \text{ k}\Omega}$$
$$= 95.3 \, \mu\text{A}$$

From Eq. 14-29, $$UTP = I_2 R_1 = 95.3 \, \mu\text{A} \times 27 \text{ k}\Omega$$
$$= 2.57 \text{ V}$$

LTP calculation (including V_F):

From Eq. 14-30, $$I_3 = \frac{V_{o(sat)} - V_F}{R_3} = \frac{15 \text{ V} - 0.7 \text{ V}}{120 \text{ k}\Omega}$$
$$= 119 \, \mu\text{A}$$

From Eq. 14-29, $$LTP = I_3 R_1 = 119 \, \mu\text{A} \times 27 \text{ k}\Omega$$
$$= 3.2 \text{ V}$$



(a) Noninverting Schmitt circuit with *LTP* = 0

(b) Noninverting Schmitt circuit with different *UTP* and LTP levels.

Figure 14-39
Diodes can be used to produce different UTP and LTP levels for noninverting Schmitt trigger circuits.

Practise Problems

14-10.1 Using a *741* op-amp with a ±12 V supply, design an inverting Schmitt trigger circuit [as in Fig. 14-36(b)] to have *UTP* = 3 V and *LTP* = -2 V.

14-10.2 Design a noninverting Schmitt trigger circuit to have approximately ±1 V trigger points. Use an *353* op-amp with a ±15 V supply.

Chapter-14 Review Questions

Section 14-1

14-1 Sketch the circuit symbol for an operational amplifier, identify all terminals, and briefly explain.

14-2 Sketch the input and output stages of a bipolar operational amplifier, explain the circuit operation, and discuss the input and output impedances.

14-3 Repeat Question 14-2 for a *BIFET* operational amplifier.

14-4 List the most important parameters for an operational amplifier, and state typical values for each parameter.

Section 14-2

14-5 Draw a complete circuit diagram to show an operational amplifier with a signal source capacitor-coupled to the noninverting input, and 100% feedback from the output to the inverting input terminal. Explain the requirement for all components.

14-6 Draw a complete circuit diagram for an operational amplifier with a plus/minus supply, its noninverting input terminal biased to a positive voltage level, and 100% feedback from the output to the inverting input terminal. Explain the requirement for all components, and discuss the component current levels.

14-7 An operational amplifier is to use a single-polarity supply, and have its noninverting input terminal biased to a positive voltage level. Also, 100% feedback is to be provided from the output to the inverting input terminal. Draw the circuit diagram, and explain the function of each component.

14-8 Explain output voltage offset nulling, and show how it can be accomplished in a *741* op-amp.

Section 14-3

14-9 Draw a circuit diagram for a direct-coupled voltage follower, identifying all terminals. Also, sketch a basic op-amp (internal) circuit with the external connection for voltage follower operation. Explain the circuit operation.

14-10 Discuss the performance of a voltage follower, and compare it to an emitter follower.

14-11 Sketch a capacitor-coupled voltage follower circuit, and explain the effects of capacitor-coupling on the circuit input impedance.

Section 14-4

14-12 Draw a circuit diagram for a direct-coupled noninverting amplifier. Identify all terminals and explain the circuit operation. Also, derive the closed-loop voltage gain equation, and write equations for the input and output impedances.

14-13 Sketch a basic operational amplifier (internal) circuit with the external connection for noninverting amplifier operation. Explain how the circuit amplifies a signal.

14-14 Sketch a capacitor-coupled noninverting amplifier circuit. Explain the circuit operation, and discuss the effects of capacitor-coupling on the circuit input impedance.

Section 14-5

14-15 Sketch a circuit diagram for a direct-coupled inverting amplifier. Identify all terminals and explain the circuit operation. Also, derive the closed-loop voltage gain equation, and write equations for the input and output impedances.

14-16 Sketch a circuit for capacitor-coupled inverting amplifier. Explain the amplifier operation, and discuss the effects of capacitor-coupling on the circuit input impedance.

Section 14-6

14-17 Sketch a three-input summing amplifier circuit and explain its operation.

14-18 For a three-input summing amplifier, derive an equation for the output voltage in terms of the input voltage and the circuit components.

Section 14-7

14-19 Sketch the circuit of an op-amp difference amplifier. Explain its operation, and derive an equation for the output voltage in terms of the input and the circuit components.

14-20 Identify the input resistances for the difference amplifier in Question 14-19. Also, discuss the effects of a common-mode input voltage, and show how common-mode voltages can be nulled.

Section 14-8

14-21 Draw the circuit diagram for an instrumentation amplifier, identify each section of the circuit, and explain its operation.

14-22 Derive an equation for the overall voltage gain of the instrumentation amplifier circuit drawn for Question 14-21. Discuss the effects of common mode input voltages.

Section 14-9

14-23 Sketch circuit diagrams for an op-amp used as (a) a zero-crossing detector, (b) as a voltage level detector. Show typical input and output waveforms and briefly explain. Define slew rate, and show its effect on an op-amp output waveform.

Section 14-10

14-24 Draw the circuit diagram of an op-amp inverting Schmitt trigger circuit. Sketch typical input and output waveforms,

and explain the circuit operation. Write equations for the circuit upper and lower trigger points.

14-25 Sketch typical output/input characteristics for an inverting Schmitt trigger circuit. Identify the upper and lower trigger points, and explain the characteristics.

14-26 Draw circuit diagrams for inverting Schmitt trigger circuits with different levels of positive and negative trigger points. Explain.

14-27 Draw the circuit diagram of an op-amp noninverting Schmitt trigger circuit. Sketch typical input and output waveforms, and explain the circuit operation. Write equations for the circuit upper and lower trigger points.

14-28 Draw circuit diagrams for noninverting Schmitt trigger circuits with different levels of positive and negative trigger points. Explain.

Chapter-14 Problems

Section 14-1

14-1 Referring to the *741* operational amplifier specification in Appendix 1-13, determine typical values of the following parameters: input resistance, input bias current, output resistance, output short-circuit current, supply current, power dissipation.

14-2 Referring to Appendix 1-14, determine typical values of the following parameters for a *LM308* operational amplifier: input resistance, input bias current, supply current, power supply rejection ratio.

14-3 From the *LF353A* op-amp specification in Appendix 1-15, determine typical values of the following parameters: supply current, common-mode rejection ratio, output voltage swing, input offset voltage.

Section 14-2

14-4 A *741* op-amp with a ±9 V supply uses voltage divider bias to provide +3 V at the noninverting input terminal. There is also 100% feedback from the output to the inverting input. Determine suitable resistor values.

14-5 Determine resistor values for a *741* op-amp with a +18 V supply, +9 V voltage divider bias at the noninverting input terminal, and 100% feedback from the output to the inverting input.

14-6 Redesign the circuit in Problem 14-4 to use a *LM108* op-amp. Note that, because the *LM108* has a very low bias current, it should be treated like a *BIFET* op-amp.

14-7 Redesign the circuit in Problem 14-5 to use a *LF353* op-amp. Then, investigate the effect of substituting a *741* in place of the *LF353* without changing the resistor values.

Section 14-3

14-8 An operational amplifier with an open-loop of 200 000 is used as a voltage follower. Calculate the precise level of the output voltage if the input voltage is exactly 8 V.

14-9 Calculate the input and output resistance of a voltage follower circuit that uses an op-amp with the following parameters: $A_{v(OL)} = 100\,000$, $r_i = 1\ \text{M}\Omega$, $r_o = 50\ \Omega$.

14-10 Design a capacitor-coupled voltage follower to use a *741* op-amp. The load resistance is 2 kΩ, the signal source resistance is 600 Ω, and the lower cutoff frequency is to be 100 Hz.

14-11 A capacitor-coupled voltage follower uses an op-amp with a 1 μA input bias current. The load resistance is 1 kΩ, and the signal source resistance is 400 Ω. Select suitable component values for the circuit to give a 120 Hz lower cutoff frequency.

Section 14-4

14-12 Design a direct-coupled noninverting amplifier to produce a ±5 V output when the input is ±75 mV. Use a *741* op-amp.

14-13 A direct-coupled noninverting amplifier that uses an op-amp with $I_{B(max)} = 750$ nA is to have a maximum output of ±10 V and a voltage gain of 120. Design the circuit.

14-14 A direct-coupled noninverting amplifier (as in Fig. 14-15) uses a *BIFET* op-amp and has the following resistor values: $R_1 = 22\ \text{k}\Omega$, $R_2 = 1\ \text{M}\Omega$, $R_3 = 22\ \text{k}\Omega$. Calculate the circuit voltage gain.

14-15 Redesign the circuit in Problem 14-12 to use an *LF353 BIFET* op-amp.

14-16 The noninverting amplifier designed for Problem 14-12 is to be modified to operate as a capacitor-coupled circuit with $f_1 = 80$ Hz, $R_L = 100\ \text{k}\Omega$, and $r_s = 300\ \Omega$. Calculate suitable capacitor values.

14-17 Calculate the input impedance of the direct-coupled circuit in Problem 14-12, and of the capacitor-coupled circuit in Problem 14-16.

14-18 A capacitor-coupled noninverting amplifier is to be designed to produce a 7 V output from a 70 mV input. The supply voltage is ±18 V, the lower cutoff frequency is 60 Hz, the load is 82 kΩ, and the signal source resistance is 600 Ω. Design the circuit to have an input impedance of 12 kΩ.

14-19 Design a direct-coupled noninverting amplifier using a *BIFET* op-amp with a 100 000 open-loop voltage gain. The closed-loop gain is to be 45, and the maximum output is to be ±2 V.

14-20 Modify the circuit for Problem 14-19 to make it capacitor-coupled with $R_L = 2\ k\Omega$ and $f_1 = 150$ Hz.

Section 14-5

14-21 A direct-coupled inverting amplifier using a *741* op-amp is to have a 45 mV input signal and a voltage gain of 200. Calculate suitable resistor values and determine the circuit input impedance.

14-22 A direct-coupled inverting amplifier is to have a 1 kΩ input impedance, and is to produce a ±3.3 V output from a ±100 mV input. Determine suitable resistor values.

14-23 Redesign the circuit in Problem 14-21 to use a *BIFET* op-amp.

14-24 The inverting amplifier designed for Problem 14-21 is to be modified to operate as a capacitor-coupled circuit with $f_1 = 50$ Hz, $R_L = 150\ k\Omega$, and $r_s = 300\ \Omega$. Determine suitable capacitor values.

14-25 A capacitor-coupled inverting amplifier is to have a 680 Ω input impedance, and a voltage gain of 49. The load resistance is 12 kΩ, the lower cutoff frequency is to be 40 Hz. Determine suitable component values.

14-26 The inverting amplifier designed for Problem 14-22 is to function as a capacitor-coupled circuit with $f_1 = 30$ Hz, $R_L = 33\ k\Omega$, and $r_s = 600\ \Omega$. Determine suitable capacitor values.

14-27 A capacitor-coupled inverting amplifier is to use a *741* op-amp with a +30 V single-polarity supply, and have $R_L = 5\ k\Omega$, $A_{CL} = 50$, $V_o = \pm 3$ V, and $f_1 = 75$ Hz. Sketch the circuit and determine suitable component values.

Section 14-6

14-28 Design a two-input summing amplifier for a voltage gain of 10 and input levels of 100 mV. Use an operational amplifier with $I_{B(max)} = 1\ \mu A$ and $A_{v(OL)} = 300\ 000$.

14-29 The circuit designed for Problem 14-28 has inputs of 60 mV and 80 mV. Analyze the circuit to determine all voltage and current levels.

14-30 A three-input summing amplifier using a *741* op-amp is to be designed for a voltage gain of 1. The input voltages are approximately 1 V. Calculate suitable component values.

Section 14-7

14-31 The difference amplifier circuit in Fig. 14-27 has the following components: $R_1 = 15\ k\Omega$, $R_2 = 33\ k\Omega$, $R_3 = 6.8\ k\Omega$,

R_4 = (12 kΩ +2.7 kΩ + 500 Ω variable). The input voltages are: V_{i1} (to R_1) = 1.47 V and V_{i2} (to R_3) = 1.23 V. Calculate V_o when R_4 is adjusted to 14.96 kΩ.

14-32 A difference amplifier is to be designed for a voltage gain of 100 and input levels of 100 mV. Using an operational amplifier with $I_{B(max)}$ = 1 μA and $A_{v(OL)}$ = 300 000, determine suitable resistor values.

14-33 If the difference amplifier in Problem 14-31 has a 500 mV common-mode input, calculate the common-mode output voltage: (a) when R_4 is set to its maximum resistance, (b) when R_4 is at its minimum value, (c) when R_4 = 14.96 kΩ.

Section 14-8

14-34 Design an instrumentation amplifier to produce a 3 V output when the inputs are +450 mV and +150 mV. Use *741* op-amps with a ±12 V supply.

14-35 Analyze the circuit designed for Problem 14-34 to determine all current and voltage levels.

Section 14-9

14-36 A zero-crossing detector uses an op-amp with V_{CC} = ±9 V, *SR* = 3 V/μs, and $A_{v(OL)}$ = 100 000. Calculate the typical output voltage swing, the output rise time, and the input voltage level required to switch the output.

Section 14-10

14-37 Using a *741* op-amp with V_{CC} = ±18 V, design an inverting Schmitt trigger circuit to have ±2 V triggering points.

14-38 Plot the output/input characteristics for the circuit in Problem 14-37.

14-39 Design a noninverting Schmitt trigger circuit to fulfil the specification in Problem 14-37.

14-40 An inverting Schmitt trigger circuit is to be designed to have *UTP* = 0 V and *LTP* = -1.5 V. Sketch the circuit and determine suitable component values if a *741* op-amp is used with a ±15 V supply.

14-41 An noninverting Schmitt trigger circuit is to be designed to have *UTP* = 1 V and *LTP* = -0.5 V. Sketch the circuit and determine suitable component values if a *LF353* op-amp is used with a ±12 V supply.

14-42 An noninverting Schmitt trigger circuit using a *741* op-amp with a ±10 V supply is to have trigger points adjustable from ±0.5 V to ±0.75 V. Sketch the circuit and determine suitable component values.

Practise Problem Answers

14-1.1 300 000, 0.8 nA, 0.7 mV, 70 MΩ
14-1.2 100 000, 50 pA, 5 mV, 10^{12} Ω
14-2.1 220 kΩ, 220 kΩ, 100 kΩ
14-2.2 180 kΩ, (220 kΩ + 33 kΩ), 100 kΩ
14-3.1 1.5 μF, 0.33 μF
14-3.2 0.68 μF, 1 μF
14-3.3 60 mV
14-4.1 1.8 kΩ, (68 kΩ + 2.2 kΩ), 1.8 kΩ
14-4.2 4.7 kΩ, (82 kΩ + 6.8 kΩ), 4.7 kΩ, 18 μF, 10 μF
14-4.3 180 kΩ, 1 MΩ, (220 kΩ + 33 kΩ)
14-5.1 5.6 kΩ, (82 kΩ + 2.2 kΩ), 5.6 kΩ
14-5.2 8 μF, 15 μF
14-5.3 (33 kΩ + 33 kΩ), 1 MΩ, 68 kΩ
14-6.1 4.7 kΩ, 4.7 kΩ, 47 kΩ, 2.2 kΩ
14-6.2 -10.6 V, 2.27 μA, 4.55 μA, 3.79 μA, 10.6 μA
14-7.1 +7.5 V, -33.9 μA, -33.9 μA, 75.76 μA, 1.36 V
14-7.2 25×10^{-3}
14-7.3 (100 kΩ + 68 kΩ), 1 MΩ, 27 kΩ, (100 kΩ + 68 kΩ)
14-8.1 47 kΩ, 1 kΩ, 47 kΩ, 47 kΩ, 47 kΩ, 47 kΩ, 47 kΩ
14-9.1 33 V, ±330 μV, 2.5 μS
14-10.1 (68 kΩ + 27 kΩ), 39 kΩ, (150 kΩ + 12 kΩ)
14-10.2 (56 kΩ + 18 kΩ), 1 MΩ